Dimitris E Ioannou

List of Publications by Year
in descending order

21	384	933264 10	1199470 12
papers	citations	h-index	g-index

21	21	21	493
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	High-performance room-temperature TiO2-functionalized GaN nanowire gas sensors. Applied Physics Letters, 2019, 115, .	1.5	22
2	Highly Efficient Rapid Annealing of Thin Polar Polymer Film Ferroelectric Devices at Subâ€Glass Transition Temperature. Advanced Functional Materials, 2018, 28, 1704165.	7.8	2
3	Ferroelectricity in Polar Polymerâ€Based FETs: A Hysteresis Analysis. Advanced Functional Materials, 2018, 28, 1705250.	7.8	14
4	Precise gas discrimination with cross-reactive graphene and metal oxide sensor arrays. Applied Physics Letters, 2018, 113, .	1.5	16
5	Glassy-electret random access memory - A naturally nanoscale memory concept. , 2018, , .		0
6	On the Nature of the Memory Mechanism of Gated-Thyristor Dynamic-RAM Cells. IEEE Journal of the Electron Devices Society, 2015, 3, 468-471.	1.2	15
7	On the T-RAM and FED-RAM memory mechanism. , 2015, , .		2
8	SOI FED-SRAM Cell: Structure and Operation. IEEE Transactions on Electron Devices, 2015, 62, 2865-2870.	1.6	21
9	High performance topological insulator nanowire field-effect transistors. , 2013, , .		2
10	SOI Field-Effect Diode DRAM Cell: Design and Operation. IEEE Electron Device Letters, 2013, 34, 1002-1004.	2.2	49
11	Topological Insulator Bi2Se3 Nanowire High Performance Field-Effect Transistors. Scientific Reports, 2013, 3, .	1.6	73
12	Non-volatile memory with self-assembled ferrocene charge trapping layer. Applied Physics Letters, 2013, 103, .	1.5	19
13	Degradation of High-k/Metal Gate nMOSFETs Under ESD-Like Stress in a 32-nm Technology. IEEE Transactions on Device and Materials Reliability, 2011, 11, 118-125.	1.5	8
14	Design and analysis of multi-gate field-effect-diodes for embedded memory. , 2011, , .		3
15	Self-aligned multi-channel silicon nanowire field-effect transistors. , 2011, , .		0
16	Steep subthreshold slope nanowire FETs with gate-induced Schottky-barrier tunneling. , 2009, , .		2
17	Scaling of the SOI field effect diode (FED) for memory application. , 2009, , .		27
18	Design and optimization of the SOI field effect diode (FED) for ESD protection. Solid-State Electronics, 2008, 52, 1482-1485.	0.8	30

#	Article	IF	Citations
19	Effect of Floating-Body and Stress Bias on NBTI and HCI on 65-nm SOI pMOSFETs. IEEE Electron Device Letters, 2008, 29, 262-264.	2.2	22
20	Methods to Characterize the Electrical and Mechanical Properties of Si Nanowires. AIP Conference Proceedings, 2007, , .	0.3	0
21	Field Effect Diode (FED): A novel device for ESD protection in deep sub-micron SOI technologies. , 2006, , .		57