Guido Groeseneken

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838	18,822	62	104
papers	citations	h-index	g-index

914	21,940	2.6	6.3
ext. papers	ext. citations	avg, IF	L-index

#	Paper	IF	Citations
838	A reliable approach to charge-pumping measurements in MOS transistors. *IEEE Transactions on Electron Devices*, **1984**, 31, 42-53	2.9	1038
837	New insights in the relation between electron trap generation and the statistical properties of oxide breakdown. *IEEE Transactions on Electron Devices*, **1998**, 45, 904-911	2.9	479
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835	. *IEEE Transactions on Electron Devices*, **1988**, 35, 2194-2209	2.9	323
834	Tunnel field-effect transistor without gate-drain overlap. *Applied Physics Letters*, **2007**, 91, 053102	3.4	319
833	. *IEEE Transactions on Electron Devices*, **2008**, 55, 547-556	2.9	314
832	. *IEEE Transactions on Electron Devices*, **2012**, 59, 292-301	2.9	294
831	Origin of the threshold voltage instability in SiO2/HfO2 dual layer gate dielectrics. *IEEE Electron Device Letters*, **2003**, 24, 87-89	4.4	280
830	Electrical properties of high-�gate dielectrics: Challenges, current issues, and possible solutions. *Materials Science and Engineering Reports*, **2006**, 51, 37-85	30.9	209
829	Modeling the single-gate, double-gate, and gate-all-around tunnel field-effect transistor. *Journal of Applied Physics*, **2010**, 107, 024518	2.5	179
828	A consistent model for the thickness dependence of intrinsic breakdown in ultra-thin oxides		176
827	Endurance/Retention Trade-off on $hbox{HfO}_{2}/hbox{Metal}$ Cap 1T1R Bipolar RRAM. *IEEE Transactions on Electron Devices*, **2013**, 60, 1114-1121	2.9	175
826	Origin of NBTI variability in deeply scaled pFETs **2010**,		173
825	Complementary Silicon-Based Heterostructure Tunnel-FETs With High Tunnel Rates. *IEEE Electron Device Letters*, **2008**, 29, 1398-1401	4.4	133
824	. *IEEE Transactions on Electron Devices*, **2012**, 59, 3243-3249	2.9	132
823	Consistent model for short-channel nMOSFET after hard gate oxide breakdown. *IEEE Transactions on Electron Devices*, **2002**, 49, 507-513	2.9	127
822	Ubiquitous relaxation in BTI stressing�New evaluation and insights **2008**,		126

821	Degradation and breakdown in thin oxide layers: mechanisms, models and reliability prediction. *Microelectronics Reliability*, **1999**, 39, 1445-1460	1.2	123
820	Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability. *IEEE Transactions on Electron Devices*, **2002**, 49, 500-506	2.9	117
819	Forward Bias Gate Breakdown Mechanism in Enhancement-Mode p-GaN Gate AlGaN/GaN High-Electron Mobility Transistors. *IEEE Electron Device Letters*, **2015**, 36, 1001-1003	4.4	116
818	Boosting the on-current of a n-channel nanowire tunnel field-effect transistor by source material optimization. *Journal of Applied Physics*, **2008**, 104, 064514	2.5	107
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816	A new model for the field dependence of intrinsic and extrinsic time-dependent dielectric breakdown. *IEEE Transactions on Electron Devices*, **1998**, 45, 472-481	2.9	104
815	. *IEEE Transactions on Electron Devices*, **1991**, 38, 1820-1831	2.9	104
814	Hot-carrier degradation phenomena in lateral and vertical DMOS transistors. *IEEE Transactions on Electron Devices*, **2004**, 51, 623-628	2.9	103
813	Drain voltage dependent analytical model of tunnel field-effect transistors. *Journal of Applied Physics*, **2011**, 110, 024510	2.5	98
812	On the Gradual Unipolar and Bipolar Resistive Switching of TiNHfO[sub 2]Pt Memory Systems. *Electrochemical and Solid-State Letters*, **2010**, 13, G54		97
811	Analysis of trap-assisted tunneling in vertical Si homo-junction and SiGe hetero-junction Tunnel-FETs. *Solid-State Electronics*, **2013**, 83, 50-55	1.7	96
810	Optimization of Gate-on-Source-Only Tunnel FETs With Counter-Doped Pockets. *IEEE Transactions on Electron Devices*, **2012**, 59, 2070-2077	2.9	94
809	Statistics of Multiple Trapped Charges in the Gate Oxide of Deeply Scaled MOSFET DevicesApplication to NBTI. *IEEE Electron Device Letters*, **2010**, 31, 411-413	4.4	94
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807	Planar Bulk MOSFETs Versus FinFETs: An Analog/RF Perspective. *IEEE Transactions on Electron Devices*, **2006**, 53, 3071-3079	2.9	91
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805	Impact of field-induced quantum confinement in tunneling field-effect devices. *Applied Physics Letters*, **2011**, 98, 143503	3.4	89
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802	Disorder-controlled-kinetics model for negative bias temperature instability and its experimental verification		84
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800	Performance Optimization of Au-Free Lateral AlGaN/GaN Schottky Barrier Diode With Gated Edge Termination on 200-mm Silicon Substrate. *IEEE Transactions on Electron Devices*, **2016**, 63, 997-1004	2.9	82
799	SiGe Channel Technology: Superior Reliability Toward Ultrathin EOT DevicesPart I: NBTI. *IEEE Transactions on Electron Devices*, **2013**, 60, 396-404	2.9	81
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797	Direct Measurement of Top and Sidewall Interface Trap Density in SOI FinFETs. *IEEE Electron Device Letters*, **2007**, 28, 232-234	4.4	79
796	On the properties of the gate and substrate current after soft breakdown in ultrathin oxide layers. *IEEE Transactions on Electron Devices*, **1998**, 45, 2329-2334	2.9	78
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788	Reliability: a possible showstopper for oxide thickness scaling?. *Semiconductor Science and Technology*, **2000**, 15, 436-444	1.8	71
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773	Analytical percolation model for predicting anomalous charge loss in flash memories. *IEEE Transactions on Electron Devices*, **2004**, 51, 1392-1400	2.9	60
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762	Characterization of the V/sub T/-instability in SiO/sub 2//HfO/sub 2/ gate dielectrics		54
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