

Guido Groeseneken

List of Publications by Year in descending order

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904
papers

24,217
citations

18436

62
h-index

24915

109
g-index

914
all docs

914
docs citations

914
times ranked

9060
citing authors

#	ARTICLE	IF	CITATIONS
1	A reliable approach to charge-pumping measurements in MOS transistors. IEEE Transactions on Electron Devices, 1984, 31, 42-53.	1.6	1,267
2	New insights in the relation between electron trap generation and the statistical properties of oxide breakdown. IEEE Transactions on Electron Devices, 1998, 45, 904-911.	1.6	570
3	Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation. IEEE Transactions on Electron Devices, 1989, 36, 1318-1335.	1.6	412
4	Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFETs. IEEE Transactions on Electron Devices, 1988, 35, 2194-2209.	1.6	400
5	Tunnel field-effect transistor without gate-drain overlap. Applied Physics Letters, 2007, 91, .	1.5	384
6	Direct and Indirect Band-to-Band Tunneling in Germanium-Based TFETs. IEEE Transactions on Electron Devices, 2012, 59, 292-301.	1.6	370
7	On the Correct Extraction of Interface Trap Density of MOS Devices With High-Mobility Semiconductor Substrates. IEEE Transactions on Electron Devices, 2008, 55, 547-556.	1.6	339
8	Origin of the threshold voltage instability in SiO ₂ /HfO ₂ dual layer gate dielectrics. IEEE Electron Device Letters, 2003, 24, 87-89.	2.2	330
9	Electrical properties of high- ϵ gate dielectrics: Challenges, current issues, and possible solutions. Materials Science and Engineering Reports, 2006, 51, 37-85.	14.8	241
10	A consistent model for the thickness dependence of intrinsic breakdown in ultra-thin oxides. , 0, , .		231
11	Origin of NBTI variability in deeply scaled pFETs. , 2010, , .		227
12	Endurance/Retention Trade-off on $\text{HfO}_2/\text{Metal}$ Cap 1T1R Bipolar RRAM. IEEE Transactions on Electron Devices, 2013, 60, 1114-1121.	1.6	225
13	Modeling the single-gate, double-gate, and gate-all-around tunnel field-effect transistor. Journal of Applied Physics, 2010, 107, .	1.1	217
14	Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability. IEEE Transactions on Electron Devices, 2002, 49, 500-506.	1.6	199
15	Ubiquitous relaxation in BTI stressingâ€”New evaluation and insights. , 2008, , .		179
16	Balancing SET/RESET Pulse for 10^{10} Endurance in HfO_2/Hf 1T1R Bipolar RRAM. IEEE Transactions on Electron Devices, 2012, 59, 3243-3249.	1.6	166
17	Complementary Silicon-Based Heterostructure Tunnel-FETs With High Tunnel Rates. IEEE Electron Device Letters, 2008, 29, 1398-1401.	2.2	161
18	Forward Bias Gate Breakdown Mechanism in Enhancement-Mode p-GaN Gate AlGaIn/GaN High-Electron Mobility Transistors. IEEE Electron Device Letters, 2015, 36, 1001-1003.	2.2	158

#	ARTICLE	IF	CITATIONS
19	Consistent model for short-channel nMOSFET after hard gate oxide breakdown. IEEE Transactions on Electron Devices, 2002, 49, 507-513.	1.6	155
20	Degradation and breakdown in thin oxide layers: mechanisms, models and reliability prediction. Microelectronics Reliability, 1999, 39, 1445-1460.	0.9	142
21	Temperature dependence of threshold voltage in thin-film SOI MOSFETs. IEEE Electron Device Letters, 1990, 11, 329-331.	2.2	138
22	Performance Optimization of Au-Free Lateral AlGaIn/GaN Schottky Barrier Diode With Gated Edge Termination on 200-mm Silicon Substrate. IEEE Transactions on Electron Devices, 2016, 63, 997-1004.	1.6	132
23	Planar Bulk MOSFETs Versus FinFETs: An Analog/RF Perspective. IEEE Transactions on Electron Devices, 2006, 53, 3071-3079.	1.6	128
24	Hole Traps in Silicon Dioxides – Part I: Properties. IEEE Transactions on Electron Devices, 2004, 51, 1267-1273.	1.6	126
25	Optimization of Gate-on-Source-Only Tunnel FETs With Counter-Doped Pockets. IEEE Transactions on Electron Devices, 2012, 59, 2070-2077.	1.6	126
26	Boosting the on-current of a n-channel nanowire tunnel field-effect transistor by source material optimization. Journal of Applied Physics, 2008, 104, .	1.1	125
27	Fabrication and Analysis of a $\text{Si}_{0.55}\text{Ge}_{0.45}$ Heterojunction Line Tunnel FET. IEEE Transactions on Electron Devices, 2014, 61, 707-715.	1.6	123
28	Hot-Carrier Degradation Phenomena in Lateral and Vertical DMOS Transistors. IEEE Transactions on Electron Devices, 2004, 51, 623-628.	1.6	120
29	A new model for the field dependence of intrinsic and extrinsic time-dependent dielectric breakdown. IEEE Transactions on Electron Devices, 1998, 45, 472-481.	1.6	118
30	Analysis of trap-assisted tunneling in vertical Si homo-junction and SiGe hetero-junction Tunnel-FETs. Solid-State Electronics, 2013, 83, 50-55.	0.8	117
31	Spectroscopic charge pumping: A new procedure for measuring interface trap distributions on MOS transistors. IEEE Transactions on Electron Devices, 1991, 38, 1820-1831.	1.6	114
32	AC NBTI studied in the 1 Hz -- 2 GHz range on dedicated on-chip CMOS circuits. , 2006, , .		114
33	Drain voltage dependent analytical model of tunnel field-effect transistors. Journal of Applied Physics, 2011, 110, .	1.1	114
34	Statistics of Multiple Trapped Charges in the Gate Oxide of Deeply Scaled MOSFET Devices – Application to NBTI. IEEE Electron Device Letters, 2010, 31, 411-413.	2.2	113
35	Disorder-controlled-kinetics model for negative bias temperature instability and its experimental verification. , 0, , .		111
36	Analysis and modeling of on-chip high-voltage generator circuits for use in EEPROM circuits. IEEE Journal of Solid-State Circuits, 1989, 24, 1372-1380.	3.5	109

#	ARTICLE	IF	CITATIONS
37	On the Gradual Unipolar and Bipolar Resistive Switching of TiN/HfO ₂ /Pt Memory Systems. Electrochemical and Solid-State Letters, 2010, 13, G54.	2.2	109
38	200 V Enhancement-Mode p-GaN HEMTs Fabricated on 200 mm GaN-on-SOI With Trench Isolation for Monolithic Integration. IEEE Electron Device Letters, 2017, 38, 918-921.	2.2	106
39	Temperature dependence of the negative bias temperature instability in the framework of dispersive transport. Applied Physics Letters, 2005, 86, 143506.	1.5	105
40	Atomistic approach to variability of bias-temperature instability in circuit simulations. , 2011, , .		102
41	Measuring the electrical resistivity and contact resistance of vertical carbon nanotube bundles for application as interconnects. Nanotechnology, 2011, 22, 085302.	1.3	101
42	SiGe Channel Technology: Superior Reliability Toward Ultrathin EOT Devices—Part I: NBTI. IEEE Transactions on Electron Devices, 2013, 60, 396-404.	1.6	100
43	Impact of field-induced quantum confinement in tunneling field-effect devices. Applied Physics Letters, 2011, 98, .	1.5	99
44	Comparative study of drain and gate low-frequency noise in nMOSFETs with hafnium-based gate dielectrics. IEEE Transactions on Electron Devices, 2006, 53, 823-828.	1.6	97
45	On the thermal stability of atomic layer deposited TiN as gate electrode in MOS devices. IEEE Electron Device Letters, 2003, 24, 550-552.	2.2	96
46	Figure of merit for and identification of sub-60 mV/decade devices. Applied Physics Letters, 2013, 102, .	1.5	95
47	On the properties of the gate and substrate current after soft breakdown in ultrathin oxide layers. IEEE Transactions on Electron Devices, 1998, 45, 2329-2334.	1.6	94
48	Direct Measurement of Top and Sidewall Interface Trap Density in SOI FinFETs. IEEE Electron Device Letters, 2007, 28, 232-234.	2.2	91
49	Performance Enhancement in Multi Gate Tunneling Field Effect Transistors by Scaling the Fin-Width. Japanese Journal of Applied Physics, 2010, 49, 04DC10.	0.8	90
50	Filament observation in metal-oxide resistive switching devices. Applied Physics Letters, 2013, 102, .	1.5	88
51	NBTI from the perspective of defect states with widely distributed time scales. Reliability Physics Symposium, 2009 IEEE International, 2009, , .	0.0	86
52	Relation between breakdown mode and breakdown location in short channel NMOSFETs and its impact on reliability specifications. , 0, , .		84
53	Reliability: a possible showstopper for oxide thickness scaling?. Semiconductor Science and Technology, 2000, 15, 436-444.	1.0	82
54	Insight Into N/PBTI Mechanisms in Sub-1-nm-EOT Devices. IEEE Transactions on Electron Devices, 2012, 59, 2042-2048.	1.6	82

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55	Low Weibull slope of breakdown distributions in high-k layers. IEEE Electron Device Letters, 2002, 23, 215-217.	2.2	81
56	Impact of fin width on digital and analog performances of n-FinFETs. Solid-State Electronics, 2007, 51, 551-559.	0.8	81
57	Impact of Wire Geometry on Interconnect R_{eff} and Circuit Delay. IEEE Transactions on Electron Devices, 2016, 63, 2488-2496.	1.6	80
58	Temperature dependence of the channel hot-carrier degradation of n-channel MOSFET's. IEEE Transactions on Electron Devices, 1990, 37, 980-993.	1.6	79
59	On the geometric component of charge-pumping current in MOSFETs. IEEE Electron Device Letters, 1993, 14, 107-109.	2.2	78
60	SILC-related effects in flash E ² /PROM's-Part I: A quantitative model for steady-state SILC. IEEE Transactions on Electron Devices, 1998, 45, 1745-1750.	1.6	78
61	Channel Hot Carrier Degradation Mechanism in Long/Short Channel n-FinFETs. IEEE Transactions on Electron Devices, 2013, 60, 4002-4007.	1.6	78
62	Analytical model for a tunnel field-effect transistor. , 2008, , .		77
63	Influence of absorbed water components on SiOCH low-k reliability. Journal of Applied Physics, 2008, 104, .	1.1	77
64	Trap Spectroscopy by Charge Injection and Sensing (TSCIS): A quantitative electrical technique for studying defects in dielectric stacks. , 2008, , .		76
65	The influence of elevated temperature on degradation and lifetime prediction of thin silicon-dioxide films. IEEE Transactions on Electron Devices, 2000, 47, 1514-1521.	1.6	75
66	Analytical Percolation Model for Predicting Anomalous Charge Loss in Flash Memories. IEEE Transactions on Electron Devices, 2004, 51, 1392-1400.	1.6	75
67	Analysis of the enhanced hot-electron injection in split-gate transistors useful for EEPROM applications. IEEE Transactions on Electron Devices, 1992, 39, 1150-1156.	1.6	74
68	Relation between breakdown mode and location in short-channel nMOSFETs and its impact on reliability specifications. IEEE Transactions on Device and Materials Reliability, 2001, 1, 163-169.	1.5	74
69	Analytical model for point and line tunneling in a tunnel field-effect transistor. , 2008, , .		74
70	The influence of the measurement setup on enhanced AC hot carrier degradation of MOSFETs. IEEE Transactions on Electron Devices, 1990, 37, 310-313.	1.6	73
71	Impact of single charged gate oxide defects on the performance and scaling of nanoscaled FETs. , 2012, , .		72
72	Reliability screening of high-k dielectrics based on voltage ramp stress. Microelectronics Reliability, 2007, 47, 513-517.	0.9	71

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73	Impact of MOSFET oxide breakdown on digital circuit operation and reliability. , 0, , .		70
74	New interface state density extraction method applicable to peaked and high-density distributions for Ge MOSFET development. IEEE Electron Device Letters, 2006, 27, 405-408.	2.2	69
75	Characterization of the V_{T} -instability in $\text{SiO}_2/\text{HfO}_2$ gate dielectrics. , 0, , .		68
76	Hot Hole Degradation Effects in Lateral nDMOS Transistors. IEEE Transactions on Electron Devices, 2004, 51, 1704-1710.	1.6	68
77	Charge trapping and dielectric reliability of $\text{SiO}_2/\text{Al}_2\text{O}_3$ gate stacks with TiN electrodes. IEEE Transactions on Electron Devices, 2003, 50, 1261-1269.	1.6	65
78	Understanding ferroelectric Al:HfO ₂ thin films with Si-based electrodes for 3D applications. Journal of Applied Physics, 2017, 121, .	1.1	64
79	Hole trapping and trap generation in the gate silicon dioxide. IEEE Transactions on Electron Devices, 2001, 48, 1127-1135.	1.6	63
80	Probabilistic defect occupancy model for NBTI. , 2011, , .		63
81	Toward Understanding Positive Bias Temperature Instability in Fully Recessed-Gate GaN MISFETs. IEEE Transactions on Electron Devices, 2016, 63, 1853-1860.	1.6	63
82	Degradation of tunnel-oxide floating-gate EEPROM devices and the correlation with high field-current-induced degradation of thin gate oxides. IEEE Transactions on Electron Devices, 1989, 36, 1663-1682.	1.6	62
83	Hot-carrier degradation in submicrometre MOSFETs: from uniform injection towards the real operating conditions. Semiconductor Science and Technology, 1995, 10, 1208-1220.	1.0	62
84	Vertical Ferroelectric HfO ₂ /FET based on 3-D NAND Architecture: Towards Dense Low-Power Memory. , 2018, , .		62
85	Characterization of front and back Si-SiO_2 interfaces in thick- and thin-film silicon-on-insulator MOS structures by the charge-pumping technique. IEEE Transactions on Electron Devices, 1989, 36, 1746-1750.	1.6	60
86	Analysis of Complementary RRAM Switching. IEEE Electron Device Letters, 2012, 33, 1186-1188.	2.2	60
87	Correlation between number of walls and diameter in multiwall carbon nanotubes grown by chemical vapor deposition. Carbon, 2012, 50, 1748-1752.	5.4	60
88	Constant current charge-to-breakdown: Still a valid tool to study the reliability of MOS structures?. , 1998, , .		58
89	Hot carrier degradation and time-dependent dielectric breakdown in oxides. Microelectronic Engineering, 1999, 49, 27-40.	1.1	58
90	Integration and electrical characterization of carbon nanotube via interconnects. Microelectronic Engineering, 2011, 88, 837-843.	1.1	58

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91	Microscopic origin of random telegraph noise fluctuations in aggressively scaled RRAM and its impact on read disturb variability. , 2013, , .		58
92	HIMOS-a high efficiency flash E/sup 2/PROM cell for embedded memory applications. IEEE Transactions on Electron Devices, 1993, 40, 2255-2263.	1.6	57
93	A Study of Relaxation Current in High- κ Dielectric Stacks. IEEE Transactions on Electron Devices, 2004, 51, 402-408.	1.6	57
94	Quantum Mechanical Performance Predictions of p-n-i-n Versus Pocketed Line Tunnel Field-Effect Transistors. IEEE Transactions on Electron Devices, 2013, 60, 2128-2134.	1.6	57
95	Impact of process and geometrical parameters on the electrical characteristics of vertical nanowire silicon n-TFETs. Solid-State Electronics, 2012, 72, 82-87.	0.8	56
96	Correlation of interface states/border traps and threshold voltage shift on AlGaIn/GaN metal-insulator-semiconductor high-electron-mobility transistors. Applied Physics Letters, 2015, 107, .	1.5	56
97	Reliability Study of Ferroelectric Al:HfO ₂ Thin Films for DRAM and NAND Applications. IEEE Transactions on Electron Devices, 2017, 64, 4091-4098.	1.6	56
98	Correlation between 1/fnoise and interface state density at the Fermi level in field-effect transistors. Journal of Applied Physics, 1985, 57, 4811-4813.	1.1	55
99	Impact of weak Fermi-level pinning on the correct interpretation of III-V MOS C-V and G-V characteristics. Microelectronic Engineering, 2007, 84, 2146-2149.	1.1	55
100	NBTI Lifetime Prediction and Kinetics at Operation Bias Based on Ultrafast Pulse Measurement. IEEE Transactions on Electron Devices, 2010, 57, 228-237.	1.6	55
101	Part I: Impact of Field-Induced Quantum Confinement on the Subthreshold Swing Behavior of Line TFETs. IEEE Transactions on Electron Devices, 2013, 60, 4057-4064.	1.6	55
102	Digital-circuit analysis of short-gate tunnel FETs for low-voltage applications. Semiconductor Science and Technology, 2011, 26, 085001.	1.0	54
103	Demonstration of GaN Integrated Half-Bridge With On-Chip Drivers on 200-mm Engineered Substrates. IEEE Electron Device Letters, 2019, 40, 1499-1502.	2.2	54
104	Hot-carrier effects in n-channel MOS transistors under alternating stress conditions. IEEE Electron Device Letters, 1988, 9, 232-234.	2.2	52
105	Emerging yield and reliability challenges in nanometer CMOS technologies. , 2008, , .		52
106	Reaction-dispersive proton transport model for negative bias temperature instabilities. Applied Physics Letters, 2005, 86, 093506.	1.5	51
107	Review of reliability issues in high-k/metal gate stacks. , 2008, , .		51
108	Response of a single trap to AC negative Bias Temperature stress. , 2011, , .		50

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109	Energy Distribution of Positive Charges in Gate Dielectric: Probing Technique and Impacts of Different Defects. IEEE Transactions on Electron Devices, 2013, 60, 1745-1753.	1.6	50
110	GaN-on-SOI: Monolithically Integrated All-GaN ICs for Power Conversion. , 2019, , .		50
111	MoS ₂ /MoTe ₂ Heterostructure Tunnel FETs Using Gated Schottky Contacts. Advanced Functional Materials, 2020, 30, 1905970.	7.8	50
112	Observation of Dynamic $\langle i \rangle_{TH}$ of p-GaN Gate HEMTs by Fast Sweeping Characterization. IEEE Electron Device Letters, 2020, 41, 577-580.	2.2	50
113	A Single Pulse Charge Pumping Technique for Fast Measurements of Interface States. IEEE Transactions on Electron Devices, 2011, 58, 1490-1498.	1.6	48
114	Insights into Ni-filament formation in unipolar-switching Ni/HfO ₂ /TiN resistive random access memory device. Applied Physics Letters, 2012, 100, .	1.5	48
115	Scaling CMOS: Finding the gate stack with the lowest leakage current. Solid-State Electronics, 2005, 49, 695-701.	0.8	47
116	Reliability Comparison of Triple-Gate Versus Planar SOI FETs. IEEE Transactions on Electron Devices, 2006, 53, 2351-2357.	1.6	47
117	Observation of single interface traps in submicron MOSFET's by charge pumping. IEEE Transactions on Electron Devices, 1996, 43, 940-945.	1.6	46
118	A novel hot-hole injection degradation model for lateral nDMOS transistors. , 0, , .		46
119	Emerging Yield and Reliability Challenges in Nanometer CMOS Technologies. , 2008, , .		46
120	Drive current enhancement in p-tunnel FETs by optimization of the process conditions. Solid-State Electronics, 2011, 65-66, 28-32.	0.8	46
121	Improvement of data retention in HfO ₂ /Hf 1T1R RRAM cell under low operating current. , 2013, , .		46
122	Suppression of the Backgating Effect of Enhancement-Mode p-GaN HEMTs on 200-mm GaN-on-SOI for Monolithic Integration. IEEE Electron Device Letters, 2018, 39, 999-1002.	2.2	46
123	Internal photoemission of electrons at interfaces of metals with low- ϵ insulators. Applied Physics Letters, 2006, 89, 202909.	1.5	45
124	Improvement in NBTI reliability of Si-passivated Ge/high-k/metal-gate pFETs. Microelectronic Engineering, 2009, 86, 1582-1584.	1.1	45
125	Generic learning of TDDDB applied to RRAM for improved understanding of conduction and switching mechanism through multiple filaments. , 2010, , .		45
126	InGaAs tunnel diodes for the calibration of semi-classical and quantum mechanical band-to-band tunneling models. Journal of Applied Physics, 2014, 115, .	1.1	45

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127	Comparison of Reaction-Diffusion and Atomistic Trap-Based BTI Models for Logic Gates. IEEE Transactions on Device and Materials Reliability, 2014, 14, 182-193.	1.5	45
128	Stress-Induced Positive Charge in Hf-Based Gate Dielectrics: Impact on Device Performance and a Framework for the Defect. IEEE Transactions on Electron Devices, 2008, 55, 1647-1656.	1.6	44
129	Temperature and voltage dependences of the capture and emission times of individual traps in high-k dielectrics. Microelectronic Engineering, 2011, 88, 1243-1246.	1.1	44
130	An Investigation on Border Traps in III-V MOSFETs With an In _{0.53} Ga _{0.47} As Channel. IEEE Transactions on Electron Devices, 2015, 62, 3633-3639.	1.6	44
131	One-Selector One-Resistor Cross-Point Array With Threshold Switching Selector. IEEE Transactions on Electron Devices, 2015, 62, 3250-3257.	1.6	44
132	Determination of spatial surface state density distribution in MOS and SIMOS transistors after channel hot electron injection. Electronics Letters, 1982, 18, 372.	0.5	43
133	On the field dependence of intrinsic and extrinsic time-dependent dielectric breakdown. , 1996, , .		43
134	Cost-effective cleaning and high-quality thin gate oxides. IBM Journal of Research and Development, 1999, 43, 339-350.	3.2	43
135	Hot carrier degradation and ESD in submicrometer CMOS technologies: how do they interact?. IEEE Transactions on Device and Materials Reliability, 2001, 1, 23-32.	1.5	43
136	Device and circuit-level analog performance trade-offs: a comparative study of planar bulk FETs versus FinFETs. , 0, , .		43
137	Competing Degradation Mechanisms in Short-Channel Transistors Under Channel Hot-Carrier Stress at Elevated Temperatures. IEEE Transactions on Device and Materials Reliability, 2009, 9, 454-458.	1.5	43
138	Advancing CMOS beyond the Si roadmap with Ge and III/V devices. , 2011, , .		43
139	Characterization of individual interface traps with charge pumping. Applied Physics Letters, 1996, 68, 1383-1385.	1.5	42
140	An Analysis of the NBTI-Induced Threshold Voltage Shift Evaluated by Different Techniques. IEEE Transactions on Electron Devices, 2009, 56, 1086-1093.	1.6	42
141	Channel Hot-Carrier Degradation in Short-Channel Transistors With High- k /Metal Gate Stacks. IEEE Transactions on Device and Materials Reliability, 2009, 9, 425-430.	1.5	42
142	Postcycling LRS Retention Analysis in HfO ₂ /Hf RRAM 1T1R Device. IEEE Electron Device Letters, 2013, 34, 626-628.	2.2	42
143	Implications of BTI-Induced Time-Dependent Statistics on Yield Estimation of Digital Circuits. IEEE Transactions on Electron Devices, 2014, 61, 666-673.	1.6	42
144	On the hot-carrier-induced post-stress interface trap generation in n-channel MOS transistors. IEEE Transactions on Electron Devices, 1994, 41, 413-419.	1.6	41

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145	SILC-related effects in flash E/sup 2/PROM's-Part II: Prediction of steady-state SILC-related disturb characteristics. IEEE Transactions on Electron Devices, 1998, 45, 1751-1760.	1.6	41
146	Temperature acceleration of oxide breakdown and its impact on ultra-thin gate oxide reliability. , 0, , .		41
147	Determination of capture cross sections for as-grown electron traps in HfO ₂ ~HfSiO stacks. Journal of Applied Physics, 2006, 100, 093716.	1.1	41
148	Stochastic variability of vacancy filament configuration in ultra-thin dielectric RRAM and its impact on OFF-state reliability. , 2013, , .		41
149	Endurance degradation mechanisms in TiNTa ₂ O ₅ Ta resistive random-access memory cells. Applied Physics Letters, 2015, 106, .	1.5	41
150	Statistical Analysis of the Impact of Anode Recess on the Electrical Characteristics of AlGaN/GaN Schottky Diodes With Gated Edge Termination. IEEE Transactions on Electron Devices, 2016, 63, 3451-3458.	1.6	41
151	Real V _{th} instability of pMOSFETs under practical operation conditions. , 2007, , .		40
152	Neutron-Induced Failure in Silicon IGBTs, Silicon Super-Junction and SiC MOSFETs. IEEE Transactions on Nuclear Science, 2012, 59, 866-871.	1.2	40
153	Defect-based methodology for workload-dependent circuit lifetime projections - Application to SRAM. , 2013, , .		40
154	Self-heating on bulk FinFET from 14nm down to 7nm node. , 2015, , .		40
155	A compact model for the grounded-gate nMOS behaviour under CDM ESD stress. , 0, , .		39
156	Negative bias temperature instability (NBTI) in SiO ₂ and SiON gate dielectrics understood through disorder-controlled kinetics. Microelectronic Engineering, 2005, 80, 122-125.	1.1	39
157	A study of Joule heating-induced breakdown of carbon nanotube interconnects. Nanotechnology, 2011, 22, 395202.	1.3	39
158	Statistical insight into controlled forming and forming free stacks for HfO _x RRAM. Microelectronic Engineering, 2013, 109, 177-181.	1.1	39
159	Ultrathin Metal/Amorphous-Silicon/Metal Diode for Bipolar RRAM Selector Applications. IEEE Electron Device Letters, 2014, 35, 199-201.	2.2	39
160	First demonstration of vertically stacked ferroelectric Al doped HfO ₂ devices for NAND applications. , 2017, , .		39
161	Design and analysis of new protection structures for smart power technology with controlled trigger and holding voltage. , 0, , .		38
162	Photoresistance Switching of Plasmonic Nanopores. Nano Letters, 2015, 15, 776-782.	4.5	38

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163	Oxide and interface degradation and breakdown under medium and high field injection conditions: A correlation study. <i>Microelectronic Engineering</i> , 1995, 28, 313-316.	1.1	37
164	Silicide Engineering to Boost Si Tunnel Transistor Drive Current. <i>Japanese Journal of Applied Physics</i> , 2011, 50, 04DC05.	0.8	37
165	Observation of hot-carrier-induced nFET gate-oxide breakdown in dynamically stressed CMOS circuits. , 0, , .		36
166	Analysis and modeling of a digital CMOS circuit operation and reliability after gate oxide breakdown: a case study. <i>Microelectronics Reliability</i> , 2002, 42, 555-564.	0.9	36
167	Hole-Traps in Silicon Dioxidesâ€”Part II: Generation Mechanism. <i>IEEE Transactions on Electron Devices</i> , 2004, 51, 1274-1280.	1.6	36
168	Positive Bias Temperature Instability in nMOSFETs with ultra-thin Hf-silicate gate dielectrics. <i>Microelectronic Engineering</i> , 2005, 80, 130-133.	1.1	36
169	Effects of Measurement Temperature on NBTI. <i>IEEE Electron Device Letters</i> , 2007, 28, 298-300.	2.2	36
170	A model determining optimal doping concentration and materialâ€™s band gap of tunnel field-effect transistors. <i>Applied Physics Letters</i> , 2012, 100, .	1.5	36
171	Understanding of the endurance failure in scaled HfO ₂ -based 1T1R RRAM through vacancy mobility degradation. , 2012, , .		36
172	Analysis of vertical cross-point resistive memory (VRRAM) for 3D RRAM design. , 2013, , .		36
173	Abrupt breakdown in dielectric/metal gate stacks: a potential reliability limitation?. <i>IEEE Electron Device Letters</i> , 2005, 26, 773-775.	2.2	35
174	An Assessment of the Location of As-Grown Electron Traps in $\text{HfO}_2/\text{HfSiO}$ Stacks. <i>IEEE Electron Device Letters</i> , 2006, 27, 817-820.	2.2	35
175	Electrical and reliability characterization of metal-gate/HfO ₂ /Ge FETs with Si passivation. <i>Microelectronic Engineering</i> , 2007, 84, 2067-2070.	1.1	35
176	Experimental validation of self-heating simulations and projections for transistors in deeply scaled nodes. , 2014, , .		35
177	Reliable Time Exponents for Long Term Prediction of Negative Bias Temperature Instability by Extrapolation. <i>IEEE Transactions on Electron Devices</i> , 2017, 64, 1467-1473.	1.6	35
178	Oxide and interface degradation resulting from substrate hot-hole injection in metal-oxide-semiconductor field-effect transistors at 295 and 77 K. <i>Journal of Applied Physics</i> , 1994, 75, 2073-2080.	1.1	34
179	Role of hydrogen on negative bias temperature instability in HfO ₂ -based hole channel field-effect transistors. <i>Applied Physics Letters</i> , 2004, 85, 2101-2103.	1.5	34
180	Dominant Layer for Stress-Induced Positive Charges in Hf-Based Gate Stacks. <i>IEEE Electron Device Letters</i> , 2008, 29, 1360-1363.	2.2	34

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181	Improvements of NBTI reliability in SiGe p-FETs. , 2010, , .		34
182	New Analysis Method for Time-Dependent Device-To-Device Variation Accounting for Within-Device Fluctuation. IEEE Transactions on Electron Devices, 2013, 60, 2505-2511.	1.6	34
183	Two types of neutral electron traps generated in the gate silicon dioxide. IEEE Transactions on Electron Devices, 2002, 49, 1868-1875.	1.6	33
184	Charge trapping in SiO ₂ /HfO ₂ gate dielectrics: Comparison between charge-pumping and pulsed IDâ€“VG. Microelectronic Engineering, 2004, 72, 267-272.	1.1	33
185	Properties and dynamic behavior of electron traps in HfO ₂ /SiO ₂ stacks. Microelectronic Engineering, 2005, 80, 366-369.	1.1	33
186	Degradation and breakdown of 0.9 nm EOT SiO ₂ /ALD HfO ₂ /metal gate stacks under positive constant voltage stress. , 0, , .		33
187	Correlation of single trapping and detrapping effects in drain and gate currents of nanoscaled nFETs and pFETs. , 2012, , .		33
188	Understanding the Basic Advantages of Bulk FinFETs for Sub- and Near-Threshold Logic Circuits From Device Measurements. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 439-442.	2.2	33
189	Tunneling Transistors Based on MoS ₂ /MoTe ₂ Van der Waals Heterostructures. IEEE Journal of the Electron Devices Society, 2018, 6, 1048-1055.	1.2	33
190	Investigation on Carrier Transport Through AlN Nucleation Layer From Differently Doped Si(111) Substrates. IEEE Transactions on Electron Devices, 2018, 65, 1721-1727.	1.6	33
191	Behavior of hot hole stressed SiO ₂ /Si interface at elevated temperature. Journal of Applied Physics, 1998, 83, 843-850.	1.1	32
192	A fast and simple methodology for lifetime prediction of ultra-thin oxides. , 0, , .		32
193	Electrical characteristics of 8- μ m EOT HfO ₂ /TaN low thermal-budget n-channel FETs with solid-phase epitaxially regrown junctions. IEEE Transactions on Electron Devices, 2006, 53, 1657-1668.	1.6	32
194	Identifying the Bottlenecks to the RF Performance of FinFETs. , 2010, , .		32
195	Hourglass concept for RRAM: A dynamic and statistical device model. , 2014, , .		32
196	Time dependent dielectric breakdown (TDDB) evaluation of PE-ALD SiN gate dielectrics on AlGaIn/GaN recessed gate D-mode MIS-HEMTs and E-mode MIS-FETs. , 2015, , .		32
197	Time-Dependent Breakdown Mechanisms and Reliability Improvement in Edge Terminated AlGaIn/GaN Schottky Diodes Under HTRB Tests. IEEE Electron Device Letters, 2017, 38, 371-374.	2.2	32
198	Continuing degradation of the SiO ₂ /Si interface after hot hole stress. Journal of Applied Physics, 1997, 81, 2686-2692.	1.1	31

#	ARTICLE	IF	CITATIONS
199	Ultra-thin oxide reliability: searching for the thickness scaling limit. <i>Microelectronics Reliability</i> , 2000, 40, 697-701.	0.9	31
200	Mechanism for the generation of interface state precursors. <i>Journal of Applied Physics</i> , 2000, 87, 2967-2977.	1.1	31
201	Analytical model for failure rate prediction due to anomalous charge loss of flash memories. , 0, , .		31
202	Competing hot carrier degradation mechanisms in lateral n-type DMOS transistors. , 0, , .		31
203	Gate oxide breakdown in FET devices and circuits: From nanoscale physics to system-level reliability. <i>Microelectronics Reliability</i> , 2007, 47, 559-566.	0.9	31
204	High performance aâ€GZO thinâ€film transistors with mfaâ€PVD SiO₂ as an etchâ€stopâ€layer. <i>Journal of the Society for Information Display</i> , 2014, 22, 23-28.	0.8	31
205	Current transient spectroscopy for trapping analysis on Au-free AlGaIn/GaN Schottky barrier diode. <i>Applied Physics Letters</i> , 2015, 106, 083502.	1.5	31
206	Write/erase degradation in source side injection flash EEPROM's: characterization techniques and wearout mechanisms. <i>IEEE Transactions on Electron Devices</i> , 1995, 42, 1992-1998.	1.6	30
207	Hydrogen induced positive charge generation in gate oxides. <i>Journal of Applied Physics</i> , 2001, 90, 1911-1919.	1.1	30
208	Evidence for source side injection hot carrier effects on lateral DMOS transistors. <i>Microelectronics Reliability</i> , 2004, 44, 1621-1624.	0.9	30
209	Trends and perspectives for electrical characterization and reliability assessment in advanced CMOS technologies. , 2010, , .		30
210	Superior NBTI reliability of SiGe channel pMOSFETs: Replacement gate, FinFETs, and impact of Body Bias. , 2011, , .		30
211	Carbon nanotubeâ€carbon nanotube contacts as an alternative towards low resistance horizontal interconnects. <i>Carbon</i> , 2011, 49, 4004-4012.	5.4	30
212	The relevance of deeply-scaled FET threshold voltage shifts for operation lifetimes. , 2012, , .		30
213	Dynamic ‘hour glass’ model for SET and RESET in HfO₂/RRAM. , 2012, , .		30
214	Reliability of MOL local interconnects. , 2013, , .		30
215	RTN and PBTI-induced time-dependent variability of replacement metal-gate high-k InGaAs FinFETs. , 2014, , .		30
216	Self-heating in FinFET and GAA-NW using Si, Ge and III/V channels. , 2016, , .		30

#	ARTICLE	IF	CITATIONS
217	On the Identification of Buffer Trapping for Bias-Dependent Dynamic R _{ON} of AlGaIn/GaN Schottky Barrier Diode With AlGaIn:C Back Barrier. IEEE Electron Device Letters, 2016, 37, 310-313.	2.2	30
218	A quantitative model for the conduction in oxides thermally grown from polycrystalline silicon. IEEE Transactions on Electron Devices, 1986, 33, 1028-1042.	1.6	29
219	Double snapback in SOI nMOSFETs and its application for SOI ESD protection. IEEE Electron Device Letters, 1993, 14, 326-328.	2.2	29
220	Reliability of Ultra-Thin Gate Oxide Below 3 nm in the Direct Tunneling Regime. Japanese Journal of Applied Physics, 1997, 36, 1602-1608.	0.8	29
221	Effect of bulk trap density on HfO ₂ reliability and yield. , 0, , .		29
222	Implications of progressive wear-out for lifetime extrapolation of ultra-thin (EOT ~ 1 nm) SiON films. , 0, , .		29
223	Effective work function modulation by controlled dielectric monolayer deposition. Applied Physics Letters, 2006, 89, 113505.	1.5	29
224	Channel hot-carrier degradation in pMOS and nMOS short channel transistors with high-k dielectric stack. Microelectronic Engineering, 2010, 87, 47-50.	1.1	29
225	Area scaling and voltage dependence of time-to-breakdown in magnetic tunnel junctions. Journal of Applied Physics, 2002, 91, 7712.	1.1	28
226	Matching Performance of FinFET Devices With Fin Widths Down to 10 nm. IEEE Electron Device Letters, 2009, 30, 1374-1376.	2.2	28
227	Defect Loss: A New Concept for Reliability of MOSFETs. IEEE Electron Device Letters, 2012, 33, 480-482.	2.2	28
228	Hydrogen-Induced Resistive Switching in TiN/ALD HfO ₂ /PEALD TiN RRAM Device. IEEE Electron Device Letters, 2012, 33, 483-485.	2.2	28
229	Junction Field Effect on the Retention Time for One-Transistor Floating-Body RAM. IEEE Transactions on Electron Devices, 2012, 59, 2167-2172.	1.6	28
230	Plasma doping and reduced crystalline damage for conformally doped fin field effect transistors. Applied Physics Letters, 2013, 102, .	1.5	28
231	Influence of tester, test method, and device type on CDM ESD testing. IEEE Transactions on Components and Packaging Technologies, 1995, 18, 284-294.	0.7	27
232	Zener tunneling in semiconductors under nonuniform electric fields. Journal of Applied Physics, 2010, 107, 054520.	1.1	27
233	Quantitative and predictive model of reading current variability in deeply scaled vertical poly-Si channel for 3D memories. , 2012, , .		27
234	Novel back-channel etch process flow based aIGZO TFTs for circuit and display applications on PEN foil. Journal of the Society for Information Display, 2013, 21, 369-375.	0.8	27

#	ARTICLE	IF	CITATIONS
235	Back-channel-etch amorphous indium-gallium-zinc oxide thin-film transistors: The impact of source/drain metal etch and final passivation. Japanese Journal of Applied Physics, 2014, 53, 111401.	0.8	27
236	BTI reliability of advanced gate stacks for Beyond-Silicon devices: Challenges and opportunities. , 2014, , .		27
237	Determination of energy and spatial distribution of oxide border traps in In _{0.53} Ga _{0.47} As MOS capacitors from capacitance-voltage characteristics measured at various temperatures. Microelectronics Reliability, 2014, 54, 746-754.	0.9	27
238	Characterization of time-dependent variability using 32k transistor arrays in an advanced HK/MG technology. , 2015, , .		27
239	Hot-carrier degradation behavior of N- and P-channel MOSFET's under dynamic operation conditions. IEEE Transactions on Electron Devices, 1994, 41, 1421-1428.	1.6	26
240	An analytical model for the optimization of source-side injection flash EEPROM devices. IEEE Transactions on Electron Devices, 1995, 42, 1314-1320.	1.6	26
241	A new analytic model for the description of the intrinsic oxide breakdown statistics of ultra-thin oxides. Microelectronics Reliability, 1996, 36, 1639-1642.	0.9	26
242	Degradation of oxides and oxynitrides under hot hole stress. IEEE Transactions on Electron Devices, 2000, 47, 378-386.	1.6	26
243	Photo-carrier generation as the origin of Fowler-Nordheim-induced substrate hole current in thin oxides. IEEE Transactions on Electron Devices, 2001, 48, 231-238.	1.6	26
244	A New TDDDB Reliability Prediction Methodology Accounting for Multiple SBD and Wear Out. IEEE Transactions on Electron Devices, 2009, 56, 1424-1432.	1.6	26
245	Integration of Vertical Carbon Nanotube Bundles for Interconnects. Journal of the Electrochemical Society, 2010, 157, K211.	1.3	26
246	A Comprehensive LER-Aware TDDDB Lifetime Model for Advanced Cu Interconnects. IEEE Transactions on Device and Materials Reliability, 2011, 11, 278-289.	1.5	26
247	Temperature dependence of the emission and capture times of SiON individual traps after positive bias temperature stress. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2011, 29, 01AA04.	0.6	26
248	Statistical spectroscopy of switching traps in deeply scaled vertical poly-Si channel for 3D memories. , 2013, , .		26
249	Characteristics improvement of top-gate self-aligned amorphous indium gallium zinc oxide thin-film transistors using a dual-gate control. Journal of the Society for Information Display, 2017, 25, 349-355.	0.8	26
250	Limitations on Lateral Nanowire Scaling Beyond 7-nm Node. IEEE Electron Device Letters, 2017, 38, 9-11.	2.2	26
251	Investigation of temperature acceleration of thin oxide time-to-breakdown. Microelectronic Engineering, 1999, 48, 47-50.	1.1	25
252	RF Split Capacitance-Voltage Measurements of Short-Channel and Leaky MOSFET Devices. IEEE Electron Device Letters, 2006, 27, 772-774.	2.2	25

#	ARTICLE	IF	CITATIONS
253	On the impact of the Si passivation layer thickness on the NBTI of nanoscaled Si _{0.45} Ge _{0.55} pMOSFETs. <i>Microelectronic Engineering</i> , 2011, 88, 1388-1391.	1.1	25
254	Modeling the Impact of Reset Depth on Vacancy-Induced Filament Perturbations in HfO_2 RRAM. <i>IEEE Electron Device Letters</i> , 2013, 34, 614-616.	2.2	25
255	Understanding the suppressed charge trapping in relaxed- and strained-Ge/SiO ₂ /HfO ₂ pMOSFETs and implications for the screening of alternative high-mobility substrate/dielectric CMOS gate stacks. , 2013, , .		25
256	Leakage-current reduction and improved on-state performance of Au-free AlGaIn/GaN-on-Si Schottky diode by embedding the edge terminations in the anode region. <i>Physica Status Solidi C: Current Topics in Solid State Physics</i> , 2014, 11, 862-865.	0.8	25
257	The impact of the gate dielectric quality in developing Au-free D-mode and E-mode recessed gate AlGaIn/GaN transistors on a 200mm Si substrate. , 2015, , .		25
258	Comments on "The generation and characterization of electron and hole traps created by hole injection during low gate voltage hot-carrier stressing of n-MOS transistors" [with reply]. <i>IEEE Transactions on Electron Devices</i> , 1992, 39, 458-464.	1.6	24
259	Direct and post-injection oxide and interface trap generation resulting from low-temperature hot-electron injection. <i>Journal of Applied Physics</i> , 1993, 74, 5582-5586.	1.1	24
260	Influence of gate length on ESD-performance for deep sub micron CMOS technology. , 0, , .		24
261	On the interface states generated under different stress conditions. <i>Applied Physics Letters</i> , 2001, 79, 3092-3094.	1.5	24
262	Stress polarity dependence of degradation and breakdown of SiO ₂ /high-k stacks. , 0, , .		24
263	Correlation between Stress-Induced Leakage Current (SILC) and the HfO ₂ bulk trap density in a SiO ₂ /HfO ₂ stack. , 0, , .		24
264	Reliability issues in MuGFET nanodevices. , 2008, , .		24
265	Statistical characterization of current paths in narrow poly-Si channels. , 2011, , .		24
266	Development of a Technique for Characterizing Bias Temperature Instability-Induced Device-to-Device Variation at SRAM-Relevant Conditions. <i>IEEE Transactions on Electron Devices</i> , 2014, 61, 3081-3089.	1.6	24
267	Critical analysis of the substrate hot-hole injection technique. <i>Solid-State Electronics</i> , 1994, 37, 393-399.	0.8	23
268	Grounded-gate nMOS transistor behavior under CDM ESD stress conditions. <i>IEEE Transactions on Electron Devices</i> , 1997, 44, 1972-1980.	1.6	23
269	A new degradation model and lifetime extrapolation technique for lightly doped drain nMOSFETs under hot-carrier degradation. <i>Microelectronics Reliability</i> , 2001, 41, 437-443.	0.9	23
270	Threshold voltage shifts in Si passivated (100)Ge p-channel field effect transistors: Insights from first-principles modeling. <i>Applied Physics Letters</i> , 2007, 91, 023506.	1.5	23

#	ARTICLE	IF	CITATIONS
271	A consistent model for oxide trap profiling with the Trap Spectroscopy by Charge Injection and Sensing (TSCIS) technique. Solid-State Electronics, 2010, 54, 1384-1391.	0.8	23
272	Time and workload dependent device variability in circuit simulations. , 2011, , .		23
273	Negative bias temperature instability lifetime prediction: Problems and solutions. , 2013, , .		23
274	Harnessing Plasmon-Induced Ionic Noise in Metallic Nanopores. Nano Letters, 2013, 13, 1724-1729.	4.5	23
275	Circuits and AMOLED display with self-aligned a-IGZO TFTs on polyimide foil. Journal of the Society for Information Display, 2014, 22, 509-517.	0.8	23
276	Low-temperature formation of source-drain contacts in self-aligned amorphous oxide thin-film transistors. Journal of Information Display, 2015, 16, 111-117.	2.1	23
277	On the Optimal ON/OFF Resistance Ratio for Resistive Switching Element in One-Selector One-Resistor Crosspoint Arrays. IEEE Electron Device Letters, 2015, 36, 570-572.	2.2	23
278	Uniform Strain in Heterostructure Tunnel Field-Effect Transistors. IEEE Electron Device Letters, 2016, 37, 337-340.	2.2	23
279	NBTI-Generated Defects in Nanoscaled Devices: Fast Characterization Methodology and Modeling. IEEE Transactions on Electron Devices, 2017, 64, 4011-4017.	1.6	23
280	Silicide Engineering to Boost Si Tunnel Transistor Drive Current. Japanese Journal of Applied Physics, 2011, 50, 04DC05.	0.8	23
281	A new quantitative model to predict SILC-related disturb characteristics in flash E/sup 2/PROM devices. , 0, , .		22
282	Direct measurement of the inversion charge in MOSFETs: application to mobility extraction in alternative gate dielectrics. , 0, , .		22
283	Insights on the physical mechanism behind negative bias temperature instabilities. Applied Physics Letters, 2007, 90, 043505.	1.5	22
284	Reduction of the BTI time-dependent variability in nanoscaled MOSFETs by body bias. , 2013, , .		22
285	Part II: Investigation of Subthreshold Swing in Line Tunnel FETs Using Bias Stress Measurements. IEEE Transactions on Electron Devices, 2013, 60, 4065-4072.	1.6	22
286	SiGe Channel Technology: Superior Reliability Toward Ultra-Thin EOT Devices Part II: Time-Dependent Variability in Nanoscaled Devices and Other Reliability Issues. IEEE Transactions on Electron Devices, 2013, 60, 405-412.	1.6	22
287	Reliability of High Mobility SiGe Channel MOSFETs for Future CMOS Applications. Springer Series in Advanced Microelectronics, 2014, , .	0.3	22
288	Characterization of self-heating in high-mobility Ge FinFET pMOS devices. , 2015, , .		22

#	ARTICLE	IF	CITATIONS
289	Cell Variability Impact on the One-Selector One-Resistor Cross-Point Array Performance. IEEE Transactions on Electron Devices, 2015, 62, 3490-3497.	1.6	22
290	Origins and implications of increased channel hot carrier variability in nFinFETs. , 2015, , .		22
291	Analysis of mechanisms for the enhanced degradation during AC hot carrier stress of MOSFETs. , 0, , .		21
292	The effect of externally imposed mechanical stress on the hot-carrier-induced degradation of deep-sub micron nMOSFET's. IEEE Transactions on Electron Devices, 1997, 44, 943-950.	1.6	21
293	Analysis of the kinetics for interface state generation following hole injection. Journal of Applied Physics, 2003, 93, 6107-6116.	1.1	21
294	Calibrated wafer-level HBM measurements for quasi-static and transient device analysis. , 2007, , .		21
295	Optimization of tunnel FETs: Impact of gate oxide thickness, implantation and annealing conditions. , 2010, , .		21
296	Positive and negative bias temperature instability on sub-nanometer eot high-K MOSFETs. , 2010, , .		21
297	Two-dimensional quantum mechanical modeling of band-to-band tunneling in indirect semiconductors. , 2011, , .		21
298	Recent trends in bias temperature instability. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2011, 29, 01AB01.	0.6	21
299	Suitability of high-k gate oxides for III–V devices: A PBTI study in In$_{0.53}$/Ga$_{0.47}$/As devices with Al$_{2}$/O$_{3}$. , 2014, , .		21
300	Extraction of the Random Component of Time-Dependent Variability Using Matched Pairs. IEEE Electron Device Letters, 2015, 36, 300-302.	2.2	21
301	Investigating the Current Collapse Mechanisms of p-GaN Gate HEMTs by Different Passivation Dielectrics. IEEE Transactions on Power Electronics, 2021, 36, 4927-4930.	5.4	21
302	Compact Modeling of Multidomain Ferroelectric FETs: Charge Trapping, Channel Percolation, and Nucleation-Growth Domain Dynamics. IEEE Transactions on Electron Devices, 2021, 68, 2107-2115.	1.6	21
303	Relation between hole traps and hydrogenous species in silicon dioxides. Solid-State Electronics, 2002, 46, 1839-1847.	0.8	20
304	Experimental verification of SRAM cell functionality after hard and soft gate oxide breakdowns. , 0, , .		20
305	Study of the Reliability Impact of Chlorine Precursor Residues in Thin Atomic-Layer-Deposited HfO_2 Layers. IEEE Transactions on Electron Devices, 2007, 54, 752-758.	1.6	20
306	Study of leakage mechanism and trap density in porous low-k materials. , 2010, , .		20

#	ARTICLE	IF	CITATIONS
307	Depth localization of positive charge trapped in silicon oxynitride field effect transistors after positive and negative gate bias temperature stress. Applied Physics Letters, 2011, 98, 183506.	1.5	20
308	HBM ESD Robustness of GaN-on-Si Schottky Diodes. IEEE Transactions on Device and Materials Reliability, 2012, 12, 589-598.	1.5	20
309	NBTI Reliability of SiGe and Ge Channel pMOSFETs With $\frac{\text{SiO}_2}{\text{HfO}_2}$ Dielectric Stack. IEEE Transactions on Device and Materials Reliability, 2013, 13, 497-506.	1.5	20
310	Quantum mechanical solver for confined heterostructure tunnel field-effect transistors. Journal of Applied Physics, 2014, 115, 053706.	1.1	20
311	Statistical poly-Si grain boundary model with discrete charging defects and its 2D and 3D implementation for vertical 3D NAND channels. , 2015, , .		20
312	Programming-conditions solutions towards suppression of retention tails of scaled oxide-based RRAM. , 2015, , .		20
313	RTN-based defect tracking technique: Experimentally probing the spatial and energy profile of the critical filament region and its correlation with HfO ₂ /RRAM switching operation and failure mechanism. , 2016, , .		20
314	Analysis of HBM ESD testers and specifications using a fourth-order lumped element model. Quality and Reliability Engineering International, 1994, 10, 325-334.	1.4	19
315	Statistical model for stress-induced leakage current and pre-breakdown current jumps in ultra-thin oxide layers. , 0, , .		19
316	Electrical signature of the defect associated with gate oxide breakdown. IEEE Electron Device Letters, 2006, 27, 393-395.	2.2	19
317	SILC defect generation spectroscopy in HfSiON using constant voltage stress and substrate hot electron injection. , 2008, , .		19
318	ESD On-Wafer Characterization: Is TLP Still the Right Measurement Tool?. IEEE Transactions on Instrumentation and Measurement, 2009, 58, 3418-3426.	2.4	19
319	Defect-centric perspective of time-dependent BTI variability. Microelectronics Reliability, 2012, 52, 1883-1890.	0.9	19
320	A comprehensive study of channel hot-carrier degradation in short channel MOSFETs with high-k dielectrics. Microelectronic Engineering, 2013, 103, 144-149.	1.1	19
321	Role of the Ta scavenger electrode in the excellent switching control and reliability of a scalable low-current operated TiN-Ta ₂ O ₅ /Ta RRAM device. , 2014, , .		19
322	Impact of the Substrate Orientation on CHC Reliability in n-FinFETs—Separation of the Various Contributions. IEEE Transactions on Device and Materials Reliability, 2014, 14, 52-56.	1.5	19
323	Physical origin of current collapse in Au-free AlGaIn/GaN Schottky Barrier Diodes. Microelectronics Reliability, 2014, 54, 2196-2199.	0.9	19
324	The Mechanisms of Hot-Carrier Degradation. , 1992, , 1-119.		19

#	ARTICLE	IF	CITATIONS
325	Analysis of Snapback in Soi nMOSFETs and its Use for an Soi ESD Protection Circuit. , 0, , .		18
326	Basics and applications of charge pumping in submicron MOSFETs © 1997 IEEE. Reprinted, with permission, from Proc. 1997 21st International Conference on Microelectronics, Nis, Yugoslavia, 14-17 September 1997, Vol. 2, pp. 581-589. Microelectronics Reliability, 1998, 38, 1379-1389.	0.9	18
327	Influence of well profile and gate length on the ESD performance of a fully silicided 0.25 µm CMOS technology. IEEE Transactions on Components, Packaging and Manufacturing Technology Part C Manufacturing, 1998, 21, 286-294.	0.4	18
328	Stress induced charge trapping effects in SiO ₂ /Al ₂ O ₃ gate stacks with TiN electrodes. Journal of Applied Physics, 2003, 94, 6627-6630.	1.1	18
329	Effects of detrapping on electron traps generated in gate oxides. Semiconductor Science and Technology, 2003, 18, 174-182.	1.0	18
330	Defects Generation in SiO ₂ /HfO ₂ Studied with Variable TCHARGE-TDIScharge Charge Pumping (VT2CP). , 2007, , .		18
331	Determining weak Fermi-level pinning in MOS devices by conductance and capacitance analysis and application to GaAs MOS devices. Solid-State Electronics, 2007, 51, 1101-1108.	0.8	18
332	BJT-Mode Endurance on a 1T-RAM Bulk FinFET Device. IEEE Electron Device Letters, 2010, 31, 1380-1382.	2.2	18
333	Impact of Back-Gate Bias and Device Geometry on the Total Ionizing Dose Response of 1-Transistor Floating Body RAMs. IEEE Transactions on Nuclear Science, 2012, 59, 2966-2973.	1.2	18
334	ESD in FinFET technologies: Past learning and emerging challenges. , 2013, , .		18
335	Degradation analysis of datapath logic subblocks under NBTI aging in FinFET technology. , 2014, , .		18
336	Photo-carrier generation as the origin of Fowler-Nordheim-induced substrate hole current in thin oxides. , 0, , .		17
337	On the Electrical Characterization of High-κ Dielectrics. MRS Bulletin, 2002, 27, 222-225.	1.7	17
338	Potential vulnerability of dynamic CMOS logic to soft gate oxide breakdown. IEEE Electron Device Letters, 2003, 24, 742-744.	2.2	17
339	New insights into the relation between channel hot carrier degradation and oxide breakdown short channel nMOSFETs. IEEE Electron Device Letters, 2003, 24, 278-280.	2.2	17
340	Measurement and statistical analysis of single trap current-voltage characteristics in ultrathin SiON. , 0, , .		17
341	Impact of gate materials on positive charge formation in HfO ₂ -SiO ₂ stacks. Applied Physics Letters, 2006, 89, 023507.	1.5	17
342	T-diodes - a novel plug-and-play wideband RF circuit ESD protection methodology. , 2007, , .		17

#	ARTICLE	IF	CITATIONS
343	Gate voltage and geometry dependence of the series resistance and of the carrier mobility in FinFET devices. <i>Microelectronic Engineering</i> , 2008, 85, 1728-1731.	1.1	17
344	Mobility and Dielectric Quality of 1-nm EOT HfSiON on Si(110) and (100). <i>IEEE Transactions on Electron Devices</i> , 2008, 55, 3414-3420.	1.6	17
345	Process-Dependent N/PBTI Characteristics of TiN Gate FinFETs. <i>IEEE Electron Device Letters</i> , 2012, 33, 937-939.	2.2	17
346	New Insights Into Defect Loss, Slowdown, and Device Lifetime Enhancement. <i>IEEE Transactions on Electron Devices</i> , 2013, 60, 413-419.	1.6	17
347	Perspective of tunnel-FET for future low-power technology nodes. , 2014, , .		17
348	Gated and STI defined ESD diodes in advanced bulk FinFET technologies. , 2014, , .		17
349	Non-Monte-Carlo methodology for high-sigma simulations of circuits under workload-dependent BTI degradation—Application to 6T SRAM. , 2014, , .		17
350	The defect-centric perspective of device and circuit reliabilityâ€™From gate oxide defects to circuits. <i>Solid-State Electronics</i> , 2016, 125, 52-62.	0.8	17
351	NBTI in Replacement Metal Gate SiGe core FinFETs: Impact of Ge concentration, fin width, fin rotation and interface passivation by high pressure anneals. , 2016, , .		17
352	Buffer Vertical Leakage Mechanism and Reliability of 200-mm GaN-on-SOI. <i>IEEE Transactions on Electron Devices</i> , 2019, 66, 553-560.	1.6	17
353	Trends in semiconductor memories. <i>Microelectronics Journal</i> , 1989, 20, 9-58.	1.1	16
354	A 5 V-compatible flash EEPROM cell with microsecond programming time for embedded memory applications. <i>IEEE Transactions on Components and Packaging Technologies</i> , 1994, 17, 380-389.	0.7	16
355	Accurate and robust noise-based trigger algorithm for soft breakdown detection in ultra thin oxides. , 0, , .		16
356	Characterization and modeling of transient device behavior under CDM ESD stress. <i>Journal of Electrostatics</i> , 2004, 62, 133-153.	1.0	16
357	Real-Time Investigation of Conduction Mechanism With Bias Stress in Silica-Based Intermetal Dielectrics. <i>IEEE Transactions on Device and Materials Reliability</i> , 2007, 7, 252-258.	1.5	16
358	TDDDB Reliability Prediction Based on the Statistical Analysis of Hard Breakdown Including Multiple Soft Breakdown and Wear-out. , 2007, , .		16
359	Impact of Si-thickness on interface and device properties for Si-passivated Ge pMOSFETs. , 2008, , .		16
360	Significant reduction of Positive Bias Temperature Instability in high-k/metal-gate nFETs by incorporation of rare earth metals. <i>Microelectronic Engineering</i> , 2009, 86, 1894-1896.	1.1	16

#	ARTICLE	IF	CITATIONS
361	Interface Trap Characterization of a 5.8-Å EOT p-MOSFET Using High-Frequency On-Chip Ring Oscillator Charge Pumping Technique. IEEE Transactions on Electron Devices, 2011, 58, 3342-3349.	1.6	16
362	Quantum ballistic transport in the junctionless nanowire pinch-off field effect transistor. Journal of Computational Electronics, 2011, 10, 216-221.	1.3	16
363	Impact of Individual Charged Gate-Oxide Defects on the Entire I_D - V_G Characteristic of Nanoscaled FETs. IEEE Electron Device Letters, 2012, 33, 779-781.	2.2	16
364	Improved source design for p-type tunnel field-effect transistors: Towards truly complementary logic. Applied Physics Letters, 2014, 105, .	1.5	16
365	Selector design considerations and requirements for 1 SIR RRAM crossbar array. , 2014, , .		16
366	Understanding the impact of programming pulses and electrode materials on the endurance properties of scaled Ta ₂ O ₅ RRAM cells. , 2014, , .		16
367	Energy Distribution of Positive Charges in $Al_2O_3/GeO_2/Ge$ pMOSFETs. IEEE Electron Device Letters, 2014, 35, 160-162.	2.2	16
368	Maximizing reliable performance of advanced CMOS circuits; A case study. , 2014, , .		16
369	Poly-Si heaters for ultra-fast local temperature control of on-wafer test structures. Microelectronic Engineering, 2014, 114, 47-51.	1.1	16
370	Hot carrier aging and its variation under use-bias: Kinetics, prediction, impact on Vdd and SRAM. , 2015, , .		16
371	The defect-centric perspective of device and circuit reliability; From individual defects to circuits. , 2015, , .		16
372	Impact of the Low Temperature Gate Dielectrics on Device Performance and Bias-Stress Stabilities of a-IGZO Thin-Film Transistors. ECS Journal of Solid State Science and Technology, 2015, 4, N99-N102.	0.9	16
373	Analysis of slow de-trapping phenomena after a positive gate bias on AlGaIn/GaN MIS-HEMTs with in-situ Si ₃ N ₄ /Al ₂ O ₃ bilayer gate dielectrics. Solid-State Electronics, 2015, 103, 127-130.	0.8	16
374	Latchup in bulk FinFET technology. , 2017, , .		16
375	BTI Reliability Improvement Strategies in Low Thermal Budget Gate Stacks for 3D Sequential Integration. , 2018, , .		16
376	Elements of the leakage current of high- $\hat{\mu}$ ferroelectric PZT films. Integrated Ferroelectrics, 1995, 7, 173-184.	0.3	15
377	Recommendations to further improvements of HBM ESD component level test specifications. , 0, , .		15
378	A new analytic model for the description of the intrinsic oxide breakdown statistics of ultra-thin oxides. , 0, , .		15

#	ARTICLE	IF	CITATIONS
379	Statistical model for prebreakdown current jumps and breakdown caused by single traps in magnetic tunnel junctions. <i>Journal of Applied Physics</i> , 2003, 94, 2749-2751.	1.1	15
380	Layout dependency induced deviation from Poisson area scaling in BEOL dielectric reliability. <i>Microelectronics Reliability</i> , 2005, 45, 1299-1304.	0.9	15
381	A low-cost 90nm RF-CMOS platform for record RF circuit performance. , 0, , .		15
382	RFCMOS ESD protection and reliability. , 0, , .		15
383	Ultrafast progressive breakdown associated with metal-like filament formation of a breakdown path in a HfO ₂ -TaN-TiN transistor. <i>Applied Physics Letters</i> , 2006, 88, 122907.	1.5	15
384	Impact of Nitrogen Incorporation in SiO _x /HfSiO Gate Stacks on Negative Bias Temperature Instabilities. , 2006, , .		15
385	FinFET technology for analog and RF circuits. , 2007, , .		15
386	A consistent model for the hard breakdown distribution including digital soft breakdown: the noble art of area scaling. <i>Microelectronic Engineering</i> , 2007, 84, 1925-1928.	1.1	15
387	Considerations for further scaling of metal-insulator-metal DRAM capacitors. <i>Journal of Vacuum Science and Technology B: Nanotechnology and Microelectronics</i> , 2013, 31, .	0.6	15
388	Sidewall Crystalline Orientation Effect of Post-treatments for a Replacement Metal Gate Bulk Fin Field Effect Transistor. <i>ACS Applied Materials & Interfaces</i> , 2013, 5, 8865-8868.	4.0	15
389	Comprehensive investigation of on-state stress on D-mode AlGaIn/GaN MIS-HEMTs. , 2013, , .		15
390	Understanding charge traps for optimizing Si-passivated Ge nMOSFETs. , 2016, , .		15
391	Physically unclonable function using CMOS breakdown position. , 2017, , .		15
392	Thermal stability analysis and modelling of advanced perpendicular magnetic tunnel junctions. <i>AIP Advances</i> , 2018, 8, .	0.6	15
393	Integration of 650 V GaN Power ICs on 200 mm Engineered Substrates. <i>IEEE Transactions on Semiconductor Manufacturing</i> , 2020, 33, 534-538.	1.4	15
394	On the channel-length dependence of the hot-carrier degradation of n-channel MOSFETs. <i>IEEE Electron Device Letters</i> , 1989, 10, 553-555.	2.2	14
395	A comparative study of the oxide breakdown in short-channel nmosfets and pmosfets stressed in inversion and in accumulation regimes. <i>IEEE Transactions on Device and Materials Reliability</i> , 2003, 3, 8-13.	1.5	14
396	Characterization and Optimization of Sub-32-nm FinFET Devices for ESD Applications. <i>IEEE Transactions on Electron Devices</i> , 2008, 55, 3507-3516.	1.6	14

#	ARTICLE	IF	CITATIONS
397	A DC-to-22 GHz 8.4mW compact dual-feedback wideband LNA in 90 nm digital CMOS. , 2009, , .		14
398	Novel Device Concepts for Nanotechnology: The Nanowire Pinch-Off FET and Graphene TunnelFET. ECS Transactions, 2010, 28, 15-26.	0.3	14
399	6Å EOT Si<inf>0.45</inf>Ge<inf>0.55</inf> pMOSFET with optimized reliability ($V_{DD}=1V$): Meeting the NBTI lifetime target at ultra-thin EOT. , 2010, , .		14
400	Gate Voltage Influence on the Channel Hot-Carrier Degradation of High- k -Based Devices. IEEE Transactions on Device and Materials Reliability, 2011, 11, 92-97.	1.5	14
401	Characterization of Electron Traps in Si-Capped Ge MOSFETs With $\text{HfO}_2/\text{SiO}_2$ Gate Stack. IEEE Electron Device Letters, 2012, 33, 1681-1683.	2.2	14
402	Low-power DRAM-compatible Replacement Gate High- k /Metal Gate Stacks. Solid-State Electronics, 2013, 84, 22-27.	0.8	14
403	High-drive current ($\approx 1\text{MA}/\text{cm}^2$) and highly nonlinear ($\approx 10^3$) TiN/amorphous-Silicon/TiN scalable bidirectional selector with excellent reliability and its variability impact on the 1S1R array performance. , 2014, , .		14
404	Endurance of One Transistor Floating Body RAM on UTBOX SOI. IEEE Transactions on Electron Devices, 2014, 61, 801-805.	1.6	14
405	Low-frequency noise assessment of border traps in Al_2O_3 capped DRAM peripheral MOSFETs. Semiconductor Science and Technology, 2014, 29, 115015.	1.0	14
406	A test-proven As-grown-Generation (A-G) model for predicting NBTI under use-bias. , 2015, , .		14
407	Predictive As-grown-Generation (A-G) model for BTI-induced device/circuit level variations in nanoscale technology nodes. , 2016, , .		14
408	Conduction mechanism in amorphous InGaZnO thin film transistors. Japanese Journal of Applied Physics, 2016, 55, 014301.	0.8	14
409	Band-Tails Tunneling Resolving the Theory-Experiment Discrepancy in Esaki Diodes. IEEE Journal of the Electron Devices Society, 2018, 6, 633-641.	1.2	14
410	Hole trapping during low gate bias, high drain bias hot-carrier injection in n-MOSFETs at 77 K. IEEE Transactions on Electron Devices, 1992, 39, 851-857.	1.6	13
411	Accurate and robust noise-based trigger algorithm for soft breakdown detection in ultrathin gate dielectrics. IEEE Transactions on Device and Materials Reliability, 2001, 1, 120-127.	1.5	13
412	Degradation and time dependent breakdown of stressed ferromagnetic tunnel junctions. Journal of Applied Physics, 2001, 89, 7350-7352.	1.1	13
413	Location and hardness of the oxide breakdown in short channel n- and p-MOSFETs. , 0, , .		13
414	Accurate reliability evaluation of non-uniform ultrathin oxynitride and high- k layers. , 0, , .		13

#	ARTICLE	IF	CITATIONS
415	Hole trap generation in gate dielectric during substrate hole injection. Semiconductor Science and Technology, 2004, 19, L1-L3.	1.0	13
416	Contribution of fast and slow states to Negative Bias Temperature Instabilities in HfxSi(1-x)ON/TaN based pMOSFETs. Microelectronic Engineering, 2005, 80, 134-137.	1.1	13
417	A Novel Methodology for Sensing the Breakdown Location and Its Application to the Reliability Study of Ultrathin Hf-Silicate Gate Dielectrics. IEEE Transactions on Electron Devices, 2005, 52, 1759-1765.	1.6	13
418	Threshold voltage instability of p-channel metal-oxide-semiconductor field effect transistors with hafnium based dielectrics. Applied Physics Letters, 2007, 90, 143502.	1.5	13
419	Understanding the optimization of sub-45nm FinFET devices for ESD applications. , 2007, , .		13
420	Novel, Effective and Cost-Efficient Method of Introducing Fluorine into Metal/Hf-based Gate Stack in MuGFET and Planar SOI Devices with Significant BTI Improvement. , 2007, , .		13
421	Negligible Effect of Process-Induced Strain on Intrinsic NBTI Behavior. IEEE Electron Device Letters, 2007, 28, 242-244.	2.2	13
422	Transient voltage overshoot in TLP testing â€œ Real or artifact?. Microelectronics Reliability, 2007, 47, 1016-1024.	0.9	13
423	Methodologies for sub-1nm EOT TDDDB evaluation. , 2011, , .		13
424	Fast V_{TH} Transients After the Program/Erase of Flash Memory Stacks With High- k Dielectrics. IEEE Transactions on Electron Devices, 2011, 58, 631-640.	1.6	13
425	Off-State Degradation of High-Voltage-Tolerant nLDMOS-SCR ESD Devices. IEEE Transactions on Electron Devices, 2011, 58, 2061-2071.	1.6	13
426	1/f noise analysis of replacement metal gate bulk p-type fin field effect transistor. Applied Physics Letters, 2013, 102, 073503.	1.5	13
427	Gate current random telegraph noise and single defect conduction. Microelectronic Engineering, 2013, 109, 123-125.	1.1	13
428	Toward a streamlined projection of small device bias temperature instability lifetime distributions. Journal of Vacuum Science and Technology B: Nanotechnology and Microelectronics, 2013, 31, 01A114.	0.6	13
429	Time-dependent variation: A new defect-based prediction methodology. , 2014, , .		13
430	Full-zone spectral envelope function formalism for the optimization of line and point tunnel field-effect transistors. Journal of Applied Physics, 2015, 118, .	1.1	13
431	Identify the critical regions and switching/failure mechanisms in non-filamentary RRAM (a-VMCO) by RTN and CVS techniques for memory window improvement. , 2016, , .		13
432	Interaction between hot carrier aging and PBTI degradation in nMOSFETs: Characterization, modelling and lifetime prediction. , 2017, , .		13

#	ARTICLE	IF	CITATIONS
433	On the Impact of the Gate Work-Function Metal on the Charge Trapping Component of NBTI and PBTI. IEEE Transactions on Device and Materials Reliability, 2019, 19, 268-274.	1.5	13
434	A physics-aware compact modeling framework for transistor aging in the entire bias space. , 2019, , .		13
435	Basics and applications of charge pumping in submicron MOSFET's. , 0, , .		12
436	Characterization of soft breakdown in thin oxide NMOSFETs based on the analysis of the substrate current. IEEE Transactions on Electron Devices, 2001, 48, 1109-1113.	1.6	12
437	ESD protection for a 5.5 GHz LNA in 90 nm RF CMOS — Implementation concepts, constraints and solutions. , 2004, , .		12
438	Negative bias temperature instabilities in HfSiON/TaN-based pMOSFETs. , 0, , .		12
439	A comprehensive model for breakdown mechanism in HfO/sub 2/ high-Î² gate stacks. , 0, , .		12
440	Impact of process conditions on interface and high-Î² trap density studied by variable Tcharge-Tdischarge charge pumping (VT2CP). Microelectronic Engineering, 2007, 84, 1951-1955.	1.1	12
441	Velocity and Mobility Investigation in 1-nm-EOT HfSiON on Si (110) and (100)â€”Does the Dielectric Quality Matter?. IEEE Transactions on Electron Devices, 2009, 56, 3009-3017.	1.6	12
442	Ion-implantation-based low-cost Hk/MG process for CMOS low-power application. , 2010, , .		12
443	Growth and characterization of horizontally suspended CNTs across TiN electrode gaps. Nanotechnology, 2010, 21, 245604.	1.3	12
444	Field induced quantum confinement in Indirect Semiconductors: Quantum mechanical and modified semiclassical model. , 2011, , .		12
445	Si-based tunnel field-effect transistors for low-power nano-electronics. , 2011, , .		12
446	A compact NBTI model for accurate analog integrated circuit reliability simulation. , 2011, , .		12
447	Negative Bias Temperature Instability in p-FinFETs With 45\$^{circ}\$ Substrate Rotation. IEEE Electron Device Letters, 2013, 34, 1211-1213.	2.2	12
448	Low Frequency Noise Analysis for Post-Treatment of Replacement Metal Gate. IEEE Transactions on Electron Devices, 2013, 60, 2960-2962.	1.6	12
449	Can p-channel tunnel field-effect transistors perform as good as n-channel?. Applied Physics Letters, 2014, 105, .	1.5	12
450	Hot-carrier analysis on nMOS Si FinFETs with solid source doped junction. , 2016, , .		12

#	ARTICLE	IF	CITATIONS
451	Investigation of the endurance of FE-HfO ₂ devices by means of TDDB studies. , 2018, , .		12
452	Physical Insights on Steep Slope FEFETs including Nucleation-Propagation and Charge Trapping. , 2019, , .		12
453	Single poly cell as the best choice for radiation-hard floating gate EEPROM technology. IEEE Transactions on Nuclear Science, 1993, 40, 1619-1627.	1.2	11
454	Read-disturb and endurance of SSI-flash E ² /PROM devices at high operating temperatures. IEEE Transactions on Electron Devices, 1998, 45, 2466-2474.	1.6	11
455	Modelling hot-carrier degradation of LDD NMOSFETs by using a high-resolution measurement technique. Microelectronics Reliability, 1999, 39, 785-790.	0.9	11
456	Interface state generation after hole injection. Journal of Applied Physics, 2001, 90, 328-336.	1.1	11
457	A unified hot carrier degradation model for integrated lateral and vertical nDMOS transistors. , 0, , .		11
458	Design-driven optimisation of a 90 nm RF CMOS process by use of elevated source/drain. , 0, , .		11
459	Weibull slope and voltage acceleration of ultra-thin (1.1-1.45 nm EOT) oxynitrides. Microelectronic Engineering, 2004, 72, 61-65.	1.1	11
460	Analysis and application of energy capability characterization methods in power MOSFETs. , 0, , .		11
461	ESD-RF co-design methodology for the state of the art RF-CMOS blocks. Microelectronics Reliability, 2005, 45, 255-268.	0.9	11
462	Impact of Hf content on negative bias temperature instabilities in HfSiON-based gate stacks. Applied Physics Letters, 2005, 86, 173509.	1.5	11
463	High performing 8 /spl Orang/ EOT HfO ₂ / tan low thermal-budget n-channel FETs with solid-phase epitaxially regrown (SPER) junctions. , 0, , .		11
464	Analysis of the FinFET parasitics for improved RF performances. SOI Conference, Proceedings of the IEEE International, 2007, , .	0.0	11
465	Electrical Characterization of Leaky Charge-Trapping High- κ MOS Devices Using Pulsed Q_{eff} . IEEE Electron Device Letters, 2007, 28, 436-439.	2.2	11
466	Channel Hot-Carrier degradation under static stress in short channel transistors with high-k/metal gate stacks. , 2008, , .		11
467	Reliability study of La ₂ O ₃ capped HfSiON high-permittivity n-type metal-oxide-semiconductor field-effect transistor devices with tantalum-rich electrodes. Journal of Applied Physics, 2008, 104, 044512.	1.1	11
468	Novel architecture to boost the vertical tunneling in Tunnel Field Effect Transistors. , 2011, , .		11

#	ARTICLE	IF	CITATIONS
469	Comparison of System-Level ESD Design Methodologies; Towards the Efficient and ESD Robust Design of Systems. IEEE Transactions on Device and Materials Reliability, 2013, 13, 213-222.	1.5	11
470	Key issues and techniques for characterizing time-dependent device-to-device variation of SRAM. , 2013, , ,		11
471	Advanced MOSFET variability and reliability characterization array. , 2015, , ,		11
472	Analysis of frequency dispersion in amorphous InGaZnO thin-film transistors. Journal of Information Display, 2015, 16, 31-36.	2.1	11
473	Novel Flexible and Cost-Effective Retention Assessment Method for TMO-Based RRAM. IEEE Electron Device Letters, 2016, 37, 1112-1115.	2.2	11
474	The impact of process variation and stochastic aging in nanoscale VLSI. , 2016, , ,		11
475	Probing Local Potentials inside Metallic Nanopores with SERS and Bipolar Electrochemistry. Advanced Optical Materials, 2017, 5, 1600907.	3.6	11
476	A new statistical model for fitting bimodal oxide breakdown distributions at different field conditions. Microelectronics Reliability, 1996, 36, 1651-1654.	0.9	10
477	Assessment of oxide reliability and hot carrier degradation in CMOS technology. Microelectronic Engineering, 1998, 40, 147-166.	1.1	10
478	Charge trapping in metal-ferroelectric-insulator-semiconductor structure with SrBi ₂ Ta ₂ O ₉ ·Al ₂ O ₃ ·SiO ₂ stack. Journal of Applied Physics, 2004, 96, 1614-1619.	1.1	10
479	A new breakdown failure mechanism in HfO ₂ /sub 2/ gate dielectric. , 0, , ,		10
480	Deposition of 60 nm thin Sr _{0.8} Bi _{2.2} Ta ₂ O ₉ layers for application in scaled 1T1C and 1T FeRAM devices. Microelectronic Engineering, 2005, 80, 162-165.	1.1	10
481	Explaining 'Voltage-Driven' Breakdown Statistics by Accurately Modeling Leakage Current Increase in Thin SiON and SiO ₂ /High-K Stacks. , 2006, , ,		10
482	FinFET and MOSFET preliminary comparison of gate oxide reliability. Microelectronics Reliability, 2006, 46, 1608-1611.	0.9	10
483	Postdeposition-Anneal Effect on Negative Bias Temperature Instability in HfSiON Gate Stacks. IEEE Transactions on Device and Materials Reliability, 2007, 7, 146-151.	1.5	10
484	Accurate Gate Impedance Determination on Ultraleaky MOSFETs by Fitting to a Three-Lumped-Parameter Model at Frequencies From DC to RF. IEEE Transactions on Electron Devices, 2007, 54, 1705-1712.	1.6	10
485	Correlation Between the V_{th} Adjustment of nMOSFETs With HfSiO Gate Oxide and the Energy Profile of the Bulk Trap Density. IEEE Electron Device Letters, 2010, 31, 272-274.	2.2	10
486	Switching by Ni Filaments in a HfO ₂ Matrix: A New Pathway to Improved Unipolar Switching RRAM. , 2011, , ,		10

#	ARTICLE	IF	CITATIONS
487	Dielectrophoretic assembly of suspended single-walled carbon nanotubes. <i>Microelectronic Engineering</i> , 2012, 98, 218-221.	1.1	10
488	Modeling the impact of junction angles in tunnel field-effect transistors. <i>Solid-State Electronics</i> , 2012, 69, 31-37.	0.8	10
489	On the Bipolar Resistive Switching Memory Using TiN/Hf/HfO ₂ /Si MIS Structure. <i>IEEE Electron Device Letters</i> , 2013, 34, 414-416.	2.2	10
490	System-Level ESD Protection Design Using On-Wafer Characterization and Transient Simulations. <i>IEEE Transactions on Device and Materials Reliability</i> , 2014, 14, 104-111.	1.5	10
491	Study of (correlated) trap sites in SILC, BTI and RTN in SiON and HKMG devices. , 2014, , .		10
492	Defect-centric perspective of combined BTI and RTN time-dependent variability. , 2015, , .		10
493	Medium Frequency Physical Vapor Deposited Al ₂ O ₃ and SiO ₂ as Etch-Stop-Layers for Amorphous Indium-Gallium-Zinc-Oxide Thin-Film-Transistors. <i>ECS Journal of Solid State Science and Technology</i> , 2015, 4, Q38-Q42.	0.9	10
494	Demonstration of an InGaAs gate stack with sufficient PBTI reliability by thermal budget optimization, nitridation, high-k material choice, and interface dipole. , 2016, , .		10
495	Characterization of oxide defects in InGaAs MOS gate stacks for high-mobility n-channel MOSFETs (invited). , 2017, , .		10
496	A multi-bit/cell PUF using analog breakdown positions in CMOS. , 2018, , .		10
497	On the Apparent Non-Arrhenius Temperature Dependence of Charge Trapping in III-V/High- κ MOS Stack. <i>IEEE Transactions on Electron Devices</i> , 2018, 65, 3689-3696.	1.6	10
498	Ferroelectric Control of Magnetism in Ultrathin HfO ₂ /CoPt Layers. <i>ACS Applied Materials & Interfaces</i> , 2019, 11, 34385-34393.	4.0	10
499	Integration of GaN analog building blocks on p-GaN wafers for GaN ICs. <i>Journal of Semiconductors</i> , 2021, 42, 024103.	2.0	10
500	Reliability of p-GaN Gate HEMTs in Reverse Conduction. <i>IEEE Transactions on Electron Devices</i> , 2021, 68, 645-652.	1.6	10
501	Investigation of the Impact of Hot-Carrier-Induced Interface State Generation on Carrier Mobility in nMOSFET. <i>IEEE Transactions on Electron Devices</i> , 2021, 68, 3246-3253.	1.6	10
502	Electronic voltage control of magnetic anisotropy at room temperature in high- κ SrTiO ₃ /trilayer. <i>Physical Review Materials</i> , 2020, 4, .	0.9	10
503	Investigation of the soft-write mechanism in source-side injection flash EEPROM devices. <i>IEEE Electron Device Letters</i> , 1995, 16, 181-183.	2.2	9
504	Substrate hole current origin after oxide breakdown. , 0, , .		9

#	ARTICLE	IF	CITATIONS
505	Spectroscopic identification of light emitted from defects in silicon devices. Journal of Applied Physics, 2001, 89, 249-258.	1.1	9
506	Achievements and challenges for the electrical performance of MOSFETs with high-k gate dielectrics. , 0, , .		9
507	On the trap generation rate in ultrathin SiON under Constant Voltage Stress. Microelectronic Engineering, 2005, 80, 440-443.	1.1	9
508	Trap generation and progressive wearout in thin HfSiON. , 0, , .		9
509	Characterization of dynamic SOA of power MOSFETs limited by electrothermal breakdown. , 0, , .		9
510	RF ESD protection strategies - the design and performance trade-off challenges. , 0, , .		9
511	Formation of Porous Alumina Patterns on Silicon. ECS Transactions, 2007, 3, 85-93.	0.3	9
512	New Developments in Charge Pumping Measurements on Thin Stacked Dielectrics. IEEE Transactions on Electron Devices, 2008, 55, 3184-3191.	1.6	9
513	Impact of different defects on the kinetics of negative bias temperature instability of hafnium stacks. Applied Physics Letters, 2008, 92, 013501.	1.5	9
514	An assessment of the mobility degradation induced by remote charge scattering. Applied Physics Letters, 2009, 95, 263502.	1.5	9
515	(Invited) Boosting the On-Current of Si-Based Tunnel Field-Effect Transistors. ECS Transactions, 2010, 33, 363-372.	0.3	9
516	Charged device model (CDM) ESD challenges for laterally diffused nMOS (nLDMOS) silicon controlled rectifier (SCR) devices for high-voltage applications in standard low-voltage CMOS technology. , 2010, , .		9
517	Degradation and failure analysis of copper and tungsten contacts under high fluence stress. , 2010, , .		9
518	Unexpected failure during HBM ESD stress in nanometer-scale nLDMOS-SCR devices. , 2011, , .		9
519	Circuit Design-Oriented Stochastic Piecewise Modeling of the Postbreakdown Gate Current in MOSFETs: Application to Ring Oscillators. IEEE Transactions on Device and Materials Reliability, 2012, 12, 78-85.	1.5	9
520	Time-Dependent Dielectric Breakdown on Subnanometer EOT nMOS FinFETs. IEEE Transactions on Device and Materials Reliability, 2012, 12, 166-170.	1.5	9
521	BTI reliability of ultra-thin EOT MOSFETs for sub-threshold logic. Microelectronics Reliability, 2012, 52, 1932-1935.	0.9	9
522	Analytical model for anomalous Positive Bias Temperature Instability in La-based HfO2 nFETs based on independent characterization of charging components. Microelectronic Engineering, 2013, 109, 314-317.	1.1	9

#	ARTICLE	IF	CITATIONS
523	Impact of High-Mobility Materials on the Performance of Near- and Sub-Threshold CMOS Logic Circuits. IEEE Transactions on Electron Devices, 2013, 60, 972-977.	1.6	9
524	Effect of TSV presence on FEOL yield and reliability. , 2013, , .		9
525	Characterizing grain size and defect energy distribution in vertical SONOS poly-Si channels by means of a resistive network model. , 2013, , .		9
526	Characterization of Negative-Bias Temperature Instability of Ge MOSFETs With $\frac{\text{m GeO}_2}{\text{m Al}_2\text{O}_3}$ Stack. IEEE Transactions on Electron Devices, 2014, 61, 1307-1315.	1.6	9
527	Scaling of BTI reliability in presence of time-zero variability. , 2014, , .		9
528	Characterization and simulation methodology for time-dependent variability in advanced technologies. , 2015, , .		9
529	Electric-field induced quantum broadening of the characteristic energy level of traps in semiconductors and oxides. Journal of Applied Physics, 2016, 120, .	1.1	9
530	Asymmetric plasmonic induced ionic noise in metallic nanopores. Nanoscale, 2016, 8, 12324-12329.	2.8	9
531	Full (V_{g} , V_{d}) Bias Space Modeling of Hot-Carrier Degradation in Nanowire FETs. , 2019, , .		9
532	Impact of processing and stack optimization on the reliability of perpendicular STT-MRAM. , 2017, , .		9
533	Simulation Comparison of Hot-Carrier Degradation in Nanowire, Nanosheet and Forksheet FETs. , 2022, , .		9
534	A new procedure for lifetime prediction of n-channel MOS-transistors using the charge pumping technique. , 0, , .		8
535	Post-stress interface trap generation: a new hot-carrier induced degradation phenomenon in passivated n-channel MOSFET's. , 1992, , .		8
536	Influence of post-stress effects on the dynamic hot-carrier degradation behavior of passivated n-channel MOSFET's. IEEE Electron Device Letters, 1992, 13, 357-359.	2.2	8
537	Analysis of externally imposed mechanical stress effects on the hot-carrier-induced degradation of MOSFET's. , 1994, , .		8
538	A compact model for the grounded-gate nMOS transistor behaviour under CDM ESD stress. Journal of Electrostatics, 1998, 42, 351-381.	1.0	8
539	Investigation and Comparison of the Noise in the Gate and Substrate Current after Soft-Breakdown. Japanese Journal of Applied Physics, 1999, 38, 2219-2222.	0.8	8
540	On the mechanism of electron trap generation in gate oxides. Microelectronic Engineering, 2001, 59, 89-94.	1.1	8

#	ARTICLE	IF	CITATIONS
541	Effect of the dielectric thickness and the metal deposition technique on the mobility for HfO ₂ /TaN NMOS devices. <i>Microelectronic Engineering</i> , 2005, 80, 86-89.	1.1	8
542	Geometry Dependence of 1/f Noise in n- and p-channel MuGFETs. <i>AIP Conference Proceedings</i> , 2005, , .	0.3	8
543	Relevance of the pulsed capacitance-voltage measurement technique for the optimization of SrBi ₂ Ta ₂ O ₉ /high-k stack combination to be used in FeFET devices. <i>Microelectronic Engineering</i> , 2006, 83, 2564-2569.	1.1	8
544	H ² Isotopic Effect on Negative Bias Temperature Instabilities in SiO _x •HfSiON•TaN Gate Stacks. <i>Electrochemical and Solid-State Letters</i> , 2006, 9, G10.	2.2	8
545	Failure Defects Observed in Post-Breakdown High-κ/Metal Gate Stack Mosfet. , 2006, , .		8
546	Reliability of Strained-Si Devices With Post-Oxide-Deposition Strain Introduction. <i>IEEE Transactions on Electron Devices</i> , 2008, 55, 3432-3441.	1.6	8
547	Applicability of Charge Pumping on Germanium MOSFETs. <i>IEEE Electron Device Letters</i> , 2008, 29, 1364-1366.	2.2	8
548	Process-induced positive charges in Hf-based gate stacks. <i>Journal of Applied Physics</i> , 2008, 103, 014507.	1.1	8
549	Anomalous positive-bias temperature instability of high-κ/metal gate devices with Dy ₂ O ₃ capping. <i>Applied Physics Letters</i> , 2008, 93, 053506.	1.5	8
550	Investigating ESD sensitivity in electrostatic SiGe MEMS. <i>Journal of Micromechanics and Microengineering</i> , 2010, 20, 055005.	1.5	8
551	On-chip circuit for massively parallel BTI characterization. , 2011, , .		8
552	ALD of Al ₂ O ₃ for Carbon Nanotube vertical interconnect and its impact on the electrical properties. <i>Materials Research Society Symposia Proceedings</i> , 2011, 1283, 1.	0.1	8
553	Modeling and tuning the filament properties in RRAM metal oxide stacks for optimized stable cycling. , 2012, , .		8
554	Buried Silicon-Germanium pMOSFETs: Experimental Analysis in VLSI Logic Circuits Under Aggressive Voltage Scaling. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2012, 20, 1487-1495.	2.1	8
555	Hf Cap Thickness Dependence in Bipolar-Switching TiN/HfO ₂ /HfTiN RRAM Device. <i>ECS Transactions</i> , 2013, 50, 3-9.	0.3	8
556	A Simulation Study on Process Sensitivity of a Line Tunnel Field-Effect Transistor. <i>IEEE Transactions on Electron Devices</i> , 2013, 60, 1019-1027.	1.6	8
557	Reliability in gate first and gate last ultra-thin-EOT gate stacks assessed with CV-eMSM BTI characterization. , 2013, , .		8
558	NBTI Aging on 32-Bit Adders in the Downscaling Planar FET Technology Nodes. , 2014, , .		8

#	ARTICLE	IF	CITATIONS
559	Design and simulation of on-chip circuits for parallel characterization of ultrascaled transistors for BTI reliability. , 2014, , .		8
560	A single device based voltage step stress (VSS) technique for fast reliability screening. , 2014, , .		8
561	Four point probe ramped voltage stress as an efficient method to understand breakdown of STT-MRAM MgO tunnel junctions. , 2015, , .		8
562	Doped Gd-O Based RRAM for Embedded Application. , 2016, , .		8
563	Perpendicular magnetic anisotropy of CoPt bilayers on ALD HfO ₂ . Journal of Applied Physics, 2016, 120, .	1.1	8
564	Statistical investigation of the impact of program history and oxide-metal interface on OxRRAM retention. , 2016, , .		8
565	New understanding of dielectric breakdown in advanced FinFET devices " physical, electrical, statistical and multiphysics study. , 2016, , .		8
566	Stack optimization of oxide-based RRAM for fast write speed ($\approx 1 \mu\text{s}$) at low operating current ($< 10 \text{ Tj ETQq0,0,0 rgBT /Overlock 1}$)	0.8	8
567	Modeling of graphene for interconnect applications. , 2016, , .		8
568	Impact of Hot Carrier Aging on Random Telegraph Noise and Within a Device Fluctuation. IEEE Journal of the Electron Devices Society, 2016, 4, 15-21.	1.2	8
569	Perpendicular magnetic anisotropy of CoFeBTa bilayers on ALD HfO ₂ . AIP Advances, 2017, 7, 055933.	0.6	8
570	Towards optimal ESD diodes in next generation bulk FinFET and GAA NW technology nodes. , 2017, , .		8
571	Large Variation in Temperature Dependence of Band-to-Band Tunneling Current in Tunnel Devices. IEEE Electron Device Letters, 2019, 40, 1864-1867.	2.2	8
572	Programming mode dependent degradation of tunnel oxide floating gate devices. , 1987, , .		7
573	Performance and reliability aspects of FOND: a new deep submicron CMOS device concept. IEEE Transactions on Electron Devices, 1996, 43, 1407-1415.	1.6	7
574	A reliability study of titanium silicide lines using micro-Raman spectroscopy and emission microscopy. Microelectronics Reliability, 1997, 37, 1591-1594.	0.9	7
575	Consistent model for short-channel nMOSFET post-hard-breakdown characteristics. , 0, , .		7
576	Origin of substrate hole current after gate oxide breakdown. Journal of Applied Physics, 2002, 91, 2155-2160.	1.1	7

#	ARTICLE	IF	CITATIONS
577	Understanding nMOSFET Characteristics after Soft Breakdown and Their Dependence on the Breakdown Location. , 2002, , .		7
578	ESD circuit model based protection network optimisation for extended-voltage NMOS drivers. Microelectronics Reliability, 2005, 45, 1430-1435.	0.9	7
579	Breakdown-induced thermochemical reactions in HfO ₂ high- κ /polycrystalline silicon gate stacks. Applied Physics Letters, 2005, 87, 242907.	1.5	7
580	Moisture Related Low-K Dielectric Reliability Before and After Thermal Annealing. , 2007, , .		7
581	Investigation of Bias-Temperature Instability in work-function-tuned high- κ /metal-gate stacks. Journal of Vacuum Science & Technology B, 2009, 27, 459.	1.3	7
582	Electrical-Based ESD Characterization of Ultrathin-Body SOI MOSFETs. IEEE Transactions on Device and Materials Reliability, 2010, 10, 130-141.	1.5	7
583	On the recoverable and permanent components of Hot Carrier and NBTI in Si pMOSFETs and their implications in Si _{0.45} Ge _{0.55} pMOSFETs. , 2011, , .		7
584	Advanced PBTI reliability with 0.69nm EOT GdHfO gate dielectric. Solid-State Electronics, 2011, 63, 5-7.	0.8	7
585	Growth Mechanism of a Hybrid Structure Consisting of a Graphite Layer on Top of Vertical Carbon Nanotubes. Journal of Nanomaterials, 2012, 2012, 1-10.	1.5	7
586	Origin of wide retention distribution in 1T Floating Body RAM. , 2012, , .		7
587	Interface States Beyond Band Gap and Their Impact on Charge Carrier Mobility in MOSFETs. IEEE Transactions on Electron Devices, 2012, 59, 783-790.	1.6	7
588	Split pocket p-n-i-n tunnel field-effect transistors. , 2013, , .		7
589	Spectroscopic study of polysilicon traps by means of fast capacitance transients. Journal of Vacuum Science and Technology B: Nanotechnology and Microelectronics, 2013, 31, 01A110.	0.6	7
590	Use of SSTA Tools for Evaluating BTI Impact on Combinational Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 280-285.	2.1	7
591	Smart-array for pipelined BTI characterization. , 2015, , .		7
592	Comparative experimental analysis of time-dependent variability using a transistor test array. , 2016, , .		7
593	Semi-empirical interconnect resistance model for advanced technology nodes: A model apt for materials selection based upon test line resistance measurements. , 2016, , .		7
594	The Influence of Gate Bias on the Anneal of Hot-Carrier Degradation. , 2020, , .		7

#	ARTICLE	IF	CITATIONS
595	RF/High-Speed I/O ESD Protection: Co-optimizing Strategy Between BEOL Capacitance and HBM Immunity in Advanced CMOS Process. IEEE Transactions on Electron Devices, 2020, 67, 2752-2759.	1.6	7
596	Impact of ambient temperature on the switching of voltage-controlled perpendicular magnetic tunnel junction. Applied Physics Letters, 2021, 118, .	1.5	7
597	Modeling of Repeated FET Hot-Carrier Stress and Anneal Cycles Using Siâ€H Bond Dissociation/Passivation Energy Distributions. IEEE Transactions on Electron Devices, 2021, 68, 1454-1460.	1.6	7
598	Evaluation of channel hot carrier effects in n-MOS transistors at 77 K with the charge pumping technique. Applied Surface Science, 1987, 30, 313-318.	3.1	6
599	Understanding of the hot carrier degradation behaviour of MOSFET's by means of the charge pumping technique. Applied Surface Science, 1989, 39, 523-534.	3.1	6
600	A model study of the hot-carrier problem in LDD and overlapped LDD MOSFETs. Microelectronic Engineering, 1995, 28, 285-288.	1.1	6
601	Impact of tunnel-oxide nitridation on endurance and read-disturb characteristics of Flash E2PROM devices. Microelectronic Engineering, 1997, 36, 301-304.	1.1	6
602	Non-uniform triggering of gg-nMOS investigated by combined emission microscopy and transmission line pulsing. Microelectronics Reliability, 1999, 39, 1551-1561.	0.9	6
603	Evaluation procedure for fast and realistic assessment of plasma charging damage in thin oxides. , 0, , .		6
604	Snapback circuit model for cascoded NMOS ESD over-voltage protection structures. , 0, , .		6
605	Dynamic substrate resistance snapback triggering of ESD protection devices. , 0, , .		6
606	Impact of gate-oxide breakdown of varying hardness on narrow and wide nFET's. , 0, , .		6
607	Hot carrier degradation on n-channel HfSiON MOSFETs: effects on the device performance and lifetime. , 0, , .		6
608	Impact of copper contacts on CMOS front-end yield and reliability. , 2006, , .		6
609	Faster ESD device characterization with wafer-level HBM. , 2007, , .		6
610	Nitrogen Incorporation in HfSiO(N)/TaN Gate Stacks: Impact on Performances and NBTI. IEEE Electron Device Letters, 2007, 28, 613-615.	2.2	6
611	Performance assessment of (110) p-FET high-Îµ/MG: is it mobility or series resistance limited?. Microelectronic Engineering, 2007, 84, 2058-2062.	1.1	6
612	Mobility extraction using RFCV for 80nm MOSFET with 1nm EOT HfSiON/TiN. Microelectronic Engineering, 2007, 84, 1878-1881.	1.1	6

#	ARTICLE	IF	CITATIONS
613	Charge pumping spectroscopy: HfSiON defect study after substrate hot electron injection. Microelectronic Engineering, 2007, 84, 1943-1946.	1.1	6
614	Tunnel Field-Effect Transistors for Future Low-Power Nano-Electronics. ECS Transactions, 2009, 25, 455-462.	0.3	6
615	Resolving fast V_{TH} transients after program/erase of flash memory stacks and their relation to electron and hole defects. , 2009, , .		6
616	Evidence of a new degradation mechanism in high-k dielectrics at elevated temperatures. Reliability Physics Symposium, 2009 IEEE International, 2009, , .	0.0	6
617	Hot hole induced damage in 1T-FBRAM on bulk FinFET. , 2011, , .		6
618	Impact of halo implant on the hot carrier reliability of germanium p-channel metal-oxide-semiconductor field-effect transistors. Journal of Vacuum Science and Technology B: Nanotechnology and Microelectronics, 2011, 29, 01A804.	0.6	6
619	Impact of process variability on the radiation-induced soft error of nanometer-scale srams in hold and read conditions. , 2011, , .		6
620	Trends and Challenges in Si and Hetero-Junction Tunnel Field Effect Transistors. ECS Transactions, 2011, 35, 15-26.	0.3	6
621	Scaled X-bar TiN/HfO ₂ /TiN RRAM cells processed with optimized plasma enhanced atomic layer deposition (PEALD) for TiN electrode. Microelectronic Engineering, 2013, 112, 92-96.	1.1	6
622	Towards CMOS-compatible single-walled carbon nanotube resonators. Microelectronic Engineering, 2013, 107, 219-222.	1.1	6
623	Quantifying the Aggregation Factor in Carbon Nanotube Dispersions by Absorption Spectroscopy. Journal of Nanoscience, 2014, 2014, 1-13.	2.6	6
624	Comparative study of source-drain contact metals for amorphous InGaZnO thin-film transistors. Journal of the Society for Information Display, 2014, 22, 310-315.	0.8	6
625	Local CDM ESD Protection Circuits for Cross-Power Domains in 3D IC Applications. IEEE Transactions on Device and Materials Reliability, 2014, 14, 781-783.	1.5	6
626	Performance and reliability of high-mobility Si _{0.55} Ge _{0.45} p-channel FinFETs based on epitaxial cladding of Si Fins. , 2014, , .		6
627	ESD characterization of gate-all-around (GAA) Si nanowire devices. , 2015, , .		6
628	Investigation of constant voltage off-state stress on Au-free AlGaIn/GaN Schottky barrier diodes. Japanese Journal of Applied Physics, 2015, 54, 04DF07.	0.8	6
629	ESD diodes in a bulk Si gate-all-around vertically stacked horizontal nanowire technology. , 2016, , .		6
630	Positive bias temperature instability evaluation in fully recessed gate GaN MIS-FETs. , 2016, , .		6

#	ARTICLE	IF	CITATIONS
631	Non-uniform strain in lattice-mismatched heterostructure tunnel field-effect transistors. , 2016, , .		6
632	BTI reliability of InGaAs nMOS gate-stack: On the impact of shallow and deep defect bands on the operating voltage range of III-V technology. , 2017, , .		6
633	Statistical assessment of the full $V_{G\&D}$ degradation space using dedicated device arrays. , 2017, , .		6
634	ANALYSIS OF HOT CARRIER DEGRADATION IN AC STRESSED N-CHANNEL MOS TRANSISTORS USING THE CHARGE PUMPING TECHNIQUE. Journal De Physique Colloque, 1988, 49, C4-651-C4-655.	0.2	6
635	On the different time dependence of interface trap generation and charge trapping during hot carrier degradation in CMOS. Microelectronic Engineering, 1992, 19, 465-468.	1.1	5
636	On the hot hole induced post-stress interface trap generation in MOSFET's. , 1996, , .		5
637	Simulation study for the CDM ESD behaviour of the grounded-gate nmos. Microelectronics Reliability, 1996, 36, 1739-1742.	0.9	5
638	Geometric current component in charge-pumping measurements. , 0, , .		5
639	Analysis of Iddq failures by spectral photon emission microscopy. Microelectronics Reliability, 1998, 38, 877-882.	0.9	5
640	Novel level-identifying circuit for flash multilevel memories. IEEE Journal of Solid-State Circuits, 1998, 33, 1090-1095.	3.5	5
641	Hot carrier degradation and ESD in submicron CMOS technologies: how do they interact?. , 0, , .		5
642	Anomalously weak antenna ratio dependence of plasma process-induced damage. , 0, , .		5
643	Plasma charging damage issues in copper single and dual damascene, oxide and low-k dielectric interconnects. , 0, , .		5
644	Explanation of nMOSFET substrate current after hard gate oxide breakdown. Microelectronic Engineering, 2001, 59, 155-160.	1.1	5
645	Influence of gate length on ESD-performance for deep submicron CMOS technology. Microelectronics Reliability, 2001, 41, 375-383.	0.9	5
646	Strong correlation between dielectric reliability and charge trapping in SiO_2/Al_2O_3 gate stacks with TiN electrodes. , 0, , .		5
647	Significance of the failure criterion on transmission line pulse testing. Microelectronics Reliability, 2002, 42, 901-907.	0.9	5
648	Impact of charging on breakdown in deep trench isolation structures [parasitic MOSFET example]. , 0, , .		5

#	ARTICLE	IF	CITATIONS
649	Impact of Band Structure on Charge Trapping in Thin $\text{SiO}_2/\text{Al}_2\text{O}_3/\text{poly-Si}$ Gate Stacks. IEEE Electron Device Letters, 2004, 25, 320-322.	2.2	5
650	A comprehensive model to accurately calculate the gate capacitance and the leakage from DC to 100 MHz for ultra thin dielectrics. , 2006, , .		5
651	Implementation of 6kV ESD Protection for a 17GHz LNA in 130nm SiGeC BiCMOS. , 2006, , .		5
652	Substrate injection induced ultrafast degradation in $\text{HfO}_2/\text{TaN}/\text{TiN}$ gate stack MOSFET. , 2006, , .		5
653	Nucleation and Growth Study of Nickel Nanoparticles on Silicon.. ECS Transactions, 2006, 2, 409-416.	0.3	5
654	A Novel Method for Guard Ring Efficiency Assessment and its Applications for ESD Protection Design and Optimization. , 2007, , .		5
655	Toward Understanding the Wide Distribution of Time Scales in Negative Bias Temperature Instability. ECS Transactions, 2007, 6, 265-281.	0.3	5
656	Hydrogen induced positive charge in Hf-based dielectrics. Microelectronic Engineering, 2007, 84, 2354-2357.	1.1	5
657	Dielectric quality and reliability of FUSI/HfSiON devices with process induced strain. Microelectronic Engineering, 2007, 84, 1906-1909.	1.1	5
658	High- κ Metal Gate MOSFETs: Impact of Extrinsic Process Condition on the Gate-Stack Quality – A Mobility Study. IEEE Transactions on Electron Devices, 2007, 54, 497-503.	1.6	5
659	Detailed analysis of charge pumping and I_d/V_g hysteresis for profiling traps in $\text{SiO}_2/\text{HfSiO(N)}$. Microelectronic Engineering, 2010, 87, 2614-2619.	1.1	5
660	Advanced ESD power clamp design for SOI FinFET CMOS technology. , 2010, , .		5
661	Fully CMOS BEOL compatible HfO_2/TiN RRAM cell, with low (~ 0.3 nA) program current, strong retention and high scalability, using an optimized plasma enhanced atomic layer deposition (PEALD) process for TiN electrode. , 2011, , .		5
662	Carbon nanotube interconnects: Electrical characterization of 150 nm CNT contacts with Cu damascene top contact. , 2011, , .		5
663	Reliability of low current filamentary HfO_2 RRAM discussed in the framework of the hourglass SET/RESET model. , 2012, , .		5
664	Trap-Assisted Tunneling in Vertical Si and SiGe Hetero-Tunnel-FETs. , 2012, , .		5
665	Analysis of the effect of cell parameters on the maximum RRAM array size considering both read and write. , 2012, , .		5
666	BTI reliability of high-mobility channel devices: SiGe, Ge and InGaAs. , 2014, , .		5

#	ARTICLE	IF	CITATIONS
667	Improved Channel Hot-Carrier Reliability in $\text{p}^+\text{n}^+\text{-FinFETs}$ With Replacement Metal Gate by a Nitrogen Postdeposition Anneal Process. IEEE Transactions on Device and Materials Reliability, 2014, 14, 408-412.	1.5	5
668	Stability evaluation of Au-free Ohmic contacts on AlGaIn/GaN HEMTs under a constant current stress. Microelectronics Reliability, 2014, 54, 2232-2236.	0.9	5
669	VFTLP characteristics of ESD protection diodes in advanced bulk FinFET technology. , 2015, , .		5
670	Voltage acceleration and pulse dependence of barrier breakdown in MgO based magnetic tunnel junctions. , 2016, , .		5
671	Modeling of Edge Scattering in Graphene Interconnects. IEEE Electron Device Letters, 2018, 39, 1085-1088.	2.2	5
672	Signature of Ballistic Band-Tail Tunneling Current in Tunnel FET. IEEE Transactions on Electron Devices, 2020, 67, 3486-3491.	1.6	5
673	Extensive assessment of the charge-trapping kinetics in InGaAs MOS gate-stacks for the demonstration of improved BTI reliability. Microelectronics Reliability, 2020, 115, 113996.	0.9	5
674	Understanding the memory window in 1T-FeFET memories: a depolarization field perspective. , 2021, , .		5
675	ESD HBM Discharge Model in RF GaN-on-Si (MIS)HEMTs. IEEE Transactions on Electron Devices, 2022, 69, 2180-2187.	1.6	5
676	Hot carrier degradation in MOSFETs in the temperature range of 77â€³300 K. Quality and Reliability Engineering International, 1991, 7, 307-322.	1.4	4
677	Justifications for reducing HBM and MM ESD qualification test time. Microelectronics Reliability, 1996, 36, 1715-1718.	0.9	4
678	The effect of plasma damage and different annealing ambients on the generation of latent interface states. , 0, , .		4
679	Relation between hydrogen and the generation of interface state precursors. Microelectronic Engineering, 1999, 48, 135-138.	1.1	4
680	Negative Bias Temperature Instabilities in $\text{SiO}_2/\text{HfO}_2$ -Based Hole Channel FETs. Journal of the Electrochemical Society, 2004, 151, F288.	1.3	4
681	Advanced modelling and parameter extraction of the MOSFET ESD breakdown triggering in the 90nm CMOS node technologies. , 2004, , .		4
682	Test circuits for fast and reliable assessment of CDM robustness of I/O stages. Microelectronics Reliability, 2005, 45, 269-277.	0.9	4
683	A fast and flexible thermal simulation tool validated on smart power devices. , 0, , .		4
684	Interface characterization of Si-passivated HfO_2 germanium capacitors using DLTS measurements. Materials Science in Semiconductor Processing, 2006, 9, 749-752.	1.9	4

#	ARTICLE	IF	CITATIONS
685	MOSFET ESD Breakdown Modeling and Parameter Extraction in Advanced CMOS Technologies. IEEE Transactions on Electron Devices, 2006, 53, 2108-2117.	1.6	4
686	Interface Trap Characterization and Fermi Level Pinning in Si-Passivated Ge/HfO ₂ Capacitors. ECS Transactions, 2006, 1, 27-32.	0.3	4
687	NBTI Study on PMOS Devices with TiN/HfO ₂ Gate Stack and Process Induced Strain. ECS Transactions, 2006, 3, 253-261.	0.3	4
688	Physics of Flash Memories. , 0, , 129-177.		4
689	Challenges in Reliability Assessment of Advanced CMOS Technologies. , 2007, , .		4
690	Negative bias temperature instabilities in HfSiO(N)-based MOSFETs: Electrical characterization and modeling. Microelectronics Reliability, 2007, 47, 880-889.	0.9	4
691	Negative bias temperature instability on Si-passivated Ge-interface. , 2008, , .		4
692	An equivalent circuit model for the recovery component of BTI. , 2008, , .		4
693	Electron energy dependence of defect generation in high-k gate stacks. Journal of Applied Physics, 2008, 103, 064503.	1.1	4
694	Mechanical response of electrostatic actuators under ESD stress. , 2009, , .		4
695	New insights into the wide ID range channel hot-carrier degradation in high-k based devices. Reliability Physics Symposium, 2009 IEEE International, 2009, , .	0.0	4
696	Positive and negative bias temperature instability in La ₂ O ₃ and Al ₂ O ₃ capped high-k MOSFETs. , 2009, , .		4
697	Integration of Vertical Carbon Nanotube Bundles for Interconnects. ECS Transactions, 2009, 19, 11-24.	0.3	4
698	Channel Hot-Carrier degradation in short channel devices with high-k/metal gate stacks. , 2009, , .		4
699	Impact of design factors and environment on the ESD sensitivity of MEMS micromirrors. Microelectronics Reliability, 2010, 50, 1383-1387.	0.9	4
700	Interface/Bulk Trap Recovery After Submelt Laser Anneal and the Impact to NBTI Reliability. IEEE Electron Device Letters, 2010, 31, 606-608.	2.2	4
701	Electrical results of vertical Si N-Tunnel FETs. , 2011, , .		4
702	Challenges for introducing Ge and III/V devices into CMOS technologies. , 2012, , .		4

#	ARTICLE	IF	CITATIONS
703	Impact of Duty Factor, Stress Stimuli, and Gate Drive Strength on Gate Delay Degradation with an Atomistic Trap-Based BTI Model. , 2012, , .		4
704	Superior reliability and reduced Time-Dependent variability in high-mobility SiGe channel pMOSFETs for VLSI logic applications. , 2012, , .		4
705	Bias-temperature instability of Si and Si(Ge)-channel sub-1nm EOT p-MOS devices: Challenges and solutions. , 2013, , .		4
706	Impact of Al$_2$O$_3$ position on performances and reliability in high-k metal gated DRAM periphery transistors. , 2013, , .		4
707	NBTI of Ge pMOSFETs: Understanding defects and enabling lifetime prediction. , 2014, , .		4
708	Energy distribution of positive charges in high-k dielectric. Microelectronics Reliability, 2014, 54, 2329-2333.	0.9	4
709	Impact of Buffer Layers on the Self-Aligned Top-Gate aIGZO TFT Characteristics. Digest of Technical Papers SID International Symposium, 2015, 46, 1139-1142.	0.1	4
710	Impact of source/drain contacts formation of self-aligned amorphous aIGZO TFTs on their negative bias illumination stress stabilities. Journal of the Society for Information Display, 2015, 23, 397-402.	0.8	4
711	AC NBTI of Ge pMOSFETs: Impact of energy alternating defects on lifetime prediction. , 2015, , .		4
712	Low-current operation of novel Gd₂O₃-based RRAM cells with large memory window. Physica Status Solidi (A) Applications and Materials Science, 2016, 213, 320-324.	0.8	4
713	Process Options Impact on ESD Diode Performance in Bulk FinFET Technology. IEEE Transactions on Electron Devices, 2016, 63, 3424-3431.	1.6	4
714	Fundamental study of the apparent voltage-dependence of NBTI kinetics by constant electric field stress in Si and SiGe devices. , 2016, , .		4
715	Leakage and trapping characteristics in Au-free AlGaIn/GaN Schottky barrier diodes fabricated on Cd-doped buffer layers. Physica Status Solidi (A) Applications and Materials Science, 2016, 213, 1229-1235.	0.8	4
716	vTLP characteristics of ESD diodes in bulk si gate-all-around vertically stacked horizontal nanowire technology. , 2017, , .		4
717	Impact of operating temperature on the electrical and magnetic properties of the bottom-pinned perpendicular magnetic tunnel junctions. Applied Physics Letters, 2018, 113, .	1.5	4
718	Phonon-assisted tunneling in direct-bandgap semiconductors. Journal of Applied Physics, 2019, 125, .	1.1	4
719	Study of precessional switching speed control in voltage-controlled perpendicular magnetic tunnel junction. AIP Advances, 2020, 10, .	0.6	4
720	Drive Current Improvement in Si Tunnel Field Effect Transistors by means of Silicide Engineering. , 2010, , .		4

#	ARTICLE	IF	CITATIONS
721	ESD Failures of GaN-on-Si D-Mode AlGaIn/GaN MIS-HEMT and HEMT Devices for 5G Telecommunications. , 2021, , .		4
722	Hot-Carrier Degradation During Dynamic Stress. , 1992, , 250-310.		3
723	An analytical model for the optimization of high injection MOS Flash E2PROM devices. Microelectronic Engineering, 1992, 19, 257-260.	1.1	3
724	Modification and application of an emission microscope for continuous wavelength spectroscopy. Microelectronics Reliability, 1997, 37, 1595-1598.	0.9	3
725	ESD protection methodology for deep-sub-micron CMOS. Microelectronics Reliability, 1998, 38, 997-1007.	0.9	3
726	Electrical characterisation of high-k materials prepared by atomic layer CVD. , 0, , .		3
727	Generation of mobile hydrogenous ions in gate oxide and their potential applications. Electronics Letters, 2001, 37, 716.	0.5	3
728	ISSUES, ACHIEVEMENTS AND CHALLENGES TOWARDS INTEGRATION OF HIGH-k DIELECTRICS. International Journal of High Speed Electronics and Systems, 2002, 12, 295-304.	0.3	3
729	High frequency characterization and modelling of the parasitic RC performance of two terminal ESD CMOS protection devices. Microelectronics Reliability, 2003, 43, 1011-1020.	0.9	3
730	Scaling of high-k dielectrics towards sub-1nm EOT. , 0, , .		3
731	Degradation and breakdown of plasma oxidized magnetic tunnel junctions: Single trap creation in Al/sub 2/O/sub 3/ tunnel barriers. IEEE Transactions on Magnetics, 2003, 39, 2815-2817.	1.2	3
732	Electrical Properties of Al[sub 2]O[sub 3]/ZrO[sub 2]/Al[sub 2]O[sub 3] Gate Stack in p-Substrate Metal Oxide Semiconductor Devices. Journal of the Electrochemical Society, 2003, 150, G307.	1.3	3
733	Multilevel Transmission Line Pulse (MTLP) tester. , 2004, , .		3
734	HfO2/spacer-interface breakdown in HfO2 high- \hat{t} /poly-silicon gate stacks. Microelectronic Engineering, 2005, 80, 370-373.	1.1	3
735	Barrier Integrity Effect on Leakage Mechanism and Dielectric Reliability of Copper/OSG Interconnects. Materials Research Society Symposia Proceedings, 2005, 863, B4.4-1.	0.1	3
736	Polarity dependence of bias temperature instabilities in Hf/sub (x)Si/sub (1-x)ON/TaN gate stacks. , 0, , .		3
737	Reliability issues in advanced High k/metal gate stacks for 45 nm CMOS applications. , 2006, , .		3
738	Influence of different deposition conditions of top and bottom electrode on the reliability of Sr0.8Bi2.2Ta2O9 ferroelectric capacitors. Solid-State Electronics, 2006, 50, 1227-1234.	0.8	3

#	ARTICLE	IF	CITATIONS
739	IMPACT OF HIGH- ϵ PROPERTIES ON MOSFET ELECTRICAL CHARACTERISTICS. , 2006, , 97-108.		3
740	Plasma ash modulation of TDDDB thermal activation energy in damascene SiOC:H. Semiconductor Science and Technology, 2007, 22, 320-325.	1.0	3
741	Advanced electrical characterization toward (sub) 1nm EOT HfSiON $\hat{\Delta}$; hole trapping in PFET and L-dependent effects. , 2007, , .		3
742	Impact of Strain on ESD Robustness of FinFET Devices. , 2008, , .		3
743	On the activation and passivation of precursors for process-induced positive charges in Hf-dielectric stacks. Journal of Applied Physics, 2009, 105, 054505.	1.1	3
744	Impact of nitridation on recoverable and permanent negative bias temperature instability degradation in high-k/metal-gate p-type metal oxide semiconductor field effect transistors. Journal of Vacuum Science & Technology B, 2009, 27, 463.	1.3	3
745	Zener tunnelling in graphene based semiconductors $\hat{\Delta}$ the $k\hat{\Delta}$ -p method. Journal of Physics: Conference Series, 2009, 193, 012111.	0.3	3
746	Methodology for Design Optimization of SOI FinFET Grounded-Gate NMOS Devices. IEEE Transactions on Device and Materials Reliability, 2010, 10, 338-346.	1.5	3
747	Neutron-induced failure in super-junction, IGBT, and SiC power devices. , 2011, , .		3
748	Study of nitrogen impact on VFB $\hat{\Delta}$ “EOT roll-off by varying interfacial SiO ₂ thickness. Solid-State Electronics, 2011, 62, 67-71.	0.8	3
749	Effect of interface states on 1T-FBRAM cell retention. , 2012, , .		3
750	Improved NBTI reliability with sub-1-nanometer EOT ZrO ₂ gate dielectric compared with HfO ₂ . IEEE Electron Device Letters, 2013, 34, 593-595.	2.2	3
751	(Invited) Reliability of SiGe Channel MOS. ECS Transactions, 2013, 50, 177-195.	0.3	3
752	Guidelines for reducing NBTI based on its correlation with effective work function studied by CV-BTI on high-k first MOS capacitors with slant-etched SiO ₂ . , 2014, , .		3
753	Channel Hot Carrier Degradation and Self-Heating Effects in FinFETs. , 2015, , 287-307.		3
754	The relationship between border traps characterized by AC admittance and BTI in III-V MOS devices. , 2015, , .		3
755	Bias Temperature Instability (BTI) in high-mobility channel devices with high-k dielectric stacks: SiGe, Ge, and InGaAs. MRS Advances, 2016, 1, 3329-3340.	0.5	3
756	A fully-integrated method for RTN parameter extraction. , 2017, , .		3

#	ARTICLE	IF	CITATIONS
757	From planar to vertical capacitors: A step towards ferroelectric V-FeFET integration. , 2017, , .		3
758	Distribution Function Based Simulations of Hot-Carrier Degradation in Nanowire FETs. , 2018, , .		3
759	Built-In Sheet Charge As an Alternative to Dopant Pockets in Tunnel Field-Effect Transistors`. IEEE Journal of the Electron Devices Society, 2018, 6, 658-663.	1.2	3
760	Effects of Back-Gate Bias on the Mobility and Reliability of Junction-Less FDSOI Transistors for 3-D Sequential Integration. IEEE Transactions on Electron Devices, 2021, 68, 464-470.	1.6	3
761	Impact of Sub-Åµm Wafer Thinning on Latch-up Risk in STCO Scaling Era. , 2021, , .		3
762	The high injection MOS cell: a novel 5V-only flash EEPROM concept with a 1½s programming time. Microelectronic Engineering, 1991, 15, 617-620.	1.1	2
763	Simulation of enhanced injection split gate flash EEPROM device programming. Microelectronic Engineering, 1992, 18, 253-258.	1.1	2
764	A 5v/3.3v-compatible Flash E/sup 2/PROM Cell With A 400ns/70½m Programming Time For Embedded Memory Applications. , 0, , .		2
765	Write/erase degradation and disturb effects in source-side injection flash eeprom devices. Quality and Reliability Engineering International, 1995, 11, 239-246.	1.4	2
766	Study of the hot-carrier degradation performance of 0.35-½m fully overlapped LDD devices. Microelectronic Engineering, 1995, 28, 265-268.	1.1	2
767	Multi-level charge storage in source-side injection flash EEPROM. , 0, , .		2
768	High-temperature reliability behavior of SSI-flash E/sup 2/PROM devices. , 0, , .		2
769	A high resolution method for measuring hot carrier degradation in matched transistor pairs. Microelectronics Reliability, 1997, 37, 1533-1536.	0.9	2
770	A reliability study of titanium silicide lines using micro-Raman spectroscopy and emission microscopy. , 1998, , .		2
771	Impact of temperature and breakdown statistics on reliability predictions for ultrathin oxides. Materials Research Society Symposia Proceedings, 1999, 592, 295.	0.1	2
772	Measurement Technique, Oxide Thickness and Area Dependence of Soft-Breakdown. Materials Research Society Symposia Proceedings, 1999, 592, 335.	0.1	2
773	Hydrogen induced and plasma charging enhanced positive charge generation in gate oxides. , 0, , .		2
774	Dependence of energy distributions of interface states on stress conditions. Microelectronic Engineering, 2001, 59, 95-99.	1.1	2

#	ARTICLE	IF	CITATIONS
775	Characterization of charge trapping in $\text{SiO}_2/\text{HfO}_2$ dielectrics. , 0, , .		2
776	Enhanced ESD protection robustness of a lateral NPN structure in the advanced CMOS. , 0, , .		2
777	Modeling and simulation for ESD protection circuit design and optimization. , 2004, , .		2
778	Experimental analysis of a Ge-HfO ₂ /sub 2/-TaN gate stack with a large amount of interface states. , 0, , .		2
779	The Impact of Ultra Thin ALD TiN Metal Gate on Low Frequency Noise of CMOS Transistors. AIP Conference Proceedings, 2007, , .	0.3	2
780	Addressing Key Concerns for Implementation of Ni FUSI into Manufacturing for 45/32 nm CMOS. , 2007, , .		2
781	Characterization and modeling of diodes in Sub-45 nm CMOS technologies under HBM stress conditions. , 2007, , .		2
782	Inductor-based ESD protection under CDM-like ESD stress conditions for RF applications. , 2008, , .		2
783	Understanding and prediction of EWF modulation induced by various dopants in the gate stack for a gate-first integration scheme. , 2008, , .		2
784	Growth and Integration of High-Density CNT for BEOL Interconnects. Materials Research Society Symposia Proceedings, 2008, 1079, 1.	0.1	2
785	Perspectives of (sub-) 32nm CMOS for Analog/RF and mm-wave Applications. , 2008, , .		2
786	Circuit-design oriented modelling of the recovery BTI component and post-BD gate currents. , 2009, , .		2
787	A CMOS circuit for evaluating the NBTI over a wide frequency range. Microelectronics Reliability, 2009, 49, 885-891.	0.9	2
788	Defect profiling in the $\text{SiO}_2/\text{Al}/\text{SiO}_2/\text{Si}$ interface using Variable Temperature Charge Pumping (VT-ACP). , 2009, , .		2
789	Simulation of the hot-carrier degradation in short channel transistors with high-K dielectric. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2010, 23, 315-323.	1.2	2
790	Shaping the future of nanoelectronics beyond the Si roadmap with new materials and devices. Proceedings of SPIE, 2010, , .	0.8	2
791	Effect of anodic interface layers on the unipolar switching of HfO_2 -based resistive RAM. , 2010, , .		2
792	Effects of gate process on NBTI characteristics of TiN gate FinFET. , 2012, , .		2

#	ARTICLE	IF	CITATIONS
793	Low-power DRAM-compatible Replacement Gate High-k/Metal Gate stacks. , 2012, , .		2
794	Assessing reliability of nano-scaled CMOS technologies one defect at a time. , 2012, , .		2
795	Modeling of Charge-Trapping/Detrapping-Induced Voltage Instability in High- ϵ Gate Dielectrics. IEEE Transactions on Device and Materials Reliability, 2012, 12, 152-157.	1.5	2
796	On the rseries extraction techniques for sub-22nm CMOS finfet and SiGe technologies. , 2012, , .		2
797	Influence of InGaP and AlGaAs Schottky Layers on ESD Robustness in GaAs pHEMTs. IEEE Electron Device Letters, 2012, 33, 1252-1254.	2.2	2
798	Superior reliability of high mobility (Si)Ge channel pMOSFETs. Microelectronic Engineering, 2013, 109, 250-256.	1.1	2
799	Quasi-3D method: Time-efficient TCAD and mixed-mode simulations on finFET technologies. , 2013, , .		2
800	Impact of duty factor, stress stimuli, gate and drive strength on gate delay degradation with an atomistic trap-based BTI model. Microprocessors and Microsystems, 2013, 37, 792-800.	1.8	2
801	Degradation Mechanisms. Springer Series in Advanced Microelectronics, 2014, , 19-66.	0.3	2
802	Improvement on CDM ESD robustness of high-voltage tolerant nLDMOS SCR devices by using differential doped gate. , 2014, , .		2
803	Impact of etch stop layer on negative bias illumination stress of amorphous Indium Gallium Zinc Oxide transistors. , 2014, , .		2
804	15-band spectral envelope function formalism applied to broken gap tunnel field-effect transistors. , 2015, , .		2
805	Impact of time-dependent variability on the yield and performance of 6T SRAM cells in an advanced HK/MG technology. , 2015, , .		2
806	Will Chips of the Future Learn How to Feel Pain and Cure Themselves?. IEEE Design and Test, 2017, 34, 80-87.	1.1	2
807	Tunneling transistors based on MoS ₂ /MoTe ₂ Van der Waals heterostructures. , 2017, , .		2
808	ESD characterisation of a-IGZO TFTs on Si and foil substrates. , 2017, , .		2
809	Impact of calibrated band-tails on the subthreshold swing of pocketed TFETs. , 2018, , .		2
810	Accelerated Capture and Emission (ACE) Measurement Pattern for Efficient BTI Characterization and Modeling. , 2019, , .		2

#	ARTICLE	IF	CITATIONS
811	Improved PBTI Reliability in Junction-Less FET Fabricated at Low Thermal Budget for 3-D Sequential Integration. IEEE Transactions on Device and Materials Reliability, 2019, 19, 262-267.	1.5	2
812	The properties, effect and extraction of localized defect profiles from degraded FET characteristics. , 2021, , .		2
813	Physics-based device aging modelling framework for accurate circuit reliability assessment. , 2021, , .		2
814	Tunnel barrier properties of stressed ferromagnetic tunnel junctions. Electronics Letters, 2001, 37, 356.	0.5	2
815	Hole trapping and hot-hole induced interface trap generation in MOSFET's at different temperatures. Microelectronic Engineering, 1992, 19, 477-480.	1.1	1
816	HIMOS: an attractive flash EEPROM cell for embedded memory applications. Microelectronics Journal, 1993, 24, 190-194.	1.1	1
817	The ESD protection mechanisms and the related failure modes and mechanisms observed in SOI snapback nMOSFET's. Microelectronics Reliability, 1995, 35, 555-566.	0.9	1
818	Generation and annealing of hot hole induced interface states. Microelectronic Engineering, 1997, 36, 227-230.	1.1	1
819	Generation of hole traps in silicon dioxides. , 0, , .		1
820	Statistical aspects of the degradation of LDD nMOSFETs. Microelectronics Reliability, 2002, 42, 1409-1413.	0.9	1
821	A CAD assisted design and optimisation methodology for over-voltage ESD protection circuits. Microelectronics Reliability, 2004, 44, 1885-1890.	0.9	1
822	Modeling of energy capability of power devices with copper layer integration. , 2005, , .		1
823	On the Recovery of Simulated Plasma Process Induced Damage in High- ϵ_r Dielectrics. , 2006, , .		1
824	Bias Stress Induced Conduction Mechanism Evolution in Silica Based Inter-Metal Dielectrics. Integrated Reliability Workshop Final Report, 2009 IRW '09 IEEE International, 2006, , .	0.0	1
825	Correlation between trench depth and TDDB thermal activation energy in single damascene Cu/SiOC:H. Microelectronic Engineering, 2006, 83, 2179-2183.	1.1	1
826	Impact of defects on the high- ϵ_r /MG stack: The electrical characterization challenge. Materials Science in Semiconductor Processing, 2006, 9, 880-884.	1.9	1
827	Implementation of plug-and-play ESD protection in 5.5GHz 90nm RF CMOS LNAs "Concepts, constraints and solutions. Microelectronics Reliability, 2006, 46, 702-712.	0.9	1
828	Reliability Prediction of Direct Tunneling RAM with SiON and HfSiON Tunnel Dielectrics Based on Transistor Leakage Current Measurements. , 2006, , .		1

#	ARTICLE	IF	CITATIONS
829	Thermal recovery from stress-induced high- $\hat{\epsilon}$ dielectric film degradation. Journal of Applied Physics, 2007, 101, 044515.	1.1	1
830	High-k Characterization by RFCV. ECS Transactions, 2007, 11, 363-376.	0.3	1
831	A Step Towards a Better Understanding of Silicon Passivated (100)Ge p-Channel Devices. ECS Transactions, 2007, 6, 53-63.	0.3	1
832	Electrical Characterization of Advanced Gate Dielectrics. , 0, , 371-435.		1
833	ESD protection for sub-45 nm MugFET technology. , 2007, , .		1
834	Proof-of-Concept Structure for Investigation of Successive Soft Gate Oxide Breakdowns in Two Dimensions. , 2007, , .		1
835	Line width dependent mobility in high-k a comparative performance study between FUSI and TiN. , 2007, , .		1
836	On the Interaction Between Inter-Metal Dielectric Reliability and Electromigration Stress. , 2007, , .		1
837	Anomalous positive-bias temperature instability of high- ϵ /metal gate nMOSFET devices with Dy ₂ O ₃ capping. , 2008, , .		1
838	Teaching nanoscience across scientific and geographical borders â€“ A European Master programme in nanoscience and nanotechnology. Journal of Physics: Conference Series, 2008, 100, 032002.	0.3	1
839	Processing impact on the reliability of single metal dual dielectric (SMDD) gate stacks. , 2009, , .		1
840	The role of nitrogen in HfSiON defect passivation. Reliability Physics Symposium, 2009 IEEE International, 2009, , .	0.0	1
841	Trapping in 1nm EOT high-k / MG. ECS Transactions, 2009, 16, 77-84.	0.3	1
842	Interpretation of PBTI/ TDDB predicted lifetime based on trap characterization by TSCIS in V _{th} -adjusted transistors. , 2010, , .		1
843	Experimental analysis of buried SiGe pMOSFETs from the perspective of aggressive voltage scaling. , 2011, , .		1
844	Positive bias temperature instabilities on sub-nanometer EOT FinFETs. Microelectronics Reliability, 2011, 51, 1521-1524.	0.9	1
845	Total ionizing dose effects on ultra thin buried oxide floating body memories. , 2012, , .		1
846	Design and fabrication of SiGe MEMS structures with high intrinsic ESD robustness. , 2012, , .		1

#	ARTICLE	IF	CITATIONS
847	Towards understanding hole traps and NBTI of Ge/GeO ₂ /Al ₂ O ₃ structure. Microelectronic Engineering, 2013, 109, 43-45.	1.1	1
848	ESD characterization of diodes and ggMOS in Germanium FinFET technologies. , 2015, , .		1
849	ESD protection diodes in optical interposer technology. , 2015, , .		1
850	Engineering of a TiNAl<inf>2</inf></inf></inf>O<inf>3</inf></inf>(Hf, operation at low current. , 2015, , .		1
851	NBTI in Si<inf>0.55</inf>Ge<inf>0.45</inf> cladding p-FinFETs: Porting the superior reliability from planar to 3D architectures. , 2015, , .		1
852	ESD characterization of planar InGaAs devices. , 2015, , .		1
853	Bidirectional NPN ESD protection in silicon photonics technology. , 2016, , .		1
854	ESD ballasting of Ge FinFET ggNMOS devices. , 2017, , .		1
855	Self-consistent procedure including envelope function normalization for full-zone Schrödinger-Poisson problems with transmitting boundary conditions. Journal of Applied Physics, 2018, 124, 204501.	1.1	1
856	Impact of slow and fast oxide traps on In<inf>0.53</inf>Ga<inf>0.47</inf>As device operation studied using CET maps. , 2018, , .		1
857	Process-Induced Power-Performance Variability in Sub-5-nm III-V Tunnel FETs. IEEE Transactions on Electron Devices, 2019, 66, 2802-2808.	1.6	1
858	Monolithically integrated GaN power ICs designed using the MIT virtual source GaNFET (MVSG) compact model for enhancement-mode p-GaN gate power HEMTs, logic transistors and resistors. , 2019, , .		1
859	ESD HBM Discharge Model in RF GaN-on-Si (MIS)HEMTs. , 2021, , .		1
860	Wafer-Level Aging of InGaAs/GaAs Nano-Ridge p-i-n Diodes Monolithically Integrated on Silicon. , 2022, , .		1
861	The Influence of Mechanical Stress on Hot-Carrier Degradation in Mosfet'S. Materials Research Society Symposia Proceedings, 1993, 308, 349.	0.1	0
862	The Influence of Mechanical Stress on Hot-Carrier Degradation in Mosfet's. Materials Research Society Symposia Proceedings, 1993, 309, 281.	0.1	0
863	Voltage variant source side injection for multilevel charge storage in flash EEPROM. IEEE Transactions on Components and Packaging Technologies, 1997, 20, 196-202.	0.7	0
864	Reduction of plasma process-induced damage during gate poly etching by using a SiO ₂ /hard mask. , 0, , .		0

#	ARTICLE	IF	CITATIONS
865	Analysing Antenna Ratio Dependence of Plasma Charging Damage with Weibull Breakdown Statistics. , 2000, , .		0
866	Relation between hole traps and non-reactive hydrogen-induced positive charges. Microelectronic Engineering, 2001, 59, 67-72.	1.1	0
867	Identification of Critical Parameters for Plasma Process-Induced Damage in 130 and 100 nm CMOS Technologies. , 2002, , .		0
868	Modeling pFET currents after soft breakdown at different gate locations. Microelectronic Engineering, 2004, 72, 125-129.	1.1	0
869	Breakdown and hot carrier injection in deep trench isolation structures. Solid-State Electronics, 2005, 49, 1370-1375.	0.8	0
870	Comprehensive study of postprocessed copper heat sinks on smart power drivers for thermal SOA improvement. , 0, , .		0
871	Performance of Direct Tunneling Floating Gate Memory with Medium- $\hat{\epsilon}$ Dielectrics for Embedded-Random-Access Memory Applications. Japanese Journal of Applied Physics, 2006, 45, 3170-3175.	0.8	0
872	On the Recovery of Simulated Plasma Process Induced Damage in High- $\hat{\epsilon}$ Dielectrics. , 2006, , .		0
873	On the Recovery of Simulated Plasma Process Induced Damage in High- $\hat{\epsilon}$ Dielectrics. , 0, , .		0
874	Instability and Defects in Gate Dielectric: Similarity and Differences Between Hf-Stacks and SiO ₂ . ECS Transactions, 2007, 11, 219-233.	0.3	0
875	NBTI reliability of Ni FUSI/HfSiON gates: Effect of silicide phase. Microelectronics Reliability, 2007, 47, 505-507.	0.9	0
876	Boosting the on-current of silicon nanowire tunnel-FETs. , 2008, , .		0
877	High Mobility Channel Materials and Novel Devices for Scaling of Nanoelectronics beyond the Si Roadmap. Materials Research Society Symposia Proceedings, 2009, 1194, 49.	0.1	0
878	Quantification of metal oxide semiconductor field effect transistor device reliability with low-V _t lanthanum-incorporated high permittivity dielectrics. Journal of Applied Physics, 2009, 106, .	1.1	0
879	Understanding and Importance of Defects in Advanced Materials. ECS Transactions, 2009, 18, 651-658.	0.3	0
880	CARBonCHIP: Carbon Nanotubes Technology on Silicon Integrated Circuits; Some Key Results. ECS Transactions, 2009, 25, 63-71.	0.3	0
881	A plug-and-play wideband RF circuit ESD protection methodology: T-diodes. Microelectronics Reliability, 2009, 49, 1440-1446.	0.9	0
882	Profiling Different Kinds of Generated Defects at Elevated Temperature in Both SiO ₂ and High-k Dielectrics. Materials Research Society Symposia Proceedings, 2010, 1252, 8.	0.1	0

#	ARTICLE	IF	CITATIONS
883	ESD protection for wideband RF CMOS LNAs. , 2010, , .		0
884	The impact of junction angle on tunnel FETs. , 2011, , .		0
885	Recent trends in CMOS reliability: From individual traps to circuit simulations. , 2011, , .		0
886	Reliability test methodology for MEMS and MOEMS under electrical overstress and electrostatic discharge stress. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2012, 11, 021204-1.	1.0	0
887	HfSiO Bulk Trap Density Controls the Initial V_{th} in nMOSFETs. IEEE Transactions on Device and Materials Reliability, 2012, 12, 323-334.	1.5	0
888	Low-frequency noise assessment of the transport mechanisms in SiGe channel bulk FinFETs. , 2012, , .		0
889	(Late) Reliability and performance considerations for NMOSFET pass gates in FPGA applications. , 2013, , .		0
890	Paper No 19.3: Back-Channel Etch Process Flow for aIGZO TFTs. Digest of Technical Papers SID International Symposium, 2013, 44, 285-288.	0.1	0
891	Corrections to "Quantum Mechanical Performance Predictions of p-n-i-n Versus Pocketed Line Tunnel Field-Effect Transistors" [Jul 13 2128-2134]. IEEE Transactions on Electron Devices, 2013, 60, 3605-3605.	1.6	0
892	Comparison of NBTI aging on adder architectures and ring oscillators in the downscaling technology nodes. Microprocessors and Microsystems, 2015, 39, 1039-1051.	1.8	0
893	Oxygen chemical potential profile optimization for fast low current ($< 10^{-4}$ A) resistive switching in oxide-based RRAM. , 2016, , .		0
894	Impact of AlGaN barrier recess on the DC and dynamic characteristics of AlGaN/GaN schottky barrier diodes with gated edge termination. , 2016, , .		0
895	vtTLP characteristics of ESD devices in Si gate-all-around (GAA) nanowires. , 2016, , .		0
896	Calibration of the high-doping induced ballistic band-tails tunneling current with $\ln(0.53)$, $\ln(0.47)$, $\ln(0.47)$ As Esaki diodes. , 2017, , .		0
897	Self-consistent 30-band simulation approach for (non-)uniformly strained confined heterostructure tunnel field-effect transistors. , 2017, , .		0
898	Trap-Aware Compact Modeling and Power-Performance Assessment of III-V Tunnel FET. , 2018, , .		0
899	On the Impact of the Gate Metal Work-Function on the Charge Trapping Component of BTI. , 2018, , .		0
900	Improved PBTI reliability in junction-less nFET fabricated at low thermal budget for 3D Sequential Integration. , 2018, , .		0

#	ARTICLE	IF	CITATIONS
901	Channel Hot Carriers and Other Reliability Mechanisms. Springer Series in Advanced Microelectronics, 2014, , 161-182.	0.3	0
902	Negative Bias Temperature Instability in Nanoscale Devices. Springer Series in Advanced Microelectronics, 2014, , 131-160.	0.3	0
903	Negative Bias Temperature Instability in (Si)Ge pMOSFETs. Springer Series in Advanced Microelectronics, 2014, , 99-129.	0.3	0
904	LaSiO ₂ - and Al ₂ O ₃ -Inserted Low-Temperature Gate-Stacks for Improved BTI Reliability in 3-D Sequential Integration. IEEE Transactions on Electron Devices, 2022, , 1-7.	1.6	0