Thambipillai Srikanthan

List of Publications by Year
in descending order

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100 papers	917 citations	858243 12 h-index	620720 26 g-index
100 all docs	100 docs citations	100 times ranked	609 citing authors

#	Article	IF	Citations
1	Reconfiguration algorithms for synchronous communication on switch based degradable arrays. Parallel Computing, 2022, 111, 102901.	1.3	0
2	Road-network aware Dynamic Workload Balancing Technique for Real-time Route Generation in On-Demand Public Transit. , 2021, , .		0
3	Cluster-First, Route-Second Heuristic for EV Scheduling in On-Demand Public Transit. , 2019, , .		1
4	Algorithms for Replica Placement and Update in Tree Network. Computer Journal, 2018, 61, 273-287.	1.5	1
5	Enhanced low-complexity pruning for corner detection. Journal of Real-Time Image Processing, 2016, 12, 197-213.	2.2	12
6	Exploiting Configuration Dependencies for Rapid Area-efficient Customization of Soft-core Processors. , 2016, , .		4
7	Memory-access aware work-load distribution for peak-temperature reduction of 3D multi-core embedded systems. , 2015, , .		1
8	Efficient VLSI Architecture for Decimation-in-Time Fast Fourier Transform of Real-Valued Data. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2836-2845.	3.5	26
9	KnapSim - Run-time efficient hardware-software partitioning technique for FPGAs. , 2015, , .		4
10	Leakage-aware intra-task dynamic voltage scaling technique for energy reduction in real-time embedded systems. , 2015, , .		0
11	Algorithmic aspects of graph reduction for hardware/software partitioning. Journal of Supercomputing, 2015, 71, 2251-2274.	2.4	10
12	Critical-path optimization for efficient hardware realization of lifting and flipping DWTs. , 2015, , .		5
13	Fast Replica Placement and Update Strategies in Tree Networks. , 2015, , .		1
14	IP-Enabled C/C++ Based High Level Synthesis: A Step towards Better Designer Productivity and Design Performance. International Journal of Reconfigurable Computing, 2014, 2014, 1-17.	0.2	0
15	Architecture and Application-Aware Management of Complexity of Mapping Multiplication to FPGA DSP Blocks in High Level Synthesis. International Journal of Reconfigurable Computing, 2014, 2014, 1-14.	0.2	0
16	CONSTRUCTING LOW-TEMPERATURE SUB-ARRAYS ON RECONFIGURABLE VLSI ARRAYS. Journal of Circuits, Systems and Computers, 2014, 23, 1450067.	1.0	2
17	EXTENDED COMPATIBILITY PATH BASED HARDWARE BINDING: AN ADAPTIVE ALGORITHM FOR HIGH LEVEL SYNTHESIS OF AREA-TIME EFFICIENT DESIGNS. Journal of Circuits, Systems and Computers, 2014, 23, 1450131.	1.0	0
18	Exploiting FPGA-Aware Merging of Custom Instructions for Runtime Reconfiguration. ACM Transactions on Reconfigurable Technology and Systems, 2014, 7, 1-15.	1.9	1

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19	Rapid evaluation of custom instruction selection approaches with FPGA estimation. Transactions on Embedded Computing Systems, 2014, 13, 1-29.	2.1	0
20	Area-delay efficient architecture for MP algorithm using reconfigurable inner-product circuits. , 2014, , .		7
21	Method for accuracy assessment of aggregated freeway traffic data. IET Intelligent Transport Systems, 2014, 8, 407-414.	1.7	2
22	Constructing Sub-Arrays with ShortInterconnects from Degradable VLSI Arrays. IEEE Transactions on Parallel and Distributed Systems, 2014, 25, 929-938.	4.0	26
23	Parallel reconfiguration algorithms for mesh-connected processor arrays. Journal of Supercomputing, 2014, 69, 610-628.	2.4	5
24	Algorithmic Aspects for Bi-Objective Multiple-Choice Hardware/Software Partitioning. , 2014, , .		3
25	CADSE: communication aware design space exploration for efficient run-time MPSoC management. Frontiers of Computer Science, 2013, 7, 416-430.	1.6	1
26	Preprocessing technique for accelerating reconfiguration of degradable VLSI arrays. , 2013, , .		0
27	FPGA-aware techniques for rapid generation of profitable custom instructions. Microprocessors and Microsystems, 2013, 37, 259-269.	1.8	6
28	Modelling communication overhead for accessing local memories in hardware accelerators. , 2013, , .		5
29	Accelerating throughput-aware runtime mapping for heterogeneous MPSoCs. ACM Transactions on Design Automation of Electronic Systems, 2013, 18, 1-29.	1.9	122
30	Iris Recognition Using Stable Dark Features. Journal of Computers, 2013, 8, .	0.4	0
31	Dataflow graph partitioning for high level synthesis. , 2012, , .		4
32	Custom instructions with local memory elements without expensive DMA transfers. , 2012, , .		4
33	Reconfiguration Algorithms for Degradable VLSI Arrays with Switch Faults. , 2012, , .		1
34	Area-time estimation of C-based functions for design space exploration. , 2012, , .		1
35	Psychoacoustic Model Compensation for Robust Speaker Verification in Environmental Noise. IEEE Transactions on Audio Speech and Language Processing, 2012, 20, 945-953.	3.8	10
36	A Low-Complexity Speaker-and-Word Recognition Application for Resource-Constrained Devices. , 2011, , .		4

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37	Reconfiguration algorithm for low temperature sub-array on VLSI/WSI arrays with faults. , 2011, , .		0
38	Communication-Aware Design Space Exploration for Efficient Run-Time MPSoC Management. , 2011, , .		0
39	Run-Time Computation and Communication Aware Mapping Heuristic for NoC-Based Heterogeneous MPSoC Platforms. , 2011, , .		13
40	Instruction set customization for area-constrained FPGA designs. , 2011, , .		3
41	Automatic Compilation of C Applications for FPGA-Based Hardware Acceleration. , 2011, , .		0
42	A Design Space Exploration Methodology for Application Specific MPSoC Design. , 2011, , .		2
43	Hybrid non-preemptive/cooperative multitasking on NoC based manycore systems. , 2011, , .		0
44	Algorithm for Time-dependent Shortest Safe Path on Transportation Networks. Procedia Computer Science, 2011, 4, 958-966.	1.2	11
45	A hybrid strategy for mapping multiple throughput-constrained applications on MPSoCs. , 2011, , .		34
46	Computation and communication aware run-time mapping for NoC-based MPSoC platforms. , 2011, , .		16
47	A scalable strategy for runtime resource management on NoC based manycore systems. , 2011, , .		6
48	Accelerating UNISIM-Based Cycle-Level Microarchitectural Simulations on Multicore Platforms. ACM Transactions on Design Automation of Electronic Systems, 2011, 16, 1-25.	1.9	0
49	A Modular Simulator Framework for Network-on-Chip Based Manycore Chips Using UNISIM. Lecture Notes in Computer Science, 2011, , 234-253.	1.0	2
50	Fast evaluation-based algorithm for fixed-outline floorplanning. , 2010, , .		1
51	Run-time mapping of multiple communicating tasks on MPSoC platforms. Procedia Computer Science, 2010, 1, 1019-1026.	1.2	27
52	Selecting profitable custom instructions for reconfigurable processors. Journal of Systems Architecture, 2010, 56, 340-351.	2.5	9
53	Communication-aware heuristics for run-time task mapping on NoC-based MPSoC platforms. Journal of Systems Architecture, 2010, 56, 242-255.	2.5	107
54	Notice of Retraction: Practical algorithm for shortest path on large networks with time-dependent edge-length. , 2010, , .		2

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55	An efficient edge and corner detector. , 2010, , .		2
56	Multiple-choice hardware/software partitioning: Computing model and algorithms. , 2010, , .		1
57	Simple but efficient reconfiguration algorithm for degradable VLSI/WSI arrays. , 2010, , .		2
58	A Novel Approach for Multilevel Fixed Outline Floorplanning. , 2010, , .		0
59	Algorithmic Aspects of Hardware/Software Partitioning: 1D Search Algorithms. IEEE Transactions on Computers, 2010, 59, 532-544.	2.4	48
60	Hierarchical Additive Hough Transform for Lane Detection. IEEE Embedded Systems Letters, 2010, 2, 23-26.	1.3	60
61	Mapping real-life applications on run-time reconfigurable NoC-based MPSoC on FPGA. , 2010, , .		14
62	Performance estimation framework for FPGA-based processors. , 2010, , .		3
63	Preprocessing and Partial Rerouting Techniques for Accelerating Reconfiguration of Degradable VLSI Arrays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 315-319.	2.1	25
64	A Parallel Paths Communication Technique for Energy Efficient Wireless Sensor Networks. Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering, 2010, , 64-78.	0.2	0
65	Minimizing interconnect length on reconfigurable meshes. Frontiers of Computer Science, 2009, 3, 315-321.	0.6	1
66	Mapping Algorithms for NoC-Based Heterogeneous MPSoC Platforms. , 2009, , .		19
67	Efficient Heuristics for Minimizing Communication Overhead in NoC-based Heterogeneous MPSoC Platforms. , 2009, , .		15
68	Efficient Heuristic Algorithm for Rapid Custom-Instruction Selection. , 2009, , .		5
69	Efficient Approximate Algorithm for Hardware/Software Partitioning. , 2009, , .		1
70	Modeling RTOS Components for instruction cache hit rate estimation. , 2009, , .		1
71	Instruction Cache Tuning for Embedded Multitasking Applications. , 2009, , .		3
72	Area-Time Estimation of Controller for Porting C-Based Functions onto FPGA. , 2009, , .		6

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73	A Hybrid Branch-and-Bound Strategy for Hardware/Software Partitioning. , 2009, , .		11
74	Rapid design exploration framework for application-aware customization of soft core processors. , 2009, , .		4
75	Selecting Profitable Custom Instructions for Areaâ€“Time-Efficient Realization on Reconfigurable Architectures. IEEE Transactions on Industrial Electronics, 2009, 56, 3998-4005.	5.2	15
76	Run-time management of custom instructions on a partially reconfigurable architecture. International Journal of Information and Communication Technology, 2009, 2, 50.	0.1	2
77	New Model and Algorithm for Hardware/Software Partitioning. Journal of Computer Science and Technology, 2008, 23, 644-651.	0.9	10
78	Rapid estimation of instruction cache hit rates using loop profiling. , 2008, , .		4
79	Performance Estimation: IPC. , 2008, , .		1
80	Finding minimum interconnect sub-arrays in reconfigurable VLSI arrays. , 2008, , .		2
81	Run-time management of custom instructions on a partially reconfigurable architecture. , 2008, , .		0
82	High-level delay estimation technique for porting C-based applications on FPGA. , 2008, , .		3
83	Fast identification algorithm for application-specific instruction-set extensions. , 2008, , .		1
84	Selection of area-time efficient custom instructions for FPGA realization. , 2008, , .		1
85	Compiler Back End Design for Translating Multi-radio Descriptions to Operating System-less Asynchronous Processor Datapaths. Journal of Computers, 2008, 3, .	0.4	0
86	One-dimensional Search Algorithms for Hardware/Software Partitioning. , 2007, , .		1
87	Integrated Row and Column Rerouting for Reconfiguration of VLSI Arrays with Four-Port Switches. IEEE Transactions on Computers, 2007, 56, 1387-1400.	2.4	38
88	Estimating Area Costs of Custom Instructions for FPGA-based Reconfigurable Processors. , 2007, , .		6
89	Efficient algorithm for functional scheduling in hardware/software co-design. , 2006, , .		0
90	Low-complex dynamic programming algorithm for hardware/software partitioning. Information Processing Letters, 2006, 98, 41-46.	0.4	57

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91	Rapid generation of custom instructions using predefined dataflow structures. Microprocessors and Microsystems, 2006, 30, 355-366.	1.8	5
92	An Efficient Algorithm for DPA-resistent RSA. , 2006, , .		6
93	Unified Signed-Digit Number Adder for RSA and ECC Public-key Cryptosystems. , 2006, , .		8
94	New Reconfiguration Algorithm for Degradable VLSI Arrays. , 2006, , .		1
95	Efficient Algorithms for Hardware/Software Partitioning to Minimize Hardware Area. , 2006, , .		2
96	Power Efficient Sub-Array in Reconfigurable VLSI Meshes. Journal of Computer Science and Technology, 2005, 20, 647-653.	0.9	2
97	Efficient Techniques and Hardware Analysis for Mesh-Connected Processors. Lecture Notes in Computer Science, 2005, , 442-446.	1.0	0
98	An improved reconfiguration algorithm for degradable VLSI/WSI arrays. Journal of Systems Architecture, 2003, 49, 23-31.	2.5	27
99	A SIMD SOLUTION TO BIOSEQUENCE DATABASE SCANNING. , 2002, , .		0
100	Decode filter cache for energy efficient instruction cache hierarchy in super scalar architectures. , 0, , .		2