Benito GonzÃ¡lez

List of Publications by Year
in descending order

33 papers	225 citations	1307594 7 h-index	1058476 14 g-index
33 all docs	33 docs citations	33 times ranked	265 citing authors

#	Article	IF	Citations
1	Gate Length-Dependent Thermal Impedance Characterization of PD-SOI MOSFETs. IEEE Transactions on Electron Devices, 2022, 69, 469-474.	3.0	2
2	RF Extraction of Thermal Resistance for GaN HEMTs on Silicon. IEEE Transactions on Electron Devices, 2022, 69, 2307-2312.	3.0	5
3	A new model of thermionic emission mechanism for non-ideal Schottky contacts and a method of extracting electrical parameters. European Physical Journal Plus, 2020, 135, 1.	2.6	6
4	Geometric Modeling of Thermal Resistance in GaN HEMTs on Silicon. IEEE Transactions on Electron Devices, 2020, 67, 5408-5414.	3.0	4
5	Temperature-Dependent Thermal Capacitance Characterization for SOI-MOSFETs. IEEE Transactions on Electron Devices, 2019, 66, 4120-4125.	3.0	6
6	Single event effects analysis and charge collection mechanisms on AlGaN/GaN HEMTs. Semiconductor Science and Technology, 2019, 34, 035029.	2.0	9
7	DC Gate Leakage Current Model Accounting for Trapping Effects in AlGaN/GaN HEMTs. Electronics (Switzerland), 2018, 7, 210.	3.1	9
8	Thermal Resistance Characterization for Multifinger SOI-MOSFETs. IEEE Transactions on Electron Devices, 2018, 65, 3626-3632.	3.0	7
9	Electrothermal DC characterization of GaN on Si MOS-HEMTs. Solid-State Electronics, 2017, 137, 44-51.	1.4	11
10	Large-Signal DG-MOSFET Modelling for RFID Rectification. Advances in Condensed Matter Physics, 2016, 2016, 1-6.	1.1	0
11	Numerical simulation and compact modelling of AlGaN/GaN HEMTs with mitigation of selfâ€heating effects by substrate materials. Physica Status Solidi (A) Applications and Materials Science, 2015, 212, 1130-1136.	1.8	8
12	DC self-heating effects modelling in SOI and bulk FinFETs. Microelectronics Journal, 2015, 46, 320-326.	2.0	20
13	DC SHEs on GaN HEMTs varying substrate material. , 2015, , .		0
14	N-well resistance modelling in Q-factor of doughnut-shaped PN varactors. Solid-State Electronics, 2015, 103, 104-109.	1.4	0
15	In-depth analysis and modelling of self-heating effects in nanometric DGMOSFETs. Solid-State Electronics, 2013, 79, 179-184.	1.4	13
16	Wide range fully integrated VCO with new cells-based varactor. International Journal of Electronics, 2012, 99, 1165-1178.	1.4	3
17	Numerical dc self-heating in planar double-gate MOSFETs. Semiconductor Science and Technology, 2011, 26, 095014.	2.0	6
18	Capacitive model for integrated PN varactors of cells with N⁺ buried layer. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2010, 23, 364-378.	1.9	4

#	Article	IF	Citations
19	Accurate planar spiral inductor simulations with a 2.5-D electromagnetic simulator. International Journal of RF and Microwave Computer-Aided Engineering, 2008, 18, 242-249.	1.2	1
20	A Physical-based Method for Parameter Extraction of On-Chip Spiral Inductor. , 2007, , .		3
21	Improved tolerance to operation temperature in Î´-doped inverted HFETs. Semiconductor Science and Technology, 2007, 22, 385-391.	2.0	1
22	An Analytical Model of Electric Substrate Losses for Planar Spiral Inductors on Silicon. IEEE Transactions on Electron Devices, 2007, 54, 546-553.	3.0	34
23	<title>DC modeling of PN integrated cross varactors</title>. , 2005, , .		0
24	Characterization of extrinsic resistances in temperature behaviour modelling of InGaAs MODFETs. Semiconductor Science and Technology, 2004, 19, 648-654.	2.0	3
25	Integrated Inductors Modeling for Library Development and Layout Generation. Analog Integrated Circuits and Signal Processing, 2003, 35, 121-132.	1.4	6
26	Empirical model of the metal losses in integrated inductors. , 2003, , .		0
27	Temperature in HFETs when operating in DC. , 2003, , .		0
28	Power model for DCFL family. Electronics Letters, 2002, 38, 13.	1.0	6
29	Static simulation of pseudomorphic heterostructure FETs at medium/high temperatures. Semiconductor Science and Technology, 2002, 17, 534-539.	2.0	1
30	Models and Tools for CMOS Integrated Inductors. Analog Integrated Circuits and Signal Processing, 2002, 33, 171-178.	1.4	5
31	Optimization of the delta-doped layer in P-HFETs at medium/high temperatures. Semiconductor Science and Technology, 2000, 15, L19-L23.	2.0	4
32	An energy relaxation time model for device simulation. Solid-State Electronics, 1999, 43, 1791-1795.	1.4	41
33	Modelling of low power cw laser beam heating effects on A GaAs substrate. Solid-State Electronics, 1998, 42, 809-816.	1.4	7