Ronald F Demara

List of Publications by Year
in descending order

167	1,878	331670	434195
papers	citations	21 h-index	31 g-index

167	167	167	1245
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Design and evaluation of an ultra-area-efficient fault-tolerant QCA full adder. Microelectronics Journal, 2015, 46, 531-542.	2.0	109
2	Towards ultra-efficient QCA reversible circuits. Microprocessors and Microsystems, 2017, 49, 127-138.	2.8	80
3	Self-healing reconfigurable logic using autonomous group testing. Microprocessors and Microsystems, 2013, 37, 174-184.	2.8	68
4	Understanding the propagation of transient errors in HPC applications. , 2015, , .		60
5	Voltage-Based Concatenatable Full Adder Using Spin Hall Effect Switching. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 2134-2138.	2.7	45
6	A Parity-Preserving Reversible QCA Gate with Self-Checking Cascadable Resiliency. IEEE Transactions on Emerging Topics in Computing, 2018, 6, 450-459.	4.6	43
7	A Tunable Majority Gate-Based Full Adder Using Current-Induced Domain Wall Nanomagnets. IEEE Transactions on Magnetics, 2016, 52, 1-7.	2.1	40
8	Scalable FPGA-based architecture for DCT computation using dynamic partial reconfiguration. Transactions on Embedded Computing Systems, 2009, 9, 1-18.	2.9	39
9	Scalable Adaptive Spintronic Reconfigurable Logic Using Area-Matched MTJ Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 678-682.	3.0	39
10	Energy-Aware Adaptive Restore Schemes for MLC STT-RAM Cache. IEEE Transactions on Computers, 2017, 66, 786-798.	3.4	38
11	Learning tactical human behavior through observation of human performance. IEEE Transactions on Systems, Man, and Cybernetics, 2006, 36, 128-140.	5.0	37
12	Composable Probabilistic Inference Networks Using MRAM-based Stochastic Neurons. ACM Journal on Emerging Technologies in Computing Systems, 2019, 15, 1-22.	2.3	33
13	Energy-Efficient Nonvolatile Reconfigurable Logic using Spin Hall Effect-based Lookup Tables. IEEE Nanotechnology Magazine, 2016, , 1-1.	2.0	32
14	Progress in autonomous fault recovery of field programmable gate arrays. ACM Computing Surveys, 2011, 43, 1-30.	23.0	30
15	Majority-Based Spin-CMOS Primitives for Approximate Computing. IEEE Nanotechnology Magazine, 2018, , 1-1.	2.0	30
16	Low-Energy Deep Belief Networks Using Intrinsic Sigmoidal Spintronic-based Probabilistic Neurons. , 2018, , .		29
17	Survey of STT-MRAM Cell Design Strategies. ACM Journal on Emerging Technologies in Computing Systems, 2017, 13, 1-16.	2.3	29
18	AOS. , 2016, , .		28

#	Article	IF	Citations
19	A Genetic Representation for Evolutionary Fault Recovery in Virtex FPGAs. Lecture Notes in Computer Science, 2003, , 47-56.	1.3	27
20	Towards a method for evaluating naturalness in conversational dialog systems. , 2009, , .		26
21	Evaluation of the Human Impact of Password Authentication. Informing Science, 0, 7, 0067-085.	0.0	26
22	Data-partitioning using the Hilbert space filling curves: Effect on the speed of convergence of Fuzzy ARTMAP for large database problems. Neural Networks, 2005, 18, 967-984.	5.9	25
23	Contemporary CMOS aging mitigation techniques: Survey, taxonomy, and methods. The Integration VLSI Journal, 2017, 59, 10-22.	2.1	25
24	Towards a Context-Based Dialog Management Layer for Expert Systems. , 2009, , .		24
25	Energy-Efficient and Process-Variation-Resilient Write Circuit Schemes for Spin Hall Effect MRAM Device. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2394-2401.	3.1	24
26	NV-Clustering: Normally-Off Computing Using Non-Volatile Datapaths. IEEE Transactions on Computers, 2018, 67, 949-959.	3.4	23
27	Cost-efficient QCA reversible combinational circuits based on a new reversible gate. , 2015, , .		22
28	A Novel Compound Synapse Using Probabilistic Spinâ€“Orbit-Torque Switching for MTJ-Based Deep Neural Networks. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 182-187.	1.5	22
29	ApGAN: Approximate GAN for Robust Low Energy Learning From Imprecise Components. IEEE Transactions on Computers, 2020, 69, 349-360.	3.4	22
30	Elevating Learner Achievement Using Formative Electronic Lab Assessments in the Engineering Laboratory: A Viable Alternative to Weekly Lab Reports. IEEE Transactions on Education, 2018, 61, 1-10.	2.4	20
31	A Sustainable Model for Integrating Current Topics in Machine Learning Research Into the Undergraduate Curriculum. IEEE Transactions on Education, 2009, 52, 503-512.	2.4	18
32	Expediting GA-Based Evolution Using Group Testing Techniques for Reconfigurable Hardware. , 2006, , .		17
33	Energy and area analysis of a floating-point unit in 15nm CMOS process technology. , 2015, , .		17
34	Non-Volatile Spintronic Flip-Flop Design for Energy-Efficient SEU and DNU Resilience. IEEE Transactions on Magnetics, 2019, 55, 1-11.	2.1	17
35	Layered Approach to Intrinsic Evolvable Hardware using Direct Bitstream Manipulation of Virtex II Pro Devices. , 2007, , .		16
36	Autonomic fault-handling and refurbishment using throughput-driven assessment. Applied Soft Computing Journal, 2011, 11, 1588-1599.	7.2	16

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37	Bit-Upset Vulnerability Factor for eDRAM Last Level Cache immunity analysis. , 2016, , .		16
38	AI in Informal Science Education: Bringing Turing Back to Life to Perform the Turing Test. International Journal of Artificial Intelligence in Education, 2017, 27, 353-384.	5.5	16
39	Consensus-Based Evaluation for Fault Isolation and On-line Evolutionary Regeneration. Lecture Notes in Computer Science, 2005, , 12-24.	1.3	16
40	Wire crossing constrained QCA circuit design using bilayer logic decomposition. Electronics Letters, 2015, 51, 1677-1679.	1.0	15
41	Composite spintronic accuracy-configurable adder for low power Digital Signal Processing. , 2017, , .		15
42	Energy-Aware Adaptive Rate and Resolution Sampling of Spectrally Sparse Signals Leveraging VCMA-MTJ Devices. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 679-692.	3.6	15
43	A Multilayer Framework Supporting Autonomous Run-Time Partial Reconfiguration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 504-516.	3.1	14
44	Applicability of power-gating strategies for aging mitigation of CMOS logic paths. , 2014, , .		14
45	Redesigning Computer Engineering Gateway Courses Using a Novel Remediation Hierarchy. , 0, , .		14
46	Radiation-hardened MRAM-based LUT for non-volatile FPGA soft error mitigation with multi-node upset tolerance. Journal Physics D: Applied Physics, 2017, 50, 505002.	2.8	14
47	Mitigating Process Variability for Non-Volatile Cache Resilience and Yield. IEEE Transactions on Emerging Topics in Computing, 2020, 8, 724-737.	4.6	14
48	Triple Modular Redundancy with Standby (TMRSB) Supporting Dynamic Resource Reconfiguration. IEEE Autotestcon Proceedings, 2006, , .	0.0	13
49	Tiered Algorithm for Distributed Process Quiescence and Termination Detection. IEEE Transactions on Parallel and Distributed Systems, 2007, 18, 1529-1538.	5.6	13
50	Scalable FPGA Refurbishment Using Netlist-Driven Evolutionary Algorithms. IEEE Transactions on Computers, 2013, 62, 1526-1541.	3.4	13
51	Heterogeneous energyâ€saparing reconfigurable logic: spinâ€based storage and CNFETâ€based multiplexing. IET Circuits, Devices and Systems, 2017, 11, 274-279.	1.4	12
52	Read-Tuned STT-RAM and eDRAM Cache Hierarchies for Throughput and Energy Optimization. IEEE Access, 2018, 6, 14576-14590.	4.2	12
53	SLIM-ADC: Spin-based Logic-In-Memory Analog to Digital Converter leveraging SHE-enabled Domain Wall Motion devices. Microelectronics Journal, 2018, 81, 137-143.	2.0	12
54	Low-Energy Acceleration of Binarized Convolutional Neural Networks Using a Spin Hall Effect Based Logic-in-Memory Architecture. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 928-940.	4.6	12

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55	Design-for-Diversity for Improved Fault-Tolerance of TMR Systems on FPGAs. , 2011, , .		11
56	Energy-efficient multiplier-less discrete convolver through probabilistic domain transformation. , 2014, , .		11
57	Exploring the Effect of Compiler Optimizations on the Reliability of HPC Applications. , 2017, , .		11
58	Processing-In-Memory Acceleration of Convolutional Neural Networks for Energy-Effciency, and Power-Intermittency Resilience. , 2019, , .		11
59	Probabilistic Interpolation Recoder for Energy-Error-Product Efficient DBNs With p-Bit Devices. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 2146-2157.	4.6	11
60	MRAM-Based Stochastic Oscillators for Adaptive Non-Uniform Sampling of Sparse Signals in IoT Applications. , 2019, , .		10
61	The SNAP-1 parallel AI prototype. IEEE Transactions on Parallel and Distributed Systems, 1993, 4, 841-854.	5.6	9
62	Parallelization of Fuzzy ARTMAP to improve its convergence speed: The network partitioning approach and the data partitioning approach. Nonlinear Analysis: Theory, Methods & Applications, 2005, 63, e877-e889.	1.1	9
63	Intrinsic evolvable hardware platform for digital circuit design and repair using genetic algorithms. Applied Soft Computing Journal, 2012, 12, 2470-2480.	7.2	9
64	Fast Online Diagnosis and Recovery of Reconfigurable Logic Fabrics Using Design Disjunction. IEEE Transactions on Computers, 2016, 65, 3055-3069.	3.4	9
65	Loss-Aware Switch Design and Non-Blocking Detection Algorithm for Intra-Chip Scale Photonic Interconnection Networks. IEEE Transactions on Computers, 2016, 65, 1789-1801.	3.4	9
66	Energy and Delay Tradeoffs of Soft-Error Masking for 16-nm FinFET Logic Paths: Survey and Impact of Process Variation in the Near-Threshold Region. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 695-699.	3.0	9
67	Clockless Spintronic Logic: A Robust and Ultra-Low Power Computing Paradigm. IEEE Transactions on Computers, 2018, 67, 631-645.	3.4	9
68	NULL convention multiply and accumulate unit with conditional rounding, scaling, and saturation. Journal of Systems Architecture, 2002, 47, 977-998.	4.3	8
69	Mitigation of network tampering using dynamic dispatch of mobile agents. Computers and Security, 2004, 23, 31-42.	6.0	8
70	PARC: A Novel Design Methodology for <u>P</u>ower <u>A</u>nalysis <u>R</u>esilient <u>C</u>ircuits Using Spintronics. IEEE Nanotechnology Magazine, 2019, 18, 885-889.	2.0	8
71	Short-Term Long-Term Compute-in-Memory Architecture: A Hybrid Spin/CMOS Approach Supporting Intrinsic Consolidation. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, 62-70.	1.5	8
72	Pipelining of Fuzzy ARTMAP without matchtracking: Correctness, performance bound, and Beowulf evaluation. Neural Networks, 2007, 20, 109-128.	5.9	7

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73	Fault Demotion Using Reconfigurable Slack (FaDReS). IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1364-1368.	3.1	7
74	Self-Adapting Resource Escalation for Resilient Signal Processing Architectures. Journal of Signal Processing Systems, 2014, 77, 257-280.	2.1	7
75	Process variation immune and energy aware sense amplifiers for resistive non-volatile memories. , 2017, , .		7
76	Designing and Evaluating Redundancy-Based Soft-Error Masking on a Continuum of Energy versus Robustness. IEEE Transactions on Sustainable Computing, 2018, 3, 139-152.	3.1	7
77	Survivability Modeling and Resource Planning for Self-Repairing Reconfigurable Device Fabrics. IEEE Transactions on Cybernetics, 2018, 48, 780-792.	9.5	7
78	MRAM-Enhanced Low Power Reconfigurable Fabric With Multi-Level Variation Tolerance. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4662-4672.	5.4	7
79	Design and Evaluation of DNU-Tolerant Registers for Resilient Architectural State Storage. , 2019, , .		7
80	Clockless Spin-based Look-Up Tables with Wide Read Margin. , 2019, , .		7
81	Subthreshold Spintronic Stochastic Spiking Neural Networks With Probabilistic Hebbian Plasticity and Homeostasis. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 43-51.	1.5	7
82	A Physical Resource Management Approach to Minimizing FPGA Partial Reconfiguration Overhead. , 2006, , .		6
83	Reactive rejuvenation of CMOS logic paths using self-activating voltage domains. , 2015, , .		6
84	Designing energy-efficient approximate adders using parallel genetic algorithms. , 2015, , .		6
85	Secure intermittent-robust computation for energy harvesting device security and outage resilience. , 2017, , .		6
86	Hybrid spinâ€CMOS stochastic spiking neuron for highâ€speed emulation of In vivo neuron dynamics. IET Computers and Digital Techniques, 2018, 12, 122-129.	1.2	6
87	Context-driven Near-term Intention Recognition. Journal of Defense Modeling and Simulation, 2004, 1, 153-170.	1.7	5
88	CONFIDANT: Collaborative Object Notification Framework for Insider Defense using Autonomous Network Transactions. Autonomous Agents and Multi-Agent Systems, 2006, 12, 93-114.	2.1	5
89	Adaptive Mitigation of Radiation-Induced Errors and TDDB in Reconfigurable Logic Fabrics. , 2015, , .		5
90	Process variation immunity of alternative 16nm HK/MG-based FPGA logic blocks. , 2015, , .		5

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91	Soft Error Effect Tolerant Temporal Self-Voting Checkers: Energy vs. Resilience Tradeoffs. , 2016, , .		5
92	Intrinsic Evolution of Truncated Puiseux Series on a Mixed-Signal Field-Programmable SoC. IEEE Access, 2016, 4, 2863-2872.	4.2	5
93	AQuRate. , 2019, , .		5
94	Mixed-Signal Spin/Charge Reconfigurable Array for Energy-Aware Compressive Signal Processing. , 2019, , .		5
95	Adaptive Non-Uniform Compressive Sensing Using SOT-MRAM Multi-Bit Precision Crossbar Arrays. IEEE Nanotechnology Magazine, 2021, 20, 224-228.	2.0	5
96	GLASS: Group Learning At Significant Scale via WiFi-Enabled Learner Design Teams in an ECE Flipped Classroom. , 0, , .		5
97	A parallel computational model for integrated speech and natural language understanding. IEEE Transactions on Computers, 1993, 42, 1171-1183.	3.4	4
98	Distributed-sum termination detection supporting multithreaded execution. Parallel Computing, 2003, 29, 953-968.	2.1	4
99	A Self-Configuring TMR Scheme Utilizing Discrepancy Resolution. , 2011, , .		4
100	Passing an Enhanced Turing Test â€“ Interacting with Lifelike Computer Representations of Specific Individuals. Journal of Intelligent Systems, 2013, 22, 365-415.	1.6	4
101	Power and quality-aware image processing soft-resilience using online multi-objective GAs. International Journal of Computational Vision and Robotics, 2015, 5, 72.	0.3	4
102	ASTRO: Synthesizing application-specific reconfigurable hardware traces to exploit memory-level parallelism. Microprocessors and Microsystems, 2015, 39, 553-564.	2.8	4
103	Self-Scaling Evolution of analog computation circuits with digital accuracy refinement. , 2015, , .		4
104	Area-energy tradeoffs of logic wear-leveling for BTI-induced aging. , 2016, , .		4
105	Variation-immune resistive Non-Volatile Memory using self-organized sub-bank circuit designs. , 2017, , .		4
106	A Spin-Orbit Torque based Cellular Neural Network (CNN) Architecture. , 2017, , .		4
107	Logic-Encrypted Synthesis for Energy-Harvesting-Powered Spintronic-Embedded Datapath Design. , 2018, , .		4
108	Guest Editorial: IEEE Transactions on Computers Special Section on Emerging Non-Volatile Memory Technologies: From Devices to Architectures and Systems. IEEE Transactions on Computers, 2019, 68, 1111-1113.	3.4	4

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109	Engineering assessment strata: A layered approach to evaluation spanning Bloomâ€™s taxonomy of learning. Education and Information Technologies, 2019, 24, 1147-1171.	5.7	4
110	Using Context-Based Neural Networks to Maintain Coherence Among Entities' States in a Distributed Simulation. Journal of Defense Modeling and Simulation, 2007, 4, 147-172.	1.7	3
111	Heterogeneous Concurrent Error Detection (hCED) Based on Output Anticipation. , 2011, , .		3
112	Hypergraph-Cover Diversity for Maximally-Resilient Reconfigurable Systems. , 2015, , .		3
113	Heterogeneous Technology Configurable Fabrics for Field-Programmable Co-Design of CMOS and Spin-Based Devices. , 2017, , .		3
114	Compact Spintronic Muller C-Element With Near-Zero Standby Energy. IEEE Transactions on Magnetics, 2018, 54, 1-7.	2.1	3
115	Leveraging Spintronic Devices for Efficient Approximate Logic and Stochastic Neural Networks. , 2018, , .		3
116	Robust and Large-Scale Convolution through Stochastic-Based Processing without Multipliers. IEEE Transactions on Emerging Topics in Computing, 2019, 7, 80-97.	4.6	3
117	Compact lowâ€power instant store and restore D flipâ€flop using a selfâ€complementing spintronic device. Electronics Letters, 2016, 52, 1238-1240.	1.0	3
118	Implementing Student-Created Video in Engineering: An Active Learning Approach for Exam Preparedness. International Journal of Engineering Pedagogy, 2019, 9, 63.	1.1	3
119	PDU Bundling and Replication for Reduction of Distributed Simulation Communication Traffic. Journal of Defense Modeling and Simulation, 2004, 1, 171-183.	1.7	2
120	Sustainability assurance modeling for SRAM-based FPGA evolutionary self-repair. , 2014, , .		2
121	Activity-Based Resource Allocation for Motion Estimation Engines. Journal of Circuits, Systems and Computers, 2015, 24, 1550004.	1.5	2
122	SNRA: A Spintronic Neuromorphic Reconfigurable Array for In-Circuit Training and Evaluation of Deep Belief Networks. , 2018, , .		2
123	Lockdown Computerized Testing Interwoven with Rapid Remediation: A Crossover Study within a Mechanical Engineering Core Course. , 2018, , .		2
124	Synthesis of normally-off boolean circuits: An evolutionary optimization approach utilizing spintronic devices. , 2018, , .		2
125	Energy Efficient Mobile Service Computing With Differential Spintronic-C-Elements: A Logic-in-Memory Asynchronous Computing Paradigm. IEEE Access, 2019, 7, 55851-55860.	4.2	2
126	An Efficient Video Prediction Recurrent Network using Focal Loss and Decomposed Tensor Train for Imbalance Dataset. , 2021, , .		2

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127	Process Variation Sensitivity of Spin-Orbit Torque Perpendicular Nanomagnets in DBNs. IEEE Transactions on Magnetics, 2021, 57, 1-8.	2.1	2
128	Long Short-Term Memory with Spin-Based Binary and Non-Binary Neurons. , 2021, , .		2
129	Spin-Orbit Torque Neuromorphic Fabrics for Low-Leakage Reconfigurable In-Memory Computation. IEEE Transactions on Electron Devices, 2022, 69, 1727-1735.	3.0	2
130	Embedded STT-MRAM Energy Analysis for Intermittent Applications using Mean Standby Duration. , 2021, , .		2
131	Helical latch for scalable Boolean logic operations. Nanotechnology, 1994, 5, 137-156.	2.6	1
132	<title>Integer-encoded massively parallel processing of fast-learning fuzzy ARTMAP neural networks</title>. , 1997, , .		1
133	SELF-TIMED ARCHITECTURE FOR MASKED SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERSION. Journal of Circuits, Systems and Computers, 2007, 16, 1-14.	1.5	1
134	Distance-Ranked Fault Identification of Reconfigurable Hardware Bitstreams via Functional Input. International Journal of Reconfigurable Computing, 2014, 2014, 1-21.	0.2	1
135	Design of Testable Adder Circuits for Spintronics Based Nanomagnetic Computing. , 2015, , .		1
136	Guest Editorial: IEEE Transactions on Computers and IEEE Transactions on Emerging Topics in Computing Joint Special Section on Innovation in Reconfigurable Computing Fabrics from Devices to Architectures. IEEE Transactions on Emerging Topics in Computing, 2017, 5, 207-209.	4.6	1
137	Non-Volatile Memory Trends: Toward Improving Density and Energy Profiles across the System Stack. Computer, 2018, 51, 12-13.	1.1	1
138	BGIM: Bit-Grained Instant-on Memory Cell for Sleep Power Critical Mobile Applications. , 2018, , .		1
139	An Ultra-Low Power Spintronic Stochastic Spiking Neuron with Self-Adaptive Discrete Sampling. , 2019, , .		1
140	Leveraging Stochasticity for In Situ Learning in Binarized Deep Neural Networks. Computer, 2019, 52, 30-39.	1.1	1
141	IRC Cross-Layer Design Exploration of Intermittent Robust Computation Units for IoTs. , 2019, , .		1
142	Efficacy and perceptions of assessment digitization within a largeâ€enrollment mechanical and aerospace engineering course. Computer Applications in Engineering Education, 2019, 27, 419-429.	3.4	1
143	Self-Organized Sub-bank SHE-MRAM-based LLC: An energy-efficient and variation-immune read and write architecture. The Integration VLSI Journal, 2019, 65, 293-307.	2.1	1
144	A Reconfigurable and Compact Spin-Based Analog Block for Generalizable nth Power and Root Computation. , 2021, , .		1

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145	Non-adaptive sparse recovery and fault evasion using disjunct design configurations (abstract only). , 2014, , .		1
146	Generalized Exponentiation Using STT Magnetic Tunnel Junctions: Circuit Design, Performance, and Application to Neural Network Gradient Decay. SN Computer Science, 2022, 3, 1.	3.6	1
147	Digitizing and Remediating Engineering Assessments: An Immersive and Transportable Faculty Development Workshop. , 0, , .		1
148	Learner Capstone Panels for Immersing Undergraduates in Mechanisms of Engineering Research. , 0, , .		1
149	High-Fidelity Digitized Assessment of Heat Transfer Fundamentals using a Tiered Delivery Strategy. , 0, , .		1
150	PERFORMANCE OF SCALABLE SHARED-MEMORY ARCHITECTURES. Journal of Circuits, Systems and Computers, 2000, 10, 1-22.	1.5	0
151	Editorial Appointments for 2005â€“2006 Term. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 773-782.	3.1	0
152	Passing an Enhanced Turing Test â€“ Interacting with Lifelike Computer Representations of Specific Individuals. Journal of Intelligent Systems, 2014, 23, 357.	1.6	0
153	Stochastically Estimating Modular Criticality in Large-Scale Logic Circuits Using Sparsity Regularization and Compressive Sensing. Journal of Low Power Electronics and Applications, 2015, 5, 3-37.	2.0	0
154	Optimally Fortifying Logic Reliability through Criticality Ranking. Electronics (Switzerland), 2015, 4, 150-172.	3.1	0
155	Guest Editorial: IEEE Transactions on Computers and IEEE Transactions on Emerging Topics in Computing Joint Special Section on Innovation in Reconfigurable Computing Fabrics from Devices to Architectures. IEEE Transactions on Computers, 2017, 66, 927-929.	3.4	0
156	RAW Keynote Speakers. , 2017, , .		0
157	High-Performance Double Node Upset-Tolerant Non-Volatile Flip-Flop Design. , 2018, , .		0
158	An Analysis of Voltage-Driven Spintronic Device Concatenation Through Spin Pumping. , 2018, , .		0
159	Virtualized Active Learning for Undergraduate Engineering Disciplines (VALUED):A Pilot in a Large Enrollment STEM Classroom. , 2019, , .		0
160	Electrically-Tunable Stochasticity for Spin-based Neuromorphic Circuits: Self-Adjusting to Variation. , 2020, , .		0
161	Data Mining of Assessments to Generate Learner Remediation Teams: Method, Efficacy, and Perceptions in an Undergraduate Engineering Pilot Offering. Journal of Educational Technology Systems, 2020, 48, 464-492.	5.8	0
162	High Accuracy Deep Belief Network: Fuzzy Neural Networks using MRAM-based Stochastic Neurons. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, , 1-1.	1.5	0

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163	Leveraging design diversity to counteract process variation: theory, method, and FPGAtoolchain to increase yield and resilienceinâ€situ. IET Computers and Digital Techniques, 2019, 13, 250-261.	1.2	0
164	Workshop on Virtualized Active Learning in STEM. , 2019, , .		0
165	Adapting Mixed-Mode Instructional Delivery to Thrive within STEM Curricula. , 0, , .		0
166	Board 38: Methods and Outcomes of the NSF Project on Synthesizing Environments for Digitally Mediated Team Learning. , 0, , .		0
167	Automated Formation of Peer-learning Cohorts Using Computer-based Assessment Data: A Double-blind Study within a Software Engineering Course. , 0, , .		0