Kia Bazargan

List of Publications by Year
in descending order

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37 papers	894 citations	1478505 6 h-index	1281871 11 g-index
38 all docs	38 docs citations	38 times ranked	399 citing authors

#	Article	IF	Citations
1	Approximate Constant-Coefficient Multiplication Using Hybrid Binary-Unary Computing for FPGAs. ACM Transactions on Reconfigurable Technology and Systems, 2022, 15, 1-25.	2.5	2
2	Parallel Unary Computing Based on Function Derivatives. ACM Transactions on Reconfigurable Technology and Systems, 2021, 14, 1-25.	2.5	4
3	Low-Cost Approximate Constant Coefficient Hybrid Binary-Unary Multiplier for DSP Applications. , 2020, , .		4
4	Deterministic Shuffling Networks to Implement Stochastic Circuits in Parallel. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1821-1832.	3.1	4
5	Hybrid Binary-Unary Hardware Accelerator. IEEE Transactions on Computers, 2020, 69, 1308-1319.	3.4	14
6	Hybrid binary-unary truncated multiplication for DSP Applications on FPGAs. , 2020, , .		0
7	Energy-Efficient Convolutional Neural Networks with Deterministic Bit-Stream Processing. , 2019, , .		33
8	Energy-Efficient Near-Sensor Convolution using Pulsed Unary Processing. , 2019, , .		2
9	Accelerating Deterministic Bit-Stream Computing with Resolution Splitting. , 2019, , .		10
10	Hybrid binary-unary hardware accelerator. , 2019, , .		14
11	Routing Magic. , 2018, , .		22
12	Low-Cost Sorting Network Circuits Using Unary Processing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1471-1480.	3.1	48
13	Low latency parallel implementation of traditionally-called stochastic circuits using deterministic shuffling networks. , 2018, , .		6
14	Polysynchronous Clocking: Exploiting the Skew Tolerance of Stochastic Circuits. IEEE Transactions on Computers, 2017, 66, 1734-1746.	3.4	4
15	Stochastic Implementation and Analysis of Dynamical Systems Similar to the Logistic Map. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 747-759.	3.1	2
16	Power and Area Efficient Sorting Networks Using Unary Processing. , 2017, , .		11
17	A memory optimized mersenne-twister random number generator. , 2017, , .		3
18	Polysynchronous stochastic circuits. , 2016, , .		12

#	Article	IF	Citations
19	Improving linear feedback shift registers using similarity transformations. , 2015, , .		0
20	Randomness meets feedback. , 2015, , .		18
21	Computation on Stochastic Bit Streams Digital Image Processing Case Studies. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 449-462.	3.1	216
22	Logical Computation on Stochastic Bit Streams with Linear Finite-State Machines. IEEE Transactions on Computers, 2014, 63, 1474-1486.	3.4	56
23	IIR filters using stochastic arithmetic. , 2014, , .		22
24	IIR filters using stochastic arithmetic. , 2014, , .		4
25	Sequential logic to transform probabilities. , 2013, , .		2
26	Stochastic functions using sequential logic. , 2013, , .		8
27	A new hybrid topology for network on chip. , 2012, , .		2
28	The synthesis of linear Finite State Machine-based Stochastic Computational Elements. , 2012, , .		8
29	An Architecture for Fault-Tolerant Computation with Stochastic Logic. IEEE Transactions on Computers, 2011, 60, 93-105.	3.4	332
30	Improvements on Efficiency and Efficacy of SPFD-Based Rewiring for LUT-Based Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1870-1883.	2.7	0
31	A fast SPFD-based rewiring technique. , 2010, , .		1
32	Estimation and optimization of reliability of noisy digital circuits. , 2009, , .		13
33	Thermal-aware floorplanning for task migration enabled active sub-threshold leakage reduction. , 2008, , .		4
34	FPGA family composition and effects of specialized blocks. , 2008, , .		1
35	Clustering based pruning for statistical criticality computation under process variations. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	10
36	Defect-Tolerant FPGA Architecture Exploration. , 2006, , .		2

#	Article	IF	Citations
37	A Novel Memory Structure for Embedded Systems: Flexible Sequential and Random Access Memory. Journal of Computer Science and Technology, 2005, 20, 596-606.	1.5	0