Ming-Dou Ker

List of Publications by Year
in descending order

433	5,033	147801	189892
papers	citations	31 h-index	50 g-index

434	434	434	1484
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	ESD HBM Discharge Model in RF GaN-on-Si (MIS)HEMTs. IEEE Transactions on Electron Devices, 2022, 69, 2180-2187.	3.0	5
2	Closed-Loop Neuromodulation System-on-Chip (SoC) for Detection and Treatment of Epilepsy. , 2022, , 383-412.		0
3	The Parasitic Latch-Up Path From Substrate Pâ¥ Guard Ring to the NMOS in Deep N-Well Operating With Negative Voltage Sources. IEEE Electron Device Letters, 2022, 43, 604-606.	3.9	2
4	Single Chip of Electrostatic Discharge Detector for IC Manufacturing Field Control. , 2022, , .		1
5	Schottky-Embedded Isolation Ring to Improve Latch-Up Immunity Between HV and LV Circuits in a 0.18 Î¼m BCD Technology. IEEE Journal of the Electron Devices Society, 2022, 10, 516-524.	2.1	2
6	Using Schottky Barrier Diode to Improve Latch-Up Immunity for CMOS ICs Operating With Negative Voltage Sources. IEEE Electron Device Letters, 2021, 42, 395-397.	3.9	10
7	Study on the Guard Rings for Latchup Prevention between HV-PMOS and LV-PMOS in a 0.15-Âµm BCD Process. , 2021, , .		1
8	Design of 2xVDD-Tolerant Power-Rail ESD Clamp Circuit Against False Trigger During Fast Power-ON Events. , 2021, , .		0
9	Stacking-MOS Protection Design for Interface Circuits Against Cross-Domain CDM ESD Stresses. IEEE Transactions on Electron Devices, 2021, 68, 1461-1470.	3.0	6
10	Schottky-Embedded Silicon-Controlled Rectifier With High Holding Voltage Realized in a 0.18-Î¼m Low-Voltage CMOS Process. IEEE Transactions on Electron Devices, 2021, 68, 1764-1771.	3.0	12
11	The Impact of Holding Voltage of Transient Voltage Suppressor (TVS) on Signal Integrity of Microelectronics System With CMOS ICs Under System-Level ESD and EFT/Burst Tests. IEEE Transactions on Electron Devices, 2021, 68, 2152-2159.	3.0	6
12	Monopolar Biphasic Stimulator With Discharge Function and Negative Level Shifter for Neuromodulation SoC Integration in Low-Voltage CMOS Process. IEEE Transactions on Biomedical Circuits and Systems, 2021, 15, 568-579.	4.0	19
13	From Bioelectronics to Nanobioelectronics: The Biomedical Electronics Translational Research Center [Highlights]. IEEE Nanotechnology Magazine, 2021, 15, 3-6.	1.3	0
14	Design of a Bone-Guided Cochlear Implant Microsystem With Monopolar Biphasic Multiple Stimulations and Evoked Compound Action Potential Acquisition and Its In Vivo Verification. IEEE Journal of Solid-State Circuits, 2021, 56, 3062-3076.	5.4	15
15	Closed-Loop Neuromodulation System-on-Chip (SoC) for Detection and Treatment of Epilepsy. , 2021, , 1-30.		0
16	Study on CDM ESD Robustness Among On-Chip Decoupling Capacitors in CMOS Integrated Circuits. IEEE Journal of the Electron Devices Society, 2021, 9, 881-890.	2.1	2
17	NBL Causing Low Latch-up Immunity between HV-PMOS and LV-P/NMOS in a 0.15-Âµm BCD Process. , 2021, , .		1
18	ESD Failures of GaN-on-Si D-Mode AlGaN/GaN MIS-HEMT and HEMT Devices for 5G Telecommunications. , 2021, , .		4

#	Article	IF	Citations
19	Study on Transmitter with Stacking-MOS Structure of Interface Circuits for Cross-Domain CDM ESD Protection. , 2021, , .		0
20	Editorial: Microelectronic Implants for Central and Peripheral Nervous System: Overview of Circuit and System Technology. Frontiers in Neuroscience, 2021, 15, 794944.	2.8	0
21	A microvalve cell printing technique using riboflavin photosensitizer for selective cell patterning onto a retinal chip. Bioprinting, 2020, 20, e00097.	5.8	8
22	Over-Voltage Protection on the CC Pin of USB Type-C Interface against Electrical Overstress Events. , 2020, , .		0
23	Miniaturized Intracerebral Potential Recorder for Long-Term Local Field Potential of Deep Brain Signals. , 2020, 2020, 5188-5191.		0
24	Design of Stage-Selective Negative Voltage Generator to Improve On-Chip Power Conversion Efficiency for Neuron Stimulation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4122-4131.	5.4	12
25	Optimization on On-Chip Surge Protection Device for USB Type-C HV Pins. , 2020, , .		2
26	New Energy Transformation Model for the Unclamped Inductive Switching (UIS) Test. , 2020, , .		2
27	Transient Voltage Suppressor (TVS) on Signal Integrity of Microelectronics System with CMOS ICs under System-Level ESD Test. , 2020, , .		2
28	RF/High-Speed I/O ESD Protection: Co-optimizing Strategy Between BEOL Capacitance and HBM Immunity in Advanced CMOS Process. IEEE Transactions on Electron Devices, 2020, 67, 2752-2759.	3.0	7
29	On-Chip Over-Voltage Protection Design Against Surge Events on the CC Pin of USB Type-C Interface. IEEE Transactions on Electron Devices, 2020, 67, 2702-2709.	3.0	1
30	Design of Dual-Mode Stimulus Chip With Built-In High Voltage Generator for Biomedical Applications. IEEE Transactions on Biomedical Circuits and Systems, 2020, 14, 961-970.	4.0	12
31	Energy Transformation Between the Inductor and the Power Transistor for the Unclamped Inductive Switching (UIS) Test. IEEE Transactions on Device and Materials Reliability, 2020, 20, 413-419.	2.0	7
32	Design of Fin-Diode-Triggered Rotated Silicon-Controlled Rectifier for High- Speed Digital Application in 16-nm FinFET Process. IEEE Transactions on Electron Devices, 2020, 67, 2725-2731.	3.0	8
33	Design of High-Voltage-Tolerant Power-Rail ESD Protection Circuit for Power Pin of Negative Voltage in Low-Voltage CMOS Processes. IEEE Transactions on Electron Devices, 2020, 67, 40-46.	3.0	4
34	Improved Design and In Vivo Animal Tests of Bone-Guided Cochlear Implant Microsystem with Monopolar Biphasic Multiple Stimulation and Neural Action Potential Acquisition. , 2020, , .		1
35	Study and Verification on the Latch-Up Path Between I/O pMOS and N-Type Decoupling Capacitors in 0.18-mu m CMOS Technology. IEEE Transactions on Device and Materials Reliability, 2019, 19, 445-451.	2.0	8
36	An Efficient, Wide-Output, High-Voltage Charge Pump With a Stage Selection Circuit Realized in a Low-Voltage CMOS Process. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3437-3444.	5.4	24

#	Article	IF	Citations
37	Investigation on Latch-Up Path Between I/O PMOS and Core PMOS in a 0.18-Î¼m CMOS Process. , 2019, , .		2
38	Area-Efficient On-Chip Transient Detection Circuit for System-Level ESD Protection Against Transient-Induced Malfunction. IEEE Transactions on Device and Materials Reliability, 2019, 19, 363-369.	2.0	3
39	A 13.56 MHz Metamaterial for the Wireless Power Transmission Enhancement in Implantable Biomedical Devices. , 2019, , .		4
40	Avalanche Ruggedness Capability and Improvement of 5-V n-Channel Large-Array MOSFET in BCD Process. IEEE Transactions on Electron Devices, 2019, 66, 3040-3048.	3.0	3
41	ESD Protection Design of High-Linearity SPDT CMOS T/R Switch for Cellular Applications. , 2019, , .		2
42	ESD Protection Design With Diode-Triggered Quad-SCR for Separated Power Domains. IEEE Transactions on Device and Materials Reliability, 2019, 19, 283-289.	2.0	4
43	An 82.9%-Efficiency Triple-Output Battery Management Unit for Implantable Neuron Stimulator in 180-nm Standard CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 788-792.	3.0	8
44	Optimization Design on Active Guard Ring to Improve Latch-Up Immunity of CMOS Integrated Circuits. IEEE Transactions on Electron Devices, 2019, 66, 1648-1655.	3.0	10
45	Design and In Vivo Verification of a CMOS Bone-Guided Cochlear Implant Microsystem. IEEE Transactions on Biomedical Engineering, 2019, 66, 3156-3167.	4.2	15
46	Design of Power-Rail ESD Clamp With Dynamic Timing-Voltage Detection Against False Trigger During Fast Power-ON Events. IEEE Transactions on Electron Devices, 2018, 65, 838-846.	3.0	14
47	A High-Voltage-Tolerant and Power-Efficient Stimulator With Adaptive Power Supply Realized in Low-Voltage CMOS Process for Implantable Biomedical Applications. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 178-186.	3.6	27
48	Self-Reset Transient Detection Circuit for On-Chip Protection Against System-Level Electrical-Transient Disturbance. IEEE Transactions on Device and Materials Reliability, 2018, 18, 114-121.	2.0	2
49	Comparison Between High-Holding-Voltage SCR and Stacked Low-Voltage Devices for ESD Protection in High-Voltage Applications. IEEE Transactions on Electron Devices, 2018, 65, 798-802.	3.0	26
50	Design of Multi-Channel Monopolar Biphasic Stimulator for Implantable Biomedical Applications. , 2018, , .		7
51	On-Chip Transient Detection Circuit for Microelectronic Systems Against Electrical Transient Disturbances due to ESD Events. , 2018, , .		1
52	On-Chip HBM and HMM ESD Protection Design for RF Applications in 40-nm CMOS Process. IEEE Transactions on Electron Devices, 2018, 65, 5267-5274.	3.0	12
53	Power-Rail ESD Clamp Circuit with Polysilicon Diodes Against False Trigger During Fast Power-on Events. , 2018, , .		3
54	Design of Multiple-Charge-Pump System for Implantable Biomedical Applications. , 2018, , .		12

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55	Study on Latchup Path between HV-LDMOS and LV-CMOS in a 0.16-Î¼m 30-V/1.8-V BCD Technology. , 2018, , .		3
56	Surge protection design with surge-to-digital converter for microelectronic circuits and systems. Microelectronics Reliability, 2018, 88-90, 2-5.	1.7	0
57	A Fully Integrated 16-Channel Closed-Loop Neural-Prosthetic CMOS SoC With Wireless Power and Bidirectional Data Telemetry for Real-Time Efficient Human Epileptic Seizure Control. IEEE Journal of Solid-State Circuits, 2018, 53, 3314-3326.	5.4	92
58	Improving Safe-Operating-Area of a 5-V n-Channel Large Array MOSFET in a 0.15-<inline-formula> <tex-math notation="LaTeX">mu </tex-math> </inline-formula>m BCD Process. IEEE Transactions on Electron Devices, 2018, 65, 2948-2956.	3.0	5
59	ESD Protection Design for Touch Panel Control IC Against Latchup-Like Failure Induced by System-Level ESD Test. IEEE Transactions on Electron Devices, 2017, 64, 642-645.	3.0	15
60	Design considerations and clinical applications of closed-loop neural disorder control SoCs. , 2017, , .		4
61	A CMOS-Process-Compatible Low-Voltage Junction-FET With Adjustable Pinch-Off Voltage. IEEE Transactions on Electron Devices, 2017, 64, 2812-2819.	3.0	4
62	Regulated Charge Pump With New Clocking Scheme for Smoothing the Charging Current in Low Voltage CMOS Process. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 528-536.	5.4	20
63	ESD protection design on T/R switch with embedded SCR in CMOS process. , 2017, , .		3
64	Design of 2.4-GHz T/R switch with embedded ESD protection devices in CMOS process. Microelectronics Reliability, 2017, 78, 258-266.	1.7	0
65	A Digitally Dynamic Power Supply Technique for 16-Channel 12 V-Tolerant Stimulator Realized in a 0.18-Î¼m 1.8-V/3.3-V Low-Voltage CMOS Process. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 1087-1096.	4.0	23
66	System-Level ESD Protection for Automotive Electronics by Co-Design of TVS and CAN Transceiver Chips. IEEE Transactions on Device and Materials Reliability, 2017, 17, 570-576.	2.0	8
67	On-Chip ESD Protection Device for High-Speed I/O Applications in CMOS Technology. IEEE Transactions on Electron Devices, 2017, 64, 3979-3985.	3.0	25
68	Investigation of Unexpected Latchup Path Between HV-LDMOS and LV-CMOS in a 0.25- $mu ext{m}$ 60-V/5-V BCD Technology. IEEE Transactions on Electron Devices, 2017, 64, 3519-3523.	3.0	10
69	A bone-guided cochlear implant CMOS microsystem preserving acoustic hearing. , 2017, , .		14
70	ESD-induced latchup-like failure in a touch panel control IC. , 2017, , .		1
71	Low-trigger ESD protection design with latch-up immunity for 5-V CMOS application by drain engineering. , 2017, , .		2
72	New on-chip transient detection circuit to improve electromagnetic susceptibility of microelectronic systems. , 2017, , .		0

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73	A fully integrated closed-loop neuromodulation SoC with wireless power and bi-directional data telemetry for real-time human epileptic seizure control. , 2017, , .		17
74	ESD Protection Design with Low-Leakage Consideration for Silicon Chips of IoT Applications. , 2017, , .		0
75	A 8 Phases 192MHz Crystal-Less Clock Generator with PVT Calibration. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2017, E100.A, 275-282.	0.3	0
76	An Ultra-Low Voltage CMOS Voltage Controlled Oscillator with Process and Temperature Compensation. IEICE Transactions on Electronics, 2017, E100.C, 675-683.	0.6	0
77	Optimization of Guard Ring Structures to Improve Latchup Immunity in an 18 V DDDMOS Process. IEEE Transactions on Electron Devices, 2016, 63, 2449-2454.	3.0	7
78	ESD protection design for high-speed applications in CMOS technology. , 2016, , .		3
79	ESD Protection Design With Stacked High-Holding-Voltage SCR for High-Voltage Pins in a Battery-Monitoring IC. IEEE Transactions on Electron Devices, 2016, 63, 1996-2002.	3.0	25
80	ESD self-protection design on 2.4-GHz T/R switch for RF application in CMOS process. , 2016, , .		3
81	Quad-SCR Device for Cross-Domain ESD Protection. IEEE Transactions on Electron Devices, 2016, 63, 3177-3184.	3.0	3
82	A 70nW, 0.3V temperature compensation voltage reference consisting of subthreshold MOSFETs in 65nm CMOS technology. , 2016, , .		5
83	Investigation of Human-Body-Model and Machine-Model ESD Robustness on Stacked Low-Voltage Field-Oxide Devices for High-Voltage Applications. IEEE Transactions on Electron Devices, 2016, , 1-6.	3.0	4
84	On-chip ESD protection design for HV integrated circuits. , 2016, , .		0
85	Design of high-voltage-tolerant level shifter in low voltage CMOS process for neuro stimulator. , 2016, , .		3
86	Low-Leakage Bidirectional SCR With Symmetrical Trigger Circuit for ESD Protection in 40-nm CMOS Process. IEEE Transactions on Device and Materials Reliability, 2016, 16, 549-555.	2.0	3
87	A High-Voltage-Tolerant and Precise Charge-Balanced Neuro-Stimulator in Low Voltage CMOS Process. IEEE Transactions on Biomedical Circuits and Systems, 2016, 10, 1087-1099.	4.0	48
88	Area-Efficient and Low-Leakage Diode String for On-Chip ESD Protection. IEEE Transactions on Electron Devices, 2016, 63, 531-536.	3.0	22
89	Study on the ESD-induced gate-oxide breakdown and the protection solution in 28nm high-k metal-gate CMOS technology. , 2015, , .		9
90	ESD protection design with stacked low-voltage devices for high-voltage pins of battery-monitoring IC. , 2015, , .		4

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91	Area-Efficient ESD Clamp Circuit With a Capacitance-Boosting Technique to Minimize Standby Leakage Current. IEEE Transactions on Device and Materials Reliability, 2015, 15, 156-162.	2.0	9
92	Stacked low-voltage PMOS for high-voltage ESD protection with latchup-free immunity. , 2015, , .		2
93	Latch-Up Protection Design With Corresponding Complementary Current to Suppress the Effect of External Current Triggers. IEEE Transactions on Device and Materials Reliability, 2015, 15, 242-249.	2.0	5
94	Vertical SCR structure for on-chip ESD protection in nanoscale CMOS technology. , 2015, , .		0
95	Impact of guard ring layout on the stacked low-voltage PMOS for high-voltage ESD protection. , 2015, , .		1
96	ESD protection design with latchup-free immunity in 120V SOI process. , 2015, , .		1
97	Active ESD protection for input transistors in a 40-nm CMOS process. , 2015, , .		4
98	Improve latch-up immunity by circuit solution. , 2015, , .		0
99	Compensation circuit with additional junction sensor to enhance latchup immunity for CMOS integrated circuits. , 2015, , .		0
100	Power-rail ESD clamp circuit with embedded-trigger SCR device in a 65-nm CMOS process. , 2014, , .		3
101	Active Guard Ring to Improve Latch-Up Immunity. IEEE Transactions on Electron Devices, 2014, 61, 4145-4152.	3.0	15
102	Study on ESD protection design with stacked low-voltage devices for high-voltage applications. , 2014, , .		11
103	Local CDM ESD Protection Circuits for Cross-Power Domains in 3D IC Applications. IEEE Transactions on Device and Materials Reliability, 2014, 14, 781-783.	2.0	6
104	ESD protection design for wideband RF applications in 65-nm CMOS process. , 2014, , .		1
105	Through Diffusion Tensor Magnetic Resonance Imaging to Evaluate the Original Properties of Neural Pathways of Patients with Partial Seizures and Secondary Generalization by Individual Anatomic Reference Atlas. BioMed Research International, 2014, 2014, 1-8.	1.9	2
106	Improving ESD robustness of stacked diodes with embedded SCR for RF applications in 65-nm CMOS. , 2014, , .		11
107	A high-voltage-tolerant stimulator realized in the low-voltage CMOS process for cochlear implant. , 2014, , .		2
108	Layout Consideration and Circuit Solution to Prevent EOS Failure Induced by Latchup Test in a High-Voltage Integrated Circuits. IEEE Transactions on Device and Materials Reliability, 2014, 14, 493-498.	2.0	7

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109	On the Design of Power-Rail ESD Clamp Circuits With Gate Leakage Consideration in Nanoscale CMOS Technology. IEEE Transactions on Device and Materials Reliability, 2014, 14, 536-544.	2.0	9
110	Design of high-voltage-tolerant stimulus driver with adaptive loading consideration to suppress epileptic seizure in a 0.18-Î¼m CMOS process. Analog Integrated Circuits and Signal Processing, 2014, 79, 219-226.	1.4	6
111	On-Chip Transient Voltage Suppressor Integrated With Silicon-Based Transceiver IC for System-Level ESD Protection. IEEE Transactions on Industrial Electronics, 2014, 61, 5615-5621.	7.9	14
112	A Fully Integrated 8-Channel Closed-Loop Neural-Prosthetic CMOS SoC for Real-Time Epileptic Seizure Control. IEEE Journal of Solid-State Circuits, 2014, 49, 232-247.	5.4	218
113	SCR-based transient detection circuit for on-chip protection design against system-level electrical transient disturbance. Microelectronics Reliability, 2014, 54, 71-78.	1.7	0
114	Metal-layer capacitors in the 65 nm CMOS process and the application for low-leakage power-rail ESD clamp circuit. Microelectronics Reliability, 2014, 54, 64-70.	1.7	33
115	Design of $2 imes {m V}_{m DD}$-Tolerant I/O Buffer With PVT Compensation Realized by Only $1 imes {m V}_{m DD}$ Thin-Oxide Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2549-2560.	5.4	27
116	PMOS-based power-rail ESD clamp circuit with adjustable holding voltage controlled by ESD detection circuit. Microelectronics Reliability, 2013, 53, 208-214.	1.7	0
117	Large-Swing-Tolerant ESD Protection Circuit for Gigahertz Power Amplifier in a 65-nm CMOS Process. IEEE Transactions on Microwave Theory and Techniques, 2013, 61, 914-921.	4.6	3
118	Robust ESD Protection Design for 40-Gb/s Transceiver in 65-nm CMOS Process. IEEE Transactions on Electron Devices, 2013, 60, 3625-3631.	3.0	7
119	Low-leakage power-rail ESD clamp circuit with gated current mirror in a 65-nm CMOS technology. , 2013, , .		2
120	A Latchup-Immune and Robust SCR Device for ESD Protection in 0.25-Î¼m 5-V CMOS Process. IEEE Electron Device Letters, 2013, 34, 674-676.	3.9	34
121	Area-efficient power-rail ESD clamp circuit with SCR device embedded into ESD-transient detection circuit in a 65nm CMOS process. , 2013, , .		1
122	SCR device for on-chip ESD protection in RF power amplifier. , 2013, , .		0
123	Implantable Stimulator for Epileptic Seizure Suppression With Loading Impedance Adaptability. IEEE Transactions on Biomedical Circuits and Systems, 2013, 7, 196-203.	4.0	32
124	Design of 2×V<inf>DD</inf> logic gates with only 1×V<inf>DD</inf> devices in nanoscale CMOS technology. , 2013, , .		0
125	Ultra-low-leakage power-rail ESD clamp circuit in a 65-nm CMOS technology. , 2013, , .		3
126	Investigation on safe operating area and ESD robustness in a 60-V BCD process with different deep P-Well test structures. , 2013, , .		4

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127	High Area-Efficient ESD Clamp Circuit With Equivalent RC-Based Detection Mechanism in a 65-nm CMOS Process. IEEE Transactions on Electron Devices, 2013, 60, 1011-1018.	3.0	11
128	Design of Dual-Band ESD Protection for 24-/60-GHz Millimeter-Wave Circuits. IEEE Transactions on Device and Materials Reliability, 2013, 13, 110-118.	2.0	4
129	Self-protected LDMOS output device with embedded SCR to improve ESD robustness in 0.25-μm 60-V BCD process. , 2013, , .		11
130	Analysis and solution to overcome EOS failure induced by latchup test in a high-voltage integrated circuits. , 2013, , .		1
131	ESD protection design for radio-frequency integrated circuits in nanoscale CMOS technology. , 2013, , .		0
132	Resistor-less power-rail ESD clamp circuit with ultra-low leakage current in 65nm CMOS process. , 2013, , .		2
133	Power-Rail ESD Clamp Circuit With Diode-String ESD Detection to Overcome the Gate Leakage Current in a 40-nm CMOS Process. IEEE Transactions on Electron Devices, 2013, 60, 3500-3507.	3.0	34
134	25.2:Invited Paper: ESD and EOS Impacts during Module Assembly Processes for Display Panels. Digest of Technical Papers SID International Symposium, 2013, 44, 302-305.	0.3	0
135	Resistor-Less Design of Power-Rail ESD Clamp Circuit in Nanoscale CMOS Technology. IEEE Transactions on Electron Devices, 2012, 59, 3456-3463.	3.0	10
136	Foreword for the Special Issue on ESD Technology. IEEE Transactions on Device and Materials Reliability, 2012, 12, 588-588.	2.0	0
137	Characterization of SOA in Time Domain and the Improvement Techniques for Using in High-Voltage Integrated Circuits. IEEE Transactions on Device and Materials Reliability, 2012, 12, 382-390.	2.0	22
138	New 4-Bit Transient-to-Digital Converter for System-Level ESD Protection in Display Panels. IEEE Transactions on Industrial Electronics, 2012, 59, 1278-1287.	7.9	11
139	ESD Protection Design for 60-GHz LNA With Inductor-Triggered SCR in 65-nm CMOS Process. IEEE Transactions on Microwave Theory and Techniques, 2012, 60, 714-723.	4.6	20
140	Live demonstration: Implantable stimulator for epileptic seizure suppression with loading impedance adaptability. , 2012, , .		0
141	Failure analysis on gate-driven ESD clamp circuit after TLP stresses of different voltage steps in a 16-V CMOS process. , 2012, , .		2
142	Design of negative high voltage generator for biphasic stimulator with soc integration consideration. , 2012, , .		4
143	Diode-Triggered Silicon-Controlled Rectifier With Reduced Voltage Overshoot for CDM ESD Protection. IEEE Transactions on Device and Materials Reliability, 2012, 12, 10-14.	2.0	36
144	High-voltage-tolerant stimulator with adaptive loading consideration for electronic epilepsy prosthetic SoC in a 0.18-µm CMOS process. , 2012, , .		9

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145	Design of ESD protection for RF CMOS power amplifier with inductor in matching network. , 2012, , .		3
146	Power-Rail ESD Clamp Circuit With Ultralow Standby Leakage Current and High Area Efficiency in Nanometer CMOS Technology. IEEE Transactions on Electron Devices, 2012, 59, 2626-2634.	3.0	7
147	New design of transient-noise detection circuit with SCR device for system-level ESD protection. , 2012, , .		1
148	Design of AC-coupled circuit for high-speed interconnects. , 2012, , .		3
149	Investigation on CDM ESD events at core circuits in a 65-nm CMOS process. Microelectronics Reliability, 2012, 52, 2627-2631.	1.7	3
150	Design of Compact ESD Protection Circuit for V-Band RF Applications in a 65-nm CMOS Technology. IEEE Transactions on Device and Materials Reliability, 2012, 12, 554-561.	2.0	4
151	Study of intrinsic characteristics of ESD protection diodes for high-speed I/O applications. Microelectronics Reliability, 2012, 52, 1020-1030.	1.7	3
152	New Design of 2 $imes$ VDD-Tolerant Power-Rail ESD Clamp Circuit for Mixed-Voltage I/O Buffers in 65-nm CMOS Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 178-182.	3.0	14
153	New Low-Leakage Power-Rail ESD Clamp Circuit in a 65-nm Low-Voltage CMOS Process. IEEE Transactions on Device and Materials Reliability, 2011, 11, 474-483.	2.0	10
154	ESD protection consideration in nanoscale CMOS technology. , 2011, , .		5
155	Design and implementation of capacitive sensor readout circuit on glass substrate for touch panel applications. , 2011, , .		5
156	Design of power-rail ESD clamp circuit with adjustable holding voltage against mis-trigger or transient-induced latch-on events. , 2011, , .		2
157	New transient detection circuit to detect ESD-induced disturbance for automatic recovery design in display panels. , 2011, , .		0
158	ESD-aware circuit design in CMOS integrated circuits to meet system-level ESD specification in microelectronic systems. , 2011, , .		2
159	Overview on ESD Protection Designs of Low-Parasitic Capacitance for RF ICs in CMOS Technologies. IEEE Transactions on Device and Materials Reliability, 2011, 11, 207-218.	2.0	50
160	Design of Integrated Gate Driver With Threshold Voltage Drop Cancellation in Amorphous Silicon Technology for TFT-LCD Application. Journal of Display Technology, 2011, 7, 657-664.	1.2	35
161	Electrostatic Discharge Protection Design for High-Voltage Programming Pin in Fully-Silicided CMOS ICs. IEEE Journal of Solid-State Circuits, 2011, 46, 537-545.	5.4	1
162	Pâ€49: Design of Digital Timeâ€Modulation Pixel Memory Circuit on Glass Substrate for Low Power Application. Digest of Technical Papers SID International Symposium, 2011, 42, 1281-1284.	0.3	1

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163	Improving Safe Operating Area of nLDMOS Array With Embedded Silicon Controlled Rectifier for ESD Protection in a 24-V BCD Process. IEEE Transactions on Electron Devices, 2011, 58, 2944-2951.	3.0	37
164	Design to suppress return-back leakage current of charge pump circuit in low-voltage CMOS process. Microelectronics Reliability, 2011, 51, 871-878.	1.7	3
165	Layout styles to improve CDM ESD robustness of integrated circuits in 65-nm CMOS process. , 2011, , .		5
166	Design of low-leakage power-rail ESD clamp circuit with MOM capacitor and STSCR in a 65-nm CMOS process. , 2011, , .		7
167	Adaptable stimulus driver for epileptic seizure suppression. , 2011, , .		3
168	Stimulus driver for epilepsy seizure suppression with adaptive loading impedance. Journal of Neural Engineering, 2011, 8, 066008.	3.5	10
169	Impact of shielding line on CDM ESD robustness of core circuits in a 65-nm CMOS process. , 2011, , .		1
170	Transient-to-digital converter to detect electrical fast transient (EFT) disturbance for system protection design. , 2011, , .		1
171	P-178: Design of On-Panel Readout Circuit for Touch Panel Application. Digest of Technical Papers SID International Symposium, 2010, 41, 1933.	0.3	5
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