Ming-Dou Ker

List of Publications by Year
in descending order

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433	5,033	147801	189892
papers	citations	31 h-index	50 g-index

434	434	434	1484
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI. IEEE Transactions on Electron Devices, 1999, 46, 173-183.	3.0	263
2	A Fully Integrated 8-Channel Closed-Loop Neural-Prosthetic CMOS SoC for Real-Time Epileptic Seizure Control. IEEE Journal of Solid-State Circuits, 2014, 49, 232-247.	5.4	218
3	Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits. IEEE Transactions on Device and Materials Reliability, 2005, 5, 235-249.	2.0	191
4	Design of Charge Pump Circuit With Consideration of Gate-Oxide Reliability in Low-Voltage CMOS Processes. IEEE Journal of Solid-State Circuits, 2006, 41, 1100-1107.	5.4	177
5	A Fully Integrated 16-Channel Closed-Loop Neural-Prosthetic CMOS SoC With Wireless Power and Bidirectional Data Telemetry for Real-Time Efficient Human Epileptic Seizure Control. IEEE Journal of Solid-State Circuits, 2018, 53, 3314-3326.	5.4	92
6	Investigation of the gate-driven effect and substrate-triggered effect on ESD robustness of CMOS devices. IEEE Transactions on Device and Materials Reliability, 2001, 1, 190-203.	2.0	80
7	Complementary-LVTSCR ESD protection circuit for submicron CMOS VLSI/ULSI. IEEE Transactions on Electron Devices, 1996, 43, 588-598.	3.0	62
8	A gate-coupled PTLSCR/NTLSCR ESD protection circuit for deep-submicron low-voltage CMOS ICs. IEEE Journal of Solid-State Circuits, 1997, 32, 38-51.	5.4	62
9	Methodology on extracting compact layout rules for latchup prevention in deep-submicron bulk CMOS technology. IEEE Transactions on Semiconductor Manufacturing, 2003, 16, 319-334.	1.7	59
10	Capacitor-couple ESD protection circuit for deep-submicron low-voltage CMOS ASIC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 1996, 4, 307-321.	3.1	55
11	ESD protection design on analog pin with very low input capacitance for high-frequency or current-mode applications. IEEE Journal of Solid-State Circuits, 2000, 35, 1194-1199.	5.4	54
12	Overview on ESD Protection Designs of Low-Parasitic Capacitance for RF ICs in CMOS Technologies. IEEE Transactions on Device and Materials Reliability, 2011, 11, 207-218.	2.0	50
13	Investigation and Design of On-Chip Power-Rail ESD Clamp Circuits Without Suffering Latchup-Like Failure During System-Level ESD Test. IEEE Journal of Solid-State Circuits, 2008, 43, 2533-2545.	5.4	48
14	A High-Voltage-Tolerant and Precise Charge-Balanced Neuro-Stimulator in Low Voltage CMOS Process. IEEE Transactions on Biomedical Circuits and Systems, 2016, 10, 1087-1099.	4.0	48
15	A new Schmitt trigger circuit in a 0.13-/spl mu/m 1/2.5-V CMOS process to receive 3.3-V input signals. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2005, 52, 361-365.	2.2	46
16	Design on the low-leakage diode string for using in the power-rail ESD clamp circuits in a 0.35-/spl mu/m silicide CMOS process. IEEE Journal of Solid-State Circuits, 2000, 35, 601-611.	5.4	45
17	Modeling the positive-feedback regenerative process of CMOS latchup by a positive transient pole method. I. theoretical derivation. IEEE Transactions on Electron Devices, 1995, 42, 1141-1148.	3.0	43
18	The impact of low-holding-voltage issue in high-voltage CMOS technology and the design of latchup-free power-rail ESD clamp circuit for LCD driver ICs. IEEE Journal of Solid-State Circuits, 2005, 40, 1751-1759.	5.4	41

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19	Substrate-triggered SCR device for on-chip ESD protection in fully silicided sub-0.25-Î¼m CMOS process. IEEE Transactions on Electron Devices, 2003, 50, 397-405.	3.0	39
20	Latchup-free esd protection design with complementary substrate-triggered scr devices. IEEE Journal of Solid-State Circuits, 2003, 38, 1380-1392.	5.4	39
21	New Curvature-Compensation Technique for CMOS Bandgap Reference with Sub-1-V Operation. , 0, , .		37
22	Low-Capacitance SCR With Waffle Layout Structure for On-Chip ESD Protection in RF ICs. IEEE Transactions on Microwave Theory and Techniques, 2008, 56, 1286-1294.	4.6	37
23	Improving Safe Operating Area of nLDMOS Array With Embedded Silicon Controlled Rectifier for ESD Protection in a 24-V BCD Process. IEEE Transactions on Electron Devices, 2011, 58, 2944-2951.	3.0	37
24	Diode-Triggered Silicon-Controlled Rectifier With Reduced Voltage Overshoot for CDM ESD Protection. IEEE Transactions on Device and Materials Reliability, 2012, 12, 10-14.	2.0	36
25	Double Snapback Characteristics in High-Voltage nMOSFETs and the Impact to On-Chip ESD Protection Design. IEEE Electron Device Letters, 2004, 25, 640-642.	3.9	35
26	Design of Integrated Gate Driver With Threshold Voltage Drop Cancellation in Amorphous Silicon Technology for TFT-LCD Application. Journal of Display Technology, 2011, 7, 657-664.	1.2	35
27	A Latchup-Immune and Robust SCR Device for ESD Protection in 0.25-Î¼m 5-V CMOS Process. IEEE Electron Device Letters, 2013, 34, 674-676.	3.9	34
28	Power-Rail ESD Clamp Circuit With Diode-String ESD Detection to Overcome the Gate Leakage Current in a 40-nm CMOS Process. IEEE Transactions on Electron Devices, 2013, 60, 3500-3507.	3.0	34
29	SCR Device With Dynamic Holding Voltage for On-Chip ESD Protection in a 0.25-<tex>$mu hbox m$</tex>Fully Salicided CMOS Process. IEEE Transactions on Electron Devices, 2004, 51, 1731-1733.	3.0	33
30	ESD Protection Design With Lateral DMOS Transistor in 40-V BCD Technology. IEEE Transactions on Electron Devices, 2010, 57, 3395-3404.	3.0	33
31	Metal-layer capacitors in the 65 nm CMOS process and the application for low-leakage power-rail ESD clamp circuit. Microelectronics Reliability, 2014, 54, 64-70.	1.7	33
32	Lateral SCR devices with low-voltage high-current triggering characteristics for output ESD protection in submicron CMOS technology. IEEE Transactions on Electron Devices, 1998, 45, 849-860.	3.0	32
33	Implantable Stimulator for Epileptic Seizure Suppression With Loading Impedance Adaptability. IEEE Transactions on Biomedical Circuits and Systems, 2013, 7, 196-203.	4.0	32
34	Analysis on the dependence of layout parameters on ESD robustness of CMOS devices for manufacturing in deep-submicron CMOS process. IEEE Transactions on Semiconductor Manufacturing, 2003, 16, 486-500.	1.7	31
35	On-Chip Transient Detection Circuit for System-Level ESD Protection in CMOS Integrated Circuits to Meet Electromagnetic Compatibility Regulation. IEEE Transactions on Electromagnetic Compatibility, 2008, 50, 13-21.	2.2	30
36	Design of Power-Rail ESD Clamp Circuit With Ultra-Low Standby Leakage Current in Nanoscale CMOS Technology. IEEE Journal of Solid-State Circuits, 2009, 44, 956-964.	5.4	30

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37	SCR Device Fabricated With Dummy-Gate Structure to Improve Turn-On Speed for Effective ESD Protection in CMOS Technology. IEEE Transactions on Semiconductor Manufacturing, 2005, 18, 320-327.	1.7	28
38	ESD Protection Design With On-Chip ESD Bus and High-Voltage-Tolerant ESD Clamp Circuit for Mixed-Voltage I/O Buffers. IEEE Transactions on Electron Devices, 2008, 55, 1409-1416.	3.0	27
39	Optimization on Layout Style of ESD Protection Diode for Radio-Frequency Front-End and High-Speed I/O Interface Circuits. IEEE Transactions on Device and Materials Reliability, 2010, 10, 238-246.	2.0	27
40	Design of $2 imes {m V}_{m DD}$-Tolerant I/O Buffer With PVT Compensation Realized by Only $1 imes {m V}_{m DD}$ Thin-Oxide Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2549-2560.	5.4	27
41	A High-Voltage-Tolerant and Power-Efficient Stimulator With Adaptive Power Supply Realized in Low-Voltage CMOS Process for Implantable Biomedical Applications. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 178-186.	3.6	27
42	Cascoded LVTSCR with tunable holding voltage for ESD protection in bulk CMOS technology without latchup danger. Solid-State Electronics, 2000, 44, 425-445.	1.4	26
43	Hardware/firmware co-design in an 8-bits microcontroller to solve the system-level ESD issue on keyboard. Microelectronics Reliability, 2001, 41, 417-429.	1.7	26
44	Implementation of Initial-On ESD Protection Concept With PMOS-Triggered SCR Devices in Deep-Submicron CMOS Technology. IEEE Journal of Solid-State Circuits, 2007, 42, 1158-1168.	5.4	26
45	Ultra-High-Voltage Charge Pump Circuit in Low-Voltage Bulk CMOS Processes With Polysilicon Diodes. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 47-51.	2.2	26
46	Comparison Between High-Holding-Voltage SCR and Stacked Low-Voltage Devices for ESD Protection in High-Voltage Applications. IEEE Transactions on Electron Devices, 2018, 65, 798-802.	3.0	26
47	ESD protection design for CMOS RF integrated circuits using polysilicon diodes. Microelectronics Reliability, 2002, 42, 863-872.	1.7	25
48	ESD Implantations for On-Chip ESD Protection With Layout Consideration in 0.18-<tex>$muhbox m$</tex>Salicided CMOS Technology. IEEE Transactions on Semiconductor Manufacturing, 2005, 18, 328-337.	1.7	25
49	New Layout Arrangement to Improve ESD Robustness of Large-Array High-Voltage nLDMOS. IEEE Electron Device Letters, 2010, 31, 159-161.	3.9	25
50	ESD Protection Design With Stacked High-Holding-Voltage SCR for High-Voltage Pins in a Battery-Monitoring IC. IEEE Transactions on Electron Devices, 2016, 63, 1996-2002.	3.0	25
51	On-Chip ESD Protection Device for High-Speed I/O Applications in CMOS Technology. IEEE Transactions on Electron Devices, 2017, 64, 3979-3985.	3.0	25
52	Overview on electrostatic discharge protection designs for mixed-voltage I/O interfaces: design concept and circuit implementations. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 235-246.	0.1	24
53	An Efficient, Wide-Output, High-Voltage Charge Pump With a Stage Selection Circuit Realized in a Low-Voltage CMOS Process. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3437-3444.	5.4	24
54	SCR device with double-triggered technique for on-chip ESD protection in sub-quarter-micron silicided CMOS processes. IEEE Transactions on Device and Materials Reliability, 2003, 3, 58-68.	2.0	23

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55	Design on mixed-voltage-tolerant I/O interface with novel tracking circuits in a 0.13-Î¼m CMOS technology. , 0, , .		23
56	Evaluation on Board-Level Noise Filter Networks to Suppress Transient-Induced Latchup in CMOS ICs Under System-Level ESD Test. IEEE Transactions on Electromagnetic Compatibility, 2006, 48, 161-171.	2.2	23
57	High-Voltage-Tolerant ESD Clamp Circuit With Low Standby Leakage in Nanoscale CMOS Process. IEEE Transactions on Electron Devices, 2010, 57, 1636-1641.	3.0	23
58	A Digitally Dynamic Power Supply Technique for 16-Channel 12 V-Tolerant Stimulator Realized in a 0.18-Î¼m 1.8-V/3.3-V Low-Voltage CMOS Process. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 1087-1096.	4.0	23
59	ESD test methods on integrated circuits: an overview. , 0, , .		22
60	Electrostatic discharge protection design for mixed-voltage CMOS I/O buffers. IEEE Journal of Solid-State Circuits, 2002, 37, 1046-1055.	5.4	22
61	CMOS chip as luminescent sensor for biochemical reactions. IEEE Sensors Journal, 2003, 3, 310-316.	4.7	22
62	An Output Buffer for 3.3-V Applications in a 0.13-<formula formulatype="inline"><tex>$muhbox{m}$</tex></formula> 1/2.5-V CMOS Process. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 14-18.	2.2	22
63	Investigation on the Validity of Holding Voltage in High-Voltage Devices Measured by Transmission-Line-Pulsing (TLP). IEEE Electron Device Letters, 2008, 29, 762-764.	3.9	22
64	Characterization of SOA in Time Domain and the Improvement Techniques for Using in High-Voltage Integrated Circuits. IEEE Transactions on Device and Materials Reliability, 2012, 12, 382-390.	2.0	22
65	Area-Efficient and Low-Leakage Diode String for On-Chip ESD Protection. IEEE Transactions on Electron Devices, 2016, 63, 531-536.	3.0	22
66	On-chip ESD protection design by using polysilicon diodes in CMOS process. IEEE Journal of Solid-State Circuits, 2001, 36, 676-686.	5.4	21
67	Active ESD Protection Design for Interface Circuits Between Separated Power Domains Against Cross-Power-Domain ESD Stresses. IEEE Transactions on Device and Materials Reliability, 2008, 8, 549-560.	2.0	21
68	ESD protection to overcome internal gate oxide damage on digital-analog interface of mixed-mode CMOS IC's. , 0, , .		20
69	Novel input ESD protection circuit with substrate-triggering technique in a 0.25-Î¼m shallow-trench-isolation CMOS technology. , 0, , .		20
70	Substrate-triggered technique for on-chip ESD protection design in a 0.18-Î¼m salicided CMOS process. IEEE Transactions on Electron Devices, 2003, 50, 1050-1057.	3.0	20
71	ESD protection design for 1- to 10-GHz distributed amplifier in CMOS technology. IEEE Transactions on Microwave Theory and Techniques, 2005, 53, 2672-2681.	4.6	20
72	Capacitor-Less Design of Power-Rail ESD Clamp Circuit With Adjustable Holding Voltage for On-Chip ESD Protection. IEEE Journal of Solid-State Circuits, 2010, , .	5.4	20

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73	ESD Protection Design for 60-GHz LNA With Inductor-Triggered SCR in 65-nm CMOS Process. IEEE Transactions on Microwave Theory and Techniques, 2012, 60, 714-723.	4.6	20
74	Regulated Charge Pump With New Clocking Scheme for Smoothing the Charging Current in Low Voltage CMOS Process. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 528-536.	5.4	20
75	Optimization of broadband RF performance and ESD robustness by -model distributed ESD protection scheme. Journal of Electrostatics, 2006, 64, 80-87.	1.9	19
76	Area-Efficient ESD-Transient Detection Circuit With Smaller Capacitance for On-Chip Power-Rail ESD Protection in CMOS ICs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 359-363.	3.0	19
77	Monopolar Biphasic Stimulator With Discharge Function and Negative Level Shifter for Neuromodulation SoC Integration in Low-Voltage CMOS Process. IEEE Transactions on Biomedical Circuits and Systems, 2021, 15, 568-579.	4.0	19
78	How to safely apply the LVTSCR for CMOS whole-chip ESD protection without being accidentally triggered on. Journal of Electrostatics, 1999, 47, 215-248.	1.9	18
79	Design on mixed-voltage I/O buffers with slew-rate control in low-voltage CMOS process. , 2008, , .		18
80	Optimization on MOS-Triggered SCR Structures for On-Chip ESD Protection. IEEE Transactions on Electron Devices, 2009, 56, 1466-1472.	3.0	18
81	Transient-to-Digital Converter for System-Level Electrostatic Discharge Protection in CMOS ICs. IEEE Transactions on Electromagnetic Compatibility, 2009, 51, 620-630.	2.2	18
82	A 5-GHz Differential Low-Noise Amplifier With High Pin-to-Pin ESD Robustness in a 130-nm CMOS Process. IEEE Transactions on Microwave Theory and Techniques, 2009, 57, 1044-1053.	4.6	18
83	ESD protection design for 900-MHz RF receiver with 8-kV HBM ESD robustness. , 0, , .		17
84	Design of 2.5 V/5 V mixed-voltage CMOS I/O buffer with only thin oxide device and dynamic N-well bias circuit. , 0, , .		17
85	A novel LC-tank ESD protection design for Giga-Hz RF circuits. , 0, , .		17
86	Decreasing-size distributed ESD protection scheme for broad-band RF circuits. IEEE Transactions on Microwave Theory and Techniques, 2005, 53, 582-589.	4.6	17
87	Transient-Induced Latchup in CMOS ICs Under Electrical Fast-Transient Test. IEEE Transactions on Device and Materials Reliability, 2009, 9, 255-264.	2.0	17
88	A fully integrated closed-loop neuromodulation SoC with wireless power and bi-directional data telemetry for real-time human epileptic seizure control. , 2017, , .		17
89	Complementary-SCR ESD protection circuit with interdigitated finger-type layout for input pads of submicron CMOS IC's. IEEE Transactions on Electron Devices, 1995, 42, 1297-1304.	3.0	16
90	On-Chip ESD Protection Design With Substrate-Triggered Technique for Mixed-Voltage I/O Circuits in Subquarter-Micrometer CMOS Process. IEEE Transactions on Electron Devices, 2004, 51, 1628-1635.	3.0	16

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91	Dependence of Device Structures on Latchup Immunity in a High-Voltage 40-V CMOS Process With Drain-Extended MOSFETs. IEEE Transactions on Electron Devices, 2007, 54, 840-851.	3.0	16
92	Design of High-Voltage-Tolerant ESD Protection Circuit in Low-Voltage CMOS Processes. IEEE Transactions on Device and Materials Reliability, 2009, 9, 49-58.	2.0	16
93	Fully process-compatible layout design on bond pad to improve wire bond reliability in CMOS ICs. IEEE Transactions on Components and Packaging Technologies, 2002, 25, 309-316.	1.3	15
94	The Effect of IEC-Like Fast Transients on <formula formulatype="inline"><tex Notation="TeX">RC</tex> </formula>-Triggered ESD Power Clamps. IEEE Transactions on Electron Devices, 2009, 56, 1204-1210.	3.0	15
95	Design of 2$imes$VDD-Tolerant Power-Rail ESD Clamp Circuit With Consideration of Gate Leakage Current in 65-nm CMOS Technology. IEEE Transactions on Electron Devices, 2010, 57, 1460-1465.	3.0	15
96	Circuit and Layout Co-Design for ESD Protection in Bipolar-CMOS-DMOS (BCD) High-Voltage Process. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1039-1047.	5.4	15
97	Active Guard Ring to Improve Latch-Up Immunity. IEEE Transactions on Electron Devices, 2014, 61, 4145-4152.	3.0	15
98	ESD Protection Design for Touch Panel Control IC Against Latchup-Like Failure Induced by System-Level ESD Test. IEEE Transactions on Electron Devices, 2017, 64, 642-645.	3.0	15
99	Design and In Vivo Verification of a CMOS Bone-Guided Cochlear Implant Microsystem. IEEE Transactions on Biomedical Engineering, 2019, 66, 3156-3167.	4.2	15
100	Design of a Bone-Guided Cochlear Implant Microsystem With Monopolar Biphasic Multiple Stimulations and Evoked Compound Action Potential Acquisition and Its In Vivo Verification. IEEE Journal of Solid-State Circuits, 2021, 56, 3062-3076.	5.4	15
101	Substrate-triggered ESD clamp devices for use in power-rail ESD clamp circuits. Solid-State Electronics, 2002, 46, 721-734.	1.4	14
102	ESD Protection Design to Overcome Internal Damage on Interface Circuits of a CMOS IC With Multiple Separated Power Pins. IEEE Transactions on Components and Packaging Technologies, 2004, 27, 445-451.	1.3	14
103	Design on ESD protection scheme for IC with power-down-mode operation. IEEE Journal of Solid-State Circuits, 2004, 39, 1378-1382.	5.4	14
104	Source-side engineering to increase holding voltage of LDMOS in a 0.5-m 16-V BCD technology to avoid latch-up failure. , 2009, , .		14
105	New Design of 2 $imes$ VDD-Tolerant Power-Rail ESD Clamp Circuit for Mixed-Voltage I/O Buffers in 65-nm CMOS Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 178-182.	3.0	14
106	On-Chip Transient Voltage Suppressor Integrated With Silicon-Based Transceiver IC for System-Level ESD Protection. IEEE Transactions on Industrial Electronics, 2014, 61, 5615-5621.	7.9	14
107	A bone-guided cochlear implant CMOS microsystem preserving acoustic hearing. , 2017, , .		14
108	Design of Power-Rail ESD Clamp With Dynamic Timing-Voltage Detection Against False Trigger During Fast Power-ON Events. IEEE Transactions on Electron Devices, 2018, 65, 838-846.	3.0	14

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109	Modeling the positive-feedback regenerative process of CMOS latchup by a positive transient pole method. II. Quantitative evaluation. IEEE Transactions on Electron Devices, 1995, 42, 1149-1155.	3.0	13
110	Substrate-triggered ESD protection circuit without extra process modification. IEEE Journal of Solid-State Circuits, 2003, 38, 295-302.	5.4	13
111	ESD-Protection Design With Extra Low-Leakage-Current Diode String for RF Circuits in SiGe BiCMOS Process. IEEE Transactions on Device and Materials Reliability, 2006, 6, 517-527.	2.0	13
112	Impact of MOSFET Gate-Oxide Reliability on CMOS Operational Amplifier in a 130-nm Low-Voltage Process. IEEE Transactions on Device and Materials Reliability, 2008, 8, 394-405.	2.0	13
113	Self-matched ESD cell in CMOS technology for 60-GHz broadband RF applications. , 2010, , .		13
114	Design on the low-capacitance bond pad for high-frequency I/O circuits in CMOS technology. IEEE Transactions on Electron Devices, 2001, 48, 2953-2956.	3.0	12
115	ESD implantation for subquarter-micron cmos technology to enhance ESD robustness. IEEE Transactions on Electron Devices, 2003, 50, 2126-2134.	3.0	12
116	Design of charge pump circuit in low-voltage CMOS process with suppressed return-back leakage current. , 2010, , .		12
117	On-Chip HBM and HMM ESD Protection Design for RF Applications in 40-nm CMOS Process. IEEE Transactions on Electron Devices, 2018, 65, 5267-5274.	3.0	12
118	Design of Multiple-Charge-Pump System for Implantable Biomedical Applications. , 2018, , .		12
119	Design of Stage-Selective Negative Voltage Generator to Improve On-Chip Power Conversion Efficiency for Neuron Stimulation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4122-4131.	5.4	12
120	Design of Dual-Mode Stimulus Chip With Built-In High Voltage Generator for Biomedical Applications. IEEE Transactions on Biomedical Circuits and Systems, 2020, 14, 961-970.	4.0	12
121	Schottky-Embedded Silicon-Controlled Rectifier With High Holding Voltage Realized in a 0.18-Î¼m Low-Voltage CMOS Process. IEEE Transactions on Electron Devices, 2021, 68, 1764-1771.	3.0	12
122	ESD protection design for I/O cells with embedded SCR structure as power-rail ESD clamp device in nanoscale CMOS technology. IEEE Journal of Solid-State Circuits, 2005, 40, 2329-2338.	5.4	11
123	The Impact of Drift Implant and Layout Parameters on ESD Robustness for On-Chip ESD Protection Devices in 40-V CMOS Technology. IEEE Transactions on Device and Materials Reliability, 2007, 7, 324-332.	2.0	11
124	On the design of power-rail esd clamp circuit with consideration of gate leakage current in 65-nm low-voltage CMOS process. , 2009, , .		11
125	New 4-Bit Transient-to-Digital Converter for System-Level ESD Protection in Display Panels. IEEE Transactions on Industrial Electronics, 2012, 59, 1278-1287.	7.9	11
126	High Area-Efficient ESD Clamp Circuit With Equivalent RC-Based Detection Mechanism in a 65-nm CMOS Process. IEEE Transactions on Electron Devices, 2013, 60, 1011-1018.	3.0	11

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127	Self-protected LDMOS output device with embedded SCR to improve ESD robustness in 0.25-μm 60-V BCD process. , 2013, , .		11
128	Study on ESD protection design with stacked low-voltage devices for high-voltage applications. , 2014, , .		11
129	Improving ESD robustness of stacked diodes with embedded SCR for RF applications in 65-nm CMOS. , 2014, , .		11
130	Layout design on multi-finger MOSFET for on-chip ESD protection circuits in a 0.18-Î¼m salicided CMOS process. , 0, , .		10
131	Design on latchup-free power-rail ESD clamp circuit in high-voltage CMOS ICs. , 2004, , .		10
132	The Impact of Inner Pickup on ESD Robustness of Multi-Finger NMOS in Nanoscale CMOS Technology. , 2006, , .		10
133	New Gate-Bias Voltage-Generating Technique With Threshold-Voltage Compensation for On-Glass Analog Circuits in LTPS Process. Journal of Display Technology, 2007, 3, 309-314.	1.2	10
134	Measurement on snapback holding voltage of high-voltage LDMOS for latch-up consideration. , 2008, , .		10
135	Low-capacitance ESD protection design for high-speed I/O interfaces in a 130-nm CMOS process. Microelectronics Reliability, 2009, 49, 650-659.	1.7	10
136	New Low-Leakage Power-Rail ESD Clamp Circuit in a 65-nm Low-Voltage CMOS Process. IEEE Transactions on Device and Materials Reliability, 2011, 11, 474-483.	2.0	10
137	Stimulus driver for epilepsy seizure suppression with adaptive loading impedance. Journal of Neural Engineering, 2011, 8, 066008.	3.5	10
138	Resistor-Less Design of Power-Rail ESD Clamp Circuit in Nanoscale CMOS Technology. IEEE Transactions on Electron Devices, 2012, 59, 3456-3463.	3.0	10
139	Investigation of Unexpected Latchup Path Between HV-LDMOS and LV-CMOS in a 0.25- $mu ext{m}$ 60-V/5-V BCD Technology. IEEE Transactions on Electron Devices, 2017, 64, 3519-3523.	3.0	10
140	Optimization Design on Active Guard Ring to Improve Latch-Up Immunity of CMOS Integrated Circuits. IEEE Transactions on Electron Devices, 2019, 66, 1648-1655.	3.0	10
141	Using Schottky Barrier Diode to Improve Latch-Up Immunity for CMOS ICs Operating With Negative Voltage Sources. IEEE Electron Device Letters, 2021, 42, 395-397.	3.9	10
142	ESD protection design for mixed-voltage I/O circuit with substrate-triggered technique in sub-quarter-micron CMOS process. , 0, , .		9
143	Investigation on Device Characteristics of MOSFET Transistor Placed Under Bond Pad for High-Pin-Count SOC Applications. IEEE Transactions on Components and Packaging Technologies, 2004, 27, 452-460.	1.3	9
144	Design on Mixed-Voltage I/O Buffers with Consideration of Hot-Carrier Reliability. , 2007, , .		9

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145	Impact of Gate Leakage on Performances of Phase-Locked Loop Circuit in Nanoscale CMOS Technology. IEEE Transactions on Electron Devices, 2009, 56, 1774-1779.	3.0	9
146	High-voltage-tolerant stimulator with adaptive loading consideration for electronic epilepsy prosthetic SoC in a 0.18-µm CMOS process. , 2012, , .		9
147	On the Design of Power-Rail ESD Clamp Circuits With Gate Leakage Consideration in Nanoscale CMOS Technology. IEEE Transactions on Device and Materials Reliability, 2014, 14, 536-544.	2.0	9
148	Study on the ESD-induced gate-oxide breakdown and the protection solution in 28nm high-k metal-gate CMOS technology. , 2015, , .		9
149	Area-Efficient ESD Clamp Circuit With a Capacitance-Boosting Technique to Minimize Standby Leakage Current. IEEE Transactions on Device and Materials Reliability, 2015, 15, 156-162.	2.0	9
150	ESD protection for output pad with well-coupled field-oxide device in 0.5-Î¼m CMOS technology. IEEE Transactions on Electron Devices, 1997, 44, 503-505.	3.0	8
151	Failure analysis of ESD damage in a high-voltage driver IC and the effective ESD protection solution [CMOS]. , 0, , .		8
152	Design of negative charge pump circuit with polysilicon diodes in a 0.25 Î¼m CMOS process. , 0, , .		8
153	On-Chip High-Voltage Charge Pump Circuit in Standard CMOS Processes With Polysilicon Diodes. , 2005, , .		8
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