In-Cheol Park

List of Publications by Year in Descending Order

104 papers	1,115 citations	20 h-index	27 g-index
153 ext. papers	1,402 ext. citations	3 avg, IF	4.87 L-index

#	Paper	IF	Citations
104	Multi-Mode QC-LDPC Decoding Architecture With Novel Memory Access Scheduling for 5G New-Radio Standard. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2022**, 1-14	3.9	
103	Constant-Time Synchronous Binary Counter With Minimal Clock Period. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 1-1	3.5	0
102	Real-Time SSDLite Object Detection on FPGA. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 1-14	2.6	7
101	Interleaved Local Sorting for Successive Cancellation List Decoding of Polar Codes. *IEEE Access*, **2021**, 9, 128623-128632	3.5	1
100	Bitwise Early Termination of Multiuser Detection for IDMA Systems. *IEEE Communications Letters*, **2021**, 25, 2998-3002	3.8	0
99	Hybrid Convolution Architecture for Energy-Efficient Deep Neural Network Processing. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 1-13	3.9	2
98	Large-Small Sorting for Successive Cancellation List Decoding of Polar Codes. *IEEE Access*, **2020**, 8, 96955-96962	3.9	2
97	Ultra-Low-Latency LDPC Decoding Architecture using Reweighted Offset Min-Sum Algorithm **2020**,		3
96	Low-Complexity Address Generation for Multiuser Detectors in IDMA Systems. *Electronics (Switzerland)*, **2020**, 9, 2069	2.6	2
95	A 120-mW 0.16-ms-Latency Connectivity-Scalable Multiuser Detector for Interleave Division Multiple Access. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 470-474	3.5	2
94	Parallel IDMA Architecture Based on Interleaving with Replicated Subpatterns **2019**,		3
93	Energy-Efficient Symmetric BC-BCH Decoder Architecture for Mobile Storages. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 4462-4475	3.9	3
92	A Low-Latency Multi-Touch Detector Based on Concurrent Processing of Redesigned Overlap Split and Connected Component Analysis. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 1-11	3.9	4
91	Retrain-Less Weight Quantization for Multiplier-Less Convolutional Neural Networks. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 1-11	3.9	9
90	Fast Low-Complexity Triple-Error-Correcting BCH Decoding Architecture. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 764-768	3.5	5
89	A 2.4pJ/bit, 6.37Gb/s SPC-enhanced BC-BCH decoder in 65nm CMOS for NAND flash storage systems **2018**,		2
88	A Memory-Efficient IDMA Architecture Based on On-the-Fly Despreading. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 3327-3337	5.5	6

87	Energy-Efficient Convolution Architecture Based on Rescheduled Dataflow. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 4196-4207	3.9	27
86	DSIP: A Scalable Inference Accelerator for Convolutional Neural Networks. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 605-618	5.5	33
85	Efficient Implementation of Multiple Interleavers in IDMA for 5G **2018**,		2
84	Interference Cancellation Architecture for Pipelined Parallel MIMO Detectors **2018**,		1
83	A Fast Successive Cancellation List Decoder for Polar Codes With an Early Stopping Criterion. *IEEE Transactions on Signal Processing*, **2018**, 66, 4971-4979	4.8	17
82	High-Performance Low-Area Video Up-Scaling Architecture for 4-K UHD Video. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 437-441	3.5	12
81	Multi-Bit Flipping Decoding of LDPC Codes for NAND Storage Systems. *IEEE Communications Letters*, **2017**, 21, 979-982	3.8	15
80	. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 1042-1046	3.5	7
79	Low-Power LDPC-CC Decoding Architecture Based on the Integration of Memory Banks. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 1057-1061	3.5	4
78	Low-Latency Low-Cost Architecture for Square and Cube Roots. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2017**, E100.A, 1951-1955	0.4	
77	Improved Successive-Cancellation Decoding of Polar Codes Based on Recursive Syndrome Decomposition. *IEEE Communications Letters*, **2017**, 21, 2344-2347	3.8	2
76	Improved Hard-Reliability Based Majority-Logic Decoding for Non-Binary LDPC Codes. *IEEE Communications Letters*, **2017**, 21, 230-233	3.8	10
75	An energy-optimized (37840, 34320) symmetric BC-BCH decoder for healthy mobile storages **2017**,		4
74	Energy-Efficient Floating-Point MFCC Extraction Architecture for Speech Recognition Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 754-758	2.6	23
73	Efficient Pruning for Successive-Cancellation Decoding of Polar Codes. *IEEE Communications Letters* , **2016**, 20, 2362-2365	3.8	3
72	Area-Efficient Approach for Generating Quantized Gaussian Noise. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2016**, 63, 1005-1013	3.9	3
71	Efficient Sorting Architecture for Successive-Cancellation-List Decoding of Polar Codes. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2016**, 63, 673-677	3.5	25
70	Low-Power Parallel Chien Search Architecture Using a Two-Step Approach. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2016**, 63, 269-273	3.5	6

69	Energy-Scalable 4KB LDPC Decoding Architecture for NAND-Flash-Based Storage Systems. *IEICE Transactions on Electronics*, **2016**, E99.C, 293-301	0.4	7
68	Low-complexity symbol detection for massive MIMO uplink based on Jacobi method **2016**,		20
67	Partially Parallel Encoder Architecture for Long Polar Codes. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2015**, 62, 306-310	3.5	16
66	Efficient Parallel Architecture for Linear Feedback Shift Registers. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2015**, 62, 1068-1072	3.5	20
65	Reverse Rate Matching for Low-Power LTE-Advanced Turbo Decoders. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2015**, 62, 2920-2928	3.9	4
64	Low-Complexity Tree Architecture for Finding the First Two Minima. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2015**, 62, 61-64	3.5	22
63	7.3 Gb/s universal BCH encoder and decoder for SSD controllers **2014**,		11
62	High-Throughput and Low-Complexity BCH Decoding Architecture for Solid-State Drives. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 1183-1187	2.6	19
61	Tail-Overlapped SISO Decoding for High-Throughput LTE-Advanced Turbo Decoders. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 2711-2720	3.9	4
60	Low-Complexity Low-Latency Architecture for Matching of Data Encoded With Hard Systematic Error-Correcting Codes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 1648-1652	2.6	3
59	Area-efficient method to approximate two minima for LDPC decoders. *Electronics Letters*, **2014**, 50, 1701-1702	1.1	1
58	A search-less DEC BCH decoder for low-complexity fault-tolerant systems **2014**,		4
57	Single-step glitch-free NAND-based digitally controlled delay lines using dual loops. *Electronics Letters*, **2014**, 50, 930-932	1.1	4
56	Efficient Tree-Traversal Strategy for Soft-Output MIMO Detection Based on Candidate-Set Reorganization. *IEEE Communications Letters*, **2013**, 17, 1758-1761	3.8	1
55	Low-Complexity Parallel QPP Interleaver Based on Permutation Patterns. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2013**, 60, 162-166	3.5	4
54	Area-Efficient Multimode Encoding Architecture for Long BCH Codes. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2013**, 60, 872-876	3.5	17
53	A 2.74-pJ/bit, 17.7-Gb/s Iterative Concatenated-BCH Decoder in 65-nm CMOS for NAND Flash Memory. *IEEE Journal of Solid-State Circuits*, **2013**, 48, 2531-2540	5.5	20
52	Area-Efficient QC-LDPC Decoder Architecture Based on Stride Scheduling and Memory Bank Division. *IEICE Transactions on Communications*, **2013**, E96.B, 1772-1779	0.5	2

51	Low-Complexity Tone Reservation for PAPR Reduction in OFDM Communication Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1919-1923	2.6	7
50	Immediate Exchange of Extrinsic Information for High-Throughput Turbo Decoding. *IEEE Communications Letters*, **2012**, 16, 2048-2051	3.8	
49	6.4Gb/s multi-threaded BCH encoder and decoder for multi-channel SSD controllers **2012**,		30
48	Small-area parallel syndrome calculation for strong BCH decoding **2012**,		5
47	Low-Complexity Parallel Chien Search Structure Using Two-Dimensional Optimization. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2011**, 58, 522-526	3.5	17
46	Efficient Pruning for Infinity-Norm Sphere Decoding Based on Schnorr-Euchner Enumeration. *IEICE Transactions on Communications*, **2011**, E94-B, 2677-2680	0.5	0
45	Spur-Free MASH Delta-Sigma Modulation. *IEEE Transactions on Circuits and Systems I: Regular Papers* , **2010**, 57, 2426-2437	3.9	34
44	High-Throughput and Area-Efficient MIMO Symbol Detection Based on Modified Dijkstra's Search. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2010**, 57, 1756-1766	3.9	19
43	Small-Area and Low-Energy K-Best MIMO Detector Using Relaxed Tree Expansion and Early Forwarding. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2010**, 57, 2753-2761	3.9	31
42	Capacitor array structure and switching control scheme to reduce capacitor mismatch effects for SAR analog-to-digital converters **2010**,		2
41	Design of a Scalable and Programmable Sound Synthesizer. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 875-886	2.6	
40	Optimization of Arithmetic Coding for JPEG2000. *IEEE Transactions on Circuits and Systems for Video Technology*, **2010**, 20, 446-451	6.4	7
39	Multiplier-less and Table-less Linear Approximation for Square-Related Functions. *IEICE Transactions on Information and Systems*, **2010**, E93-D, 2979-2988	0.6	2
38	A unified parallel radix-4 turbo decoder for mobile WiMAX and 3GPP-LTE **2009**,		39
37	Pipelined Discrete Wavelet Transform Architecture Scanning Dual Lines. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2009**, 56, 916-920	3.5	12
36	Novel pipelined DWT architecture for dual-line scan **2009**,		4
35	Bit-Level Extrinsic Information Exchange Method for Double-Binary Turbo Codes. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2009**, 56, 81-85	3.5	20
34	Multiplier-less and table-less linear approximation for square and square-root **2009**,		7

33	Low-Power and High-Accurate Synchronization for IEEE 802.16d Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2008**, 16, 1620-1630	2.6	8
32	FIR Filter Synthesis Considering Multiple Adder Graphs for a Coefficient. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2008**, 27, 958-962	2.5	12
31	Double-Binary Circular Turbo Decoding Based on Border Metric Encoding. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2008**, 55, 79-83	3.5	20
30	A 50Mbps double-binary turbo decoder for WiMAX based on bit-level extrinsic information exchange **2008**,		6
29	Pipelined Cartesian-to-Polar Coordinate Conversion Based on SRT Division. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2007**, 54, 680-684		8
28	Two-Step Aprroach for Coarse Time Synchronization and Frequency Offset Estimation for IEEE 802.16D Systems. *Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on*, **2007**,		1
27	High Speed Sphere Decoding Based on Vertically Incremental Computation **2007**,		6
26	SIMD Processor-Based Turbo Decoder Supporting Multiple Third-Generation Wireless Standards. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2007**, 15, 801-810	2.6	25
25	Balanced Binary-Tree Decomposition for Area-Efficient Pipelined FFT Processing. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2007**, 54, 889-900		53
24	Low-power log-MAP decoding based on reduced metric memory access. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2006**, 53, 1244-1253		8
23	Loosely coupled memory-based decoding architecture for low density parity check codes. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2006**, 53, 1045-1056		34
22	A third-order /spl Sigma//spl Delta/ modulator in 0.18-/spl mu/m CMOS with calibrated mixed-mode integrators. *IEEE Journal of Solid-State Circuits*, **2005**, 40, 918-925	5.5	15
21	SAT-based unbounded symbolic model checking. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2005**, 24, 129-140	2.5	9
20	A low-power variable length decoder for MPEG-2 based on successive decoding of short codewords. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2003**, 39, 73-82		5
19	A single-chip programmable platform based on a multithreaded processor and configurable logic clusters. *IEEE Journal of Solid-State Circuits*, **2003**, 38, 1703-1711	5.5	1
18	Processor-based turbo interleaver for multiple third-generation wireless standards. *IEEE Communications Letters*, **2003**, 7, 210-212	3.8	16
17	High performance memory mode control for HDTV decoders. *IEEE Transactions on Consumer Electronics*, **2003**, 49, 1348-1353	4.8	10
16	Digital filter synthesis based on an algorithm to generate all minimal signed digit representations. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2002**, 21, 1525-1529	2.5	46

15	FIR filter synthesis algorithms for minimizing the delay and the number of adders. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2001**, 48, 770-777		49
14	A fixed-point MPEG audio processor operating at low frequency. *IEEE Transactions on Consumer Electronics*, **2001**, 47, 779-786	4.8	1
13	High-performance and low-power memory-interface architecture for video processing applications. *IEEE Transactions on Circuits and Systems for Video Technology*, **2001**, 11, 1160-1170	6.4	31
12	MetaCore: an application-specific programmable DSP development system. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2000**, 8, 173-183	2.6	6
11	Synthesis of application specific instructions for embedded DSP software. *IEEE Transactions on Computers*, **1999**, 48, 603-614	2.5	38
10	Digital signal processor with efficient RGB interpolation and histogram accumulation. *IEEE Transactions on Consumer Electronics*, **1998**, 44, 1389-1395	4.8	15
9	Design Verification of Complex Microprocessors. *Journal of Circuits, Systems and Computers*, **1997**, 07, 301-318	0.9	0
8	Verification methodology of compatible microprocessors		1
7	A hybrid delta-sigma modulator with adaptive calibration		3
6	History-based memory mode prediction for improving memory performance		1
5	A programmable turbo decoder for multiple 3G wireless standards		8
4	Scheduling algorithm for partially parallel architecture of LDPC decoder by matrix permutation		6
3	Area-efficient digital baseband module for Bluetooth wireless communications		1
2	A hardware accelerator for the specular intensity of Phong illumination model in 3-dimensional graphics		1
1	Exploiting intellectual properties in ASIP designs for embedded DSP software		3