Oscar Gustafsson

List of Publications by Year
in descending order

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Version: 2024-02-01

130	1,613	471509	434195
papers	citations	17	31
		h-index	g-index

135	135	135	711
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Massive Machine-Type Communication Pilot-Hopping Sequence Detection Architectures Based on Non-Negative Least Squares for Grant-Free Random Access. IEEE Open Journal of Circuits and Systems, 2021, 2, 253-264.	1.9	2
2	Overlap-Save Commutators for High-Speed Streaming Data Filtering. , 2021, , .		0
3	Low-Latency Parallel Hermitian Positive-Definite Matrix Inversion for Massive MIMO. , 2021, , .		0
4	Approximate Floating-Point Operations with Integer Units by Processing in the Logarithmic Domain. , 2021, , .		5
5	Improved Particle Filter Resampling Architectures. Journal of Signal Processing Systems, 2020, 92, 555-568.	2.1	10
6	Using Transposition to Efficiently Solve Constant Matrix-Vector Multiplication and Sum of Product Problems. Journal of Signal Processing Systems, 2020, 92, 1075-1089.	2.1	0
7	High-Speed Chromatic Dispersion Compensation Filtering in FPGAs for Coherent Optical Communication. , 2020, , .		0
8	Acceleration of Simulation Models Through Automatic Conversion to FPGA Hardware. , 2020, , .		1
9	Pilot-Hopping Sequence Detection Architecture for Grant-Free Random Access using Massive MIMO. , 2020, , .		2
10	A Tool to Enable FPGA-Accelerated Dynamic Programming for Energy Management of Hybrid Electric Vehicles. IFAC-PapersOnLine, 2020, 53, 15104-15109.	0.9	1
11	An Architecture for Grant-Free Random Access Massive Machine Type Communication Using Coordinate Descent. , 2020, , .		2
12	Optimum Circuits for Bit-Dimension Permutations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1148-1160.	3.1	17
13	A 1 Million-Point FFT on a Single FPGA. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3863-3873.	5.4	13
14	Direct digital-to-RF converter employing semi-digital FIR voltage-mode RF DAC. The Integration VLSI Journal, 2019, 66, 128-134.	2.1	0
15	An Architecture for Grant-Free Massive MIMO MTC Based on Compressive Sensing. , 2019, , .		4
16	Optimization problem formulation for semi-digital FIR digital-to-analog converter considering coefficients precision and analog metrics. Analog Integrated Circuits and Signal Processing, 2019, 99, 287-298.	1.4	2
17	Hardware architectures for the fast Fourier transform. , 2019, , 613-647.		15
18	SFFâ€"The Single-Stream FPGA-Optimized Feedforward FFT Hardware Architecture. Journal of Signal Processing Systems, 2018, 90, 1583-1592.	2.1	12

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19	Optimal Single Constant Multiplication Using Ternary Adders. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 928-932.	3.0	13
20	Improved Implementation Approaches for 512-tap 60 GSa/s Chromatic Dispersion FIR Filters. , 2018, , .		2
21	A Modular Base Station Architecture for Massive MIMO with Antenna and User Scalability per Processing Node. , 2018, , .		2
22	Area-Efficient Scheduling Scheme Based FFT Processor for Various OFDM Systems. , 2018, , .		7
23	Obtaining Minimum Depth Sum of Products from Multiple Constant Multiplication. , 2018, , .		1
24	Karatsuba with Rectangular Multipliers for FPGAs. , 2018, , .		11
25	On Lifting-Based Fixed-Point Complex Multiplications and Rotations. , 2017, , .		4
26	Efficient FPGA Mapping of Pipeline SDF FFT Cores. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2486-2497.	3.1	21
27	Computation limited matrix inversion using Neumann series expansion for massive MIMO. , 2017, , .		2
28	Approximate Neumann Series or Exact Matrix Inversion for Massive MIMO?. , 2017, , .		13
29	Implementation approaches for 512-tap 60 GSa/s chromatic dispersion FIR filters. , 2017, , .		6
30	A scalable architecture for massive MIMO base stations using distributed processing. , 2016, , .		25
31	Hardware architecture for positive definite matrix inversion based on LDL decomposition and back-substitution. , 2016, , .		3
32	Multiplierless Unity-Gain SDF FFTs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3003-3007.	3.1	28
33	On the Implementation of Time-Multiplexed Frequency-Response Masking Filters. IEEE Transactions on Signal Processing, 2016, 64, 3933-3944.	5.3	6
34	Fast and area efficient adder for wide data in recent Xilinx FPGAs. , 2016, , .		5
35	The Serial Commutator FFT. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 974-978.	3.0	33
36	CORDIC II: A New Improved CORDIC Algorithm. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 186-190.	3.0	60

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37	Filter-bank based all-digital channelizers and aggregators for multi-standard video distribution. , 2015, , .		0
38	On fixed-point implementation of symmetric matrix inversion. , 2015, , .		10
39	Generalized division-free architecture and compact memory structure for resampling in particle filters. , 2015, , .		0
40	Decimation filters for high-speed delta-sigma modulators with passband constraints: General versus CIC-based FIR filters. , 2015, , .		0
41	On frequency-domain implementation of digital FIR filters. , 2015, , .		0
42	Design of Finite Word Length Linear-Phase FIR Filters in the Logarithmic Number System Domain. VLSI Design, 2014, 2014, 1-14.	0.5	9
43	Challenging the limits of FFT performance on FPGAs (Invited paper). , 2014, , .		15
44	Optimal Least-Squares FIR Digital Filters for Compensation of Chromatic Dispersion in Digital Coherent Optical Receivers. Journal of Lightwave Technology, 2014, 32, 1449-1456.	4.6	45
45	Low-Complexity Multiplierless Constant Rotators Based on Combined Coefficient Selection and Shift-and-Add Implementation (CCSSI). IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2002-2012.	5.4	33
46	Reducing Complexity and Power of Digital Multibit Errorâ€“Feedback $DeltaSigma$ Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 641-645.	3.0	0
47	Linear programming design of semi-digital FIR filter and ΣΔ modulator for VDSL2 transmitter. , 2014, , .		3
48	Low-complexity general FIR filters based on Winograd's inner product algorithm. , 2013, , .		1
49	Pipelined Radix-2^{k} Feedforward FFT Architectures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 23-32.	3.1	164
50	On the Fixed-Point Implementation of Fractional-Delay Filters Based on the Farrow Structure. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 926-937.	5.4	18
51	Hardware Implementation of Digital Signal Processing Algorithms. Journal of Electrical and Computer Engineering, 2013, 2013, 1-2.	0.9	5
52	Unified architecture for 2, 3, 4, 5, and 7â€point DFTs based on Winograd Fourier transform algorithm. Electronics Letters, 2013, 49, 348-349.	1.0	25
53	A reconfigurable FFT architecture for variable-length and multi-streaming OFDM standards. , 2013, , .		13
54	Low-complexity rotators for the FFT using base-3 signed stages. , 2012, , .		4

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55	Using DSP block pre-adders in pipeline SDF FFT implementations in contemporary FPGAs. , 2012, , .		4
56	Linear Programming Design of Coefficient Decimation FIR Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 60-64.	3.0	8
57	Magnitude scaling for increased SFDR in DDFS. , 2011, , .		0
58	Generation of all radix-2 fast Fourier transform algorithms using binary trees. , 2011, , .		20
59	Computational and implementation complexity of polynomial evaluation schemes. , 2011, , .		3
60	Optimum Circuits for Bit Reversal. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 657-661.	3.0	42
61	Minimum adder depth multiple constant multiplication algorithm for low power FIR filters. , 2011, , .		19
62	Implementation of time-multiplexed sparse periodic FIR filters for FRM on FPGAs. , 2011, , .		3
63	Accurate Rotations Based on Coefficient Scaling. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 662-666.	3.0	20
64	Implementation of narrow-band frequency-response masking for efficient narrow transition band FIR filters on FPGAs. , 2011, , .		4
65	Finite wordlength properties of matrix inversion algorithms in fixed-point and logarithmic number systems. , 2011, , .		2
66	On the efficient computation of single-bit input word length pipelined FFTs. IEICE Electronics Express, 2011, 8, 1437-1443.	0.8	0
67	The Impact of Dynamic Voltage and Frequency Scaling on Multicore DSP Algorithm Design [Exploratory DSP]. IEEE Signal Processing Magazine, 2011, 28, 127-144.	5.6	18
68	FPGA implementation of rate-compatible QC-LDPC code decoder. , 2011, , .		4
69	Optimization of AIQ representations for low complexity wavelet transforms. , 2011, , .		6
70	On using the logarithmic number system for finite wordlength matrix inversion. , 2011, , .		2
71	A 512-point 8-parallel pipelined feedforward FFT for WPAN. , 2011, , .		24
72	Fast and VLSI efficient binary-to-CSD encoder using bypass signal. Electronics Letters, 2011, 47, 18.	1.0	14

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73	Low-Complexity Constant Multiplication Based on Trigonometric Identities with Applications to FFTs. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2011, E94-A, 2361-2368.	0.3	8
74	Integer Linear Programming-Based Bit-Level Optimization for High-Speed FIR Decimation Filter Architectures. Circuits, Systems, and Signal Processing, 2010, 29, 81-101.	2.0	17
75	Twiddle factor memory switching activity analysis of radix-2² and equivalent FFT algorithms. , 2010, , .		5
76	4k-point FFT algorithms based on optimized twiddle factor multiplication for FPGAs. , 2010, , .		8
77	Integer linear programming based optimization of puncturing sequences for quasi-cyclic low-density parity-check codes. , 2010, , .		0
78	Reconfigurable multiple constant multiplication using minimum adder depth. , 2010, , .		9
79	Low-complexity parallel evaluation of powers exploiting bit-level redundancy. , 2010, , .		0
80	Architectures for cognitive radio testbeds and demonstrators - An overview. , 2010, , .		13
81	Rate-compatible LDPC code decoder using check-node merging. , 2010, , .		1
82	Redundancy reduction for high-speed fir filter architectures based on carry-save adder trees. , 2010, , .		3
83	Power estimation of recursive and non-recursive CIC filters implemented in deep-submicron technology. , 2010, , .		15
84	Design of sparse non-periodic narrow-band and wide-band FRM-like FIR filters. , 2010, , .		2
85	Alternatives for low-complexity complex rotators. , 2010, , .		0
86	Generalized overlapping digit patterns for multi-dimensional sub-expression sharing. , 2010, , .		2
87	Switching activity estimation of CIC filter integrators. , 2010, , .		1
88	Addition Aware Quantization for Low Complexity and High Precision Constant Multiplication. IEEE Signal Processing Letters, 2010, 17, 173-176.	3.6	22
89	Estimation of the switching activity in shift-and-add based computations. , 2009, , .		6
90	Techniques for avoiding sign-extension in multiple constant multiplication. , 2009, , .		6

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91	Low-complexity reconfigurable complex constant multiplication for FFTs. , 2009, , .		25
92	Analysis of switching activity in DSP signals in the presence of noise. , 2009, , .		1
93	Analysis of twiddle factor memory complexity of radix-2ⁱ pipelined FFTs. , 2009, , .		5
94	Design of multiplierless FIR filters with an adder depth versus filter order trade-off. , 2009, , .		3
95	Scaling of fractional delay filters based on the Farrow structure. , 2009, , .		4
96	Bit-level optimized FIR filter architectures for high-speed decimation applications. , 2008, , .		5
97	Implementation of elementary functions for logarithmic number systems. IET Computers and Digital Techniques, 2008, 2, 295.	1.2	29
98	Comparison of multiplierless implementation of nonlinear-phase versus linear-phase FIR filters. , 2008, , .		3
99	Switching activity estimation for shift-and-add based constant multipliers. , 2008, , .		10
100	An empirical study on standard cell synthesis of elementary function lookup tables. , 2008, , .		5
101	Architecture-aware design of a decimation filter based on a dual wordlength multiply-accumulate unit. , 2008, , .		1
102	Power optimization of weighted bit-product summation tree for elementary function generator. , 2008, , .		0
103	Towards optimal multiple constant multiplication: A hypergraph approach. , 2008, , .		23
104	Synthesis of bandpass circulator-tree wave digital filters. , 2008, , .		1
105	The canonical minimised Adder graph representation. Proceedings of SPIE, 2008, , .	0.8	0
106	Comments on 'A 70 MHz Multiplierless FIR Hilbert Transformer in 0.35 Âm Standard CMOS Library'. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2008, E91-A, 899-900.	0.3	3
107	On the Design of Sparse Half-Band Like FIR Filters. Conference Record of the Asilomar Conference on Signals, Systems and Computers, 2007, , .	0.0	22
108	Complexity Comparison of Linear-Phase Mth-Band and General FIR Filters. , 2007, , .		4

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109	Transition-activity aware design of reduction-stages for parallel multipliers. , 2007, , .		5
110	A Difference Based Adder Graph Heuristic for Multiple Constant Multiplication Problems. , 2007, , .		80
111	Lower Bounds for Constant Multiplication Problems. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 974-978.	3.0	89
112	Bit-Level Optimization of Shift-and-Add Based FIR Filters. , 2007, , .		31
113	Synthesis of Circulator-Tree Wave Digital Filters. Proc Int Symp Image Signal Process Anal, 2007, , .	0.0	2
114	Low-Complexity Constant Multiplication Using Carry-Save Arithmetic for High-Speed Digital Filters. Proc Int Symp Image Signal Process Anal, 2007, , .	0.0	8
115	On the Complexity of Multiplierless Direct and Polyphase FIR Filter Structures. Proc Int Symp Image Signal Process Anal, 2007, , .	0.0	10
116	Power optimized partial product reduction interconnect ordering in parallel multipliers. , 2007, , .		7
117	Complexity Reduction of Constant Matrix Computations over the Binary Field. Lecture Notes in Computer Science, 2007, , 103-115.	1.3	8
118	Multiplierless Piecewise Linear Approximation of Elementary Functions. , 2006, , .		4
119	Implementation of Polyphase Decomposed FIR Filters for Interpolation and Decimation Using Multiple Constant Multiplication Techniques. , 2006, , .		17
120	Low-Complexity and Low-Power Color Space Conversion for Digital Video. , 2006, , .		8
121	Adjustable Fractional-Delay FIR Filters Using the Farrow Structure and Multirate Techniques. , 2006, , .		22
122	Simplified Design of Constant Coefficient Multipliers. Circuits, Systems, and Signal Processing, 2006, 25, 225-251.	2.0	79
123	Energy-efficient data representation in LDPC decoders. Electronics Letters, 2006, 42, 1051.	1.0	0
124	Efficient Implementation of FIR Filter Based Rational Sampling Rate Converters Using Constant Matrix Multiplication. , 2006, , .		11
125	Linear-phase FIR interpolation, decimation, and mth-band filters utilizing the farrow structure. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2005, 52, 2197-2207.	0.1	46
126	Graph-based codeword selection for memoryless low-power bus coding. Electronics Letters, 2004, 40, 1531.	1.0	2

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127	Power Estimation for Ripple-Carry Adders with Correlated Input Data. Lecture Notes in Computer Science, 2004, , 662-674.	1.3	11
128	Single Filter Frequency Masking High-Speed Recursive Digital Filters. Circuits, Systems, and Signal Processing, 2003, 22, 219.	2.0	14
129	SINGLE FILTER FREQUENCY-RESPONSE MASKING FIR FILTERS. Journal of Circuits, Systems and Computers, 2003, 12, 601-630.	1.5	17
130	Low-Complexity and High-Speed Constant Multiplications for Digital Filters Using Carry-Save Arithmetic. , 0, , .		8