

Anjana Dissanayake

List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/8840339/publications.pdf>

Version: 2024-02-01

18
papers

153
citations

1307594

7
h-index

1588992

8
g-index

18
all docs

18
docs citations

18
times ranked

134
citing authors

#	ARTICLE	IF	CITATIONS
1	A 2.4 GHz-91.5 dBm Sensitivity Within-Packet Duty-Cycled Wake-Up Receiver. IEEE Journal of Solid-State Circuits, 2022, 57, 917-931.	5.4	14
2	A 184-nW, $\hat{\sim}$ 78.3-dBm Sensitivity Antenna-Coupled Supply, Temperature, and Interference-Robust Wake-Up Receiver at 4.9 GHz. IEEE Transactions on Microwave Theory and Techniques, 2022, 70, 744-757.	4.6	7
3	21.5 An Integrated 2.4GHz -91.5dBm-Sensitivity Within-Packet Duty-Cycled Wake-Up Receiver Achieving $2\hat{1}\frac{3}{4}$ W at 100ms Latency. , 2021, , .		2
4	A 0.6V 785-nW Multimodal Sensor Interface IC for Ozone Pollutant Sensing and Correlated Cardiovascular Disease Monitoring. IEEE Journal of Solid-State Circuits, 2021, 56, 1058-1070.	5.4	13
5	Stacked Transconductance Boosting for Ultra-Low Power 2.4GHz RF Front-End Design. , 2021, , .		0
6	A Multichannel, MEMS-Less $\hat{\sim}$ 99dBm 260nW Bit-Level Duty Cycled Wakeup Receiver. , 2020, , .		9
7	A 785nW Multimodal (V/I/R) Sensor Interface IC for Ozone Pollutant Sensing and Correlated Cardiovascular Disease Monitoring. , 2020, , .		2
8	A- 108dBm Sensitivity, -28dB SIR, 130nW to 41 \hat{A} μ W, Digitally Reconfigurable Bit-Level Duty-Cycled Wakeup and Data Receiver. , 2020, , .		2
9	Enabling Channelizing Filters for High Impedance Nodes with Temperature Compensated Lamb-Wave Resonators. , 2020, , .		1
10	A -106dBm 33nW Bit-Level Duty-Cycled Tuned RF Wake-up Receiver. , 2019, , .		13
11	A 2.5 ppm/ \hat{A} $^{\circ}$ C 1.05-MHz Relaxation Oscillator With Dynamic Frequency-Error Compensation and Fast Start-Up Time. IEEE Journal of Solid-State Circuits, 2019, 54, 1952-1959.	5.4	20
12	A Highly Reconfigurable Bit-Level Duty-Cycled TRF Receiver Achieving $\hat{\sim}$ 106-dBm Sensitivity and 33-nW Average Power Consumption. IEEE Solid-State Circuits Letters, 2019, 2, 309-312.	2.0	11
13	A 0.6-V 44.6-fj/Cycle Energy-Optimized Frequency-Locked Loop in 65-nm CMOS With 20.3-ppm/ \hat{A} $^{\circ}$ C Stability. IEEE Solid-State Circuits Letters, 2019, 2, 223-226.	2.0	9
14	A 45- $\hat{;}$ μ W, 162.1-dBc/Hz FoM, 490-MHz Two-Stage Differential Ring VCO Without a Cross-Coupled Latch. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1579-1583.	3.0	13
15	A 2.5 ppm/ \hat{A} $^{\circ}$ C 1.05 MHz Relaxation Oscillator with Dynamic Frequency-Error Compensation and 8 \hat{A} μ s Start-up Time. , 2018, , .		1
16	A 64 \hat{A} μ W, 23 dB gain, 8 dB NF, 2.4 GHz RF front-end for ultra-low power Internet-of-Things transceivers. , 2017, , .		11
17	A 2.4GHz, $\hat{\sim}$ 102dBm-sensitivity, 25kb/s, 0.466mW interference resistant BFSK multi-channel sliding-IF ULP receiver. , 2017, , .		14
18	The Evolution of Channelization Receiver Architecture: Principles and Design Challenges. IEEE Access, 2017, 5, 25385-25395.	4.2	11