Henrik Sjoland

List of Publications by Year
in descending order

124 papers	1,508 citations	687363 13 h-index	361022 35 g-index
124 all docs	124 docs citations	124 times ranked	1144 citing authors

#	Article	IF	Citations
1	An ultra-low power high-precision logarithmic-curvature compensated all-CMOS voltage reference in 65Ânm CMOS. Analog Integrated Circuits and Signal Processing, 2021, 107, 319-330.	1.4	1
2	6G Wireless Systems: Vision, Requirements, Challenges, Insights, and Opportunities. Proceedings of the IEEE, 2021, 109, 1166-1199.	21.3	538
3	Power Scaling Laws for Radio Receiver Front Ends. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2183-2195.	5.4	1
4	A Decade Frequency Range CMOS Power Amplifier for Sub-6-GHz Cellular Terminals. IEEE Microwave and Wireless Components Letters, 2020, 30, 54-57.	3.2	11
5	A 20-GHz Bandwidth Power Amplifier for Phased Array 5G New Radio Transmitters. IEEE Solid-State Circuits Letters, 2020, 3, 302-305.	2.0	3
6	A high precision logarithmic-curvature compensated all CMOS voltage reference. Analog Integrated Circuits and Signal Processing, 2019, 99, 383-392.	1.4	4
7	A Bond Wire Connection Implementation at mm-Wave Active Microstrip Antenna. IEEE Microwave and Wireless Components Letters, 2019, 29, 427-429.	3.2	8
8	A 10-mW mm-Wave Phase-Locked Loop With Improved Lock Time in 28-nm FD-SOI CMOS. IEEE Transactions on Microwave Theory and Techniques, 2019, 67, 1588-1600.	4.6	23
9	An Injection-Locked Power Up-Converter in 65-nm CMOS for Cellular Applications. IEEE Transactions on Microwave Theory and Techniques, 2019, 67, 1065-1077.	4.6	2
10	Improving Receiver Close-In Blocker Tolerance by Baseband <inline-formula> <tex-math notation="LaTeX">G_m-C </tex-math> </inline-formula> Notch Filtering. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 885-896.	5.4	10
11	A 28-nm FD-SOI 115-fs Jitter PLL-Based LO System for 24â€“30-GHz Sliding-IF 5G Transceivers. IEEE Journal of Solid-State Circuits, 2018, 53, 1988-2000.	5.4	54
12	A 26GHz 22.2DBM Variable Gain Power Amplifier in 28NM FD-SOI CMOS for 5G Antenna Arrays. , 2018, , .		4
13	Two mm-Wave VCOs in 28-nm UTBB FD-SOI CMOS. IEEE Microwave and Wireless Components Letters, 2017, 27, 509-511.	3.2	10
14	System simulations of a 1.5ÂV SiGe 81â€“86ÂGHz E-band transmitter. Analog Integrated Circuits and Signal Processing, 2017, 90, 333-349.	1.4	2
15	Two Tunable Frequency Duplexer Architectures for Cellular Transceivers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2988-2999.	5.4	5
16	A Linearization Technique for Differential OTAs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1002-1006.	3.0	7
17	Broadband LDMOS 40 W and 55 W integrated power amplifiers. , 2017, , .		0
18	A 16â€“20 GHz LO system with 115 fs jitter for 24â€“30 GHz 5G in 28 nm FD-SOI CMOS. , 2017, , .		8

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19	A 65 nm CMOS Wideband Radio Receiver With <inline-formula> <tex-math notation="LaTeX">$Delta Sigma $</tex-math> </inline-formula>-Based A/D-Converting Channel-Select Filters. IEEE Journal of Solid-State Circuits, 2016, 51, 1566-1578.	5.4	16
20	Experimental Investigation of Adaptive Impedance Matching for a MIMO Terminal With CMOS-SOI Tuners. IEEE Transactions on Microwave Theory and Techniques, 2016, 64, 1622-1633.	4.6	7
21	A 1.5 V 28 GHz Beam Steering SiGe PLL for an 81-86 GHz E-Band Transmitter. IEEE Microwave and Wireless Components Letters, 2016, 26, 843-845.	3.2	10
22	A cellular receiver front-end with blocker sensing. , 2016, , .		5
23	A Digitally Assisted Nonlinearity Mitigation System for Tunable Channel Select Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 69-73.	3.0	10
24	A two-stage mm-wave PA with 18.5% PAE in 65 nm CMOS. , 2015, , .		2
25	CMOS adaptive TIA with embedded single-ended to differential conversion for analog optical links. , 2015, , .		10
26	A positive feedback passive mixer-first receiver front-end. , 2015, , .		25
27	Low Power Analog and Digital (7,5) Convolutional Decoders in 65 nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1863-1872.	5.4	4
28	A 28ÂGHz SiGe PLL for an 81â€“86ÂGHz E-band beam steering transmitter and an I/Q phase imbalance detection and compensation circuit. Analog Integrated Circuits and Signal Processing, 2015, 84, 383-398.	1.4	3
29	A Noise-Cancelling Receiver Front-End With Frequency Selective Input Matching. IEEE Journal of Solid-State Circuits, 2015, 50, 1137-1147.	5.4	21
30	A fully integrated 26 dBm linearized RF power amplifier in 65nm CMOS technology. , 2015, , .		3
31	A low band cellular terminal antenna impedance tuner in 130nm CMOS-SOI technology. , 2014, , .		4
32	InAs nanowire MOSFET differential active mixer on Siâ€substrate. Electronics Letters, 2014, 50, 682-683.	1.0	11
33	A 28 GHz SiGe QVCO and divider for an 81–86 GHz E-band beam steering transmitter PLL. , 2014, , .		1
34	A digital baseband for low power FSK based receiver in 65 nm CMOS. , 2014, , .		0
35	A 65 nm CMOS varactorless mm-wave VCO. , 2014, , .		2
36	A 4th order Gm-C filter with 10MHz bandwidth and 39dBm IIP3 in 65nm CMOS. , 2014, , .		2

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37	Lessons from ten years of the international master's program in System-on-Chip. , 2014, , .		1
38	Constant Mismatch Loss Boundary Circles and Their Application to Optimum State Distribution in Adaptive Matching Networks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 922-926.	3.0	12
39	A 2.45GHz, 50uW wake-up receiver front-end with −88dBm sensitivity and 250kbps data rate. , 2014, , .		12
40	Fully integrated radio over fiber downlink for distributed multi-antenna systems in 65 nm CMOS. , 2014, , .		0
41	InAs nanowire MOSFETs in three-transistor configurations: single balanced RF down-conversion mixers. Nanotechnology, 2014, 25, 485203.	2.6	7
42	An SDR duplex filter in SOI technology. , 2014, , .		0
43	A 28 GHz SiGe QVCO with an I/Q phase error detector for an 81–86 GHz E-band transceiver. , 2014, , .		4
44	A Fully Integrated Radio-Fiber Interface in 65 nm CMOS Technology. IEEE Photonics Technology Letters, 2014, 26, 444-446.	2.5	4
45	L-band 180° passive phase shifter employing auto-transformer in an SOS process. , 2014, , .		3
46	A noise cancelling 0.7–3.8 GHz resistive feedback receiver front-end in 65 nm CMOS. , 2014, , .		1
47	High-Resolution Passive Phase Shifters for Adaptive Duplexing Applications in SOS Process. IEEE Transactions on Microwave Theory and Techniques, 2014, 62, 1678-1685.	4.6	9
48	Ultra low power transceivers for wireless sensors and body area networks. , 2014, , .		3
49	A 60ÂGHz receiver front-end with PLL based phase controlled LO generation for phased-arrays. Analog Integrated Circuits and Signal Processing, 2014, 80, 23-32.	1.4	8
50	A 1ÂV power amplifier for 81â€“86ÂGHz E-band. Analog Integrated Circuits and Signal Processing, 2014, 80, 335-348.	1.4	4
51	A Compensation Technique for Two-Stage Differential OTAs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 594-598.	3.0	26
52	Digitally assisted adaptive non-linearity suppression scheme for RF front ends. , 2014, , .		1
53	Ultra low energy design exploration of digital decimation filters in 65nm dual-VT CMOS in the sub-VT domain. Microprocessors and Microsystems, 2013, 37, 494-504.	2.8	4
54	A 1V SiGe power amplifier for 81–86 GHz E-band. , 2013, , .		2

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55	Tunable wideband SAW-less receiver front-end in 65Ânm CMOS. Analog Integrated Circuits and Signal Processing, 2013, 77, 3-16.	1.4	2
56	A 3μW 500 kb/s ultra low power analog decoder with digital I/O in 65 nm CMOS. , 2013, , .		0
57	Performance evaluation of N-well/P-sub photodiodes in 65nm CMOS process. , 2013, , .		0
58	Wideband SAW-Less Receiver Front-End With Harmonic Rejection Mixer in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 242-246.	3.0	21
59	A 0.7 to 3ÂGHz wireless receiver front end in 65-nm CMOS with an LNA linearized by positive feedback. Analog Integrated Circuits and Signal Processing, 2013, 74, 49-57.	1.4	4
60	Introduction to the Special Issue on 29th NORCHIP Conference. Analog Integrated Circuits and Signal Processing, 2013, 74, 1-2.	1.4	0
61	An LC-based tunable low-isolation device for adaptive duplexers. , 2013, , .		2
62	A 31.25/125MSps continuous-time ΔΣ ADC with 64/59db SNDR in 130nm CMOS. , 2013, , .		0
63	A 3.4mW 65nm CMOS 5th order programmable active-RC channel select filter for LTE receivers. , 2013, , .		8
64	A 0.7 – 3.7 GHz six phase receiver front-end with third order harmonic rejection. , 2013, , .		4
65	Analog and digital approaches for an energy efficient low complexity channel decoder. , 2013, , .		3
66	A 70 and 210 GHz LO generator in 65nm CMOS. , 2012, , .		0
67	A Receiver Architecture for Devices in Wireless Body Area Networks. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2012, 2, 82-95.	3.6	34
68	A 2.45GHz ultra-low power quadrature front-end in 65nm CMOS. , 2012, , .		9
69	A 65-nm CMOS 250uW quadrature LO generation circuit. , 2012, , .		0
70	A 2GHz Tx LO generation circuit with active PPF and 3/2 divider in 65nm CMOS. , 2011, , .		0
71	Transistor sizing for a 4-state current mode analog channel decoder in 65-nm CMOS. , 2011, , .		4
72	A 2.25mW inductor-less 24 GHz CML frequency divider in 90nm CMOS. , 2011, , .		4

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73	A CMOS 4.35-mW +22-dBm IIP3 Continuously Tunable Channel Select Filter for WLAN/WiMAX Receivers. IEEE Journal of Solid-State Circuits, 2011, 46, 1382-1391.	5.4	143
74	A 5ÂGHz 90-nm CMOS all digital phase-locked loop. Analog Integrated Circuits and Signal Processing, 2011, 66, 49-59.	1.4	6
75	Design and analysis of an ultra-low-power LC quadrature VCO. Analog Integrated Circuits and Signal Processing, 2011, 67, 49-60.	1.4	3
76	A PLL based 12ÂGHz LO generator with digital phase control in 90Ânm CMOS. Analog Integrated Circuits and Signal Processing, 2011, 67, 309-318.	1.4	3
77	A 65nm CMOS 282μW 915MHz direct conversion receiver front-end. , 2011, , .		4
78	A linearized 1.6–5 GHz low noise amplifier using positive feedback in 65 nm CMOS. , 2011, , .		0
79	Design exploration of a 65 nm Sub-V<inf>T</inf> CMOS digital decimation filter chain. , 2011, , .		4
80	An analog (7,5) convolutional decoder in 65 nm CMOS for low power wireless applications. , 2011, , .		6
81	A 0.13µm CMOS ΔΣ PLL FM transmitter. , 2011, , .		0
82	A 90 nm CMOS 14.5 GHz Injection Locked LO generator with digital phase control. , 2010, , .		1
83	A 24-GHz 90-nm CMOS beamforming receiver front-end with analog baseband phase rotation. , 2010, , .		2
84	Low-Frequency Noise in Vertical InAs Nanowire FETs. IEEE Electron Device Letters, 2010, 31, 428-430.	3.9	30
85	A 90 nm CMOS <formula formulatype="inline"> <tex Notation="TeX">$+$</tex></formula>11 dBm IIP3 4 mW Dual-Band LNA for Cellular Handsets. IEEE Microwave and Wireless Components Letters, 2010, 20, 513-515.	3.2	14
86	A low power analog channel decoder for Ultra Portable Devices in 65 nm technology. , 2010, , .		1
87	Switched Mode Transmitter Architectures. , 2010, , 325-342.		5
88	Two 24 GHz receiver front-ends in 130-nm CMOS using SOP technology. , 2009, , .		8
89	A 24 GHz VCO with 20 % tuning range in 130-nm CMOS using SOP Technology. , 2009, , .		4
90	A 24-GHz quadrature receiver front-end in 90-nm CMOS. , 2009, , .		5

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91	Analysis of a high frequency and wide bandwidth active polyphase filter based on CMOS inverters. Analog Integrated Circuits and Signal Processing, 2009, 59, 243-255.	1.4	1
92	Third-order nonlinearity vs. load impedance for CMOS low-noise amplifiers. The Integration VLSI Journal, 2009, 42, 89-94.	2.1	1
93	A 5GHz 90-nm CMOS all digital phase-locked loop. , 2009, , .		2
94	A PLL based 12GHz LO generator with digital phase control in 90nm CMOS. , 2009, , .		4
95	A 65-nm CMOS ultra-low-power LC quadrature VCO. , 2009, , .		13
96	Two 130nm CMOS class-D RF power amplifiers suitable for polar transmitter architectures. , 2008, , .		6
97	A comparison of polar transmitter architectures using a GaN HEMT power amplifier. , 2008, , .		2
98	A 1W Class-D Audio Power Amplifier in a 0.35μm CMOS Process. , 2008, , .		0
99	A 30 GHz 90-nm CMOS Passive Subharmonic Mixer with 15 GHz Differential LO. , 2008, , .		0
100	A 90nm CMOS UWB LNA. , 2008, , .		2
101	60 GHz 130-nm CMOS second harmonic power amplifiers. , 2008, , .		1
102	A 24-GHz LC-QVCO in 130-nm CMOS using 4-bit switched tuning. , 2008, , .		12
103	A 5.4GHz 90-nm CMOS Digitally Controlled LC Oscillator with 21% Tuning Range, 1.1MHz resolution, and 180dB FOM. , 2008, , .		4
104	A 25-GHz differential LC-VCO in 90-nm CMOS. , 2008, , .		4
105	A 20-GHz 130-nm CMOS front-end using baluns on glass carrier. , 2008, , .		2
106	An 8-GHz Beamforming Transmitter IC in 130-nm CMOS. Radio Frequency Integrated Circuits (RFIC) Symposium, IEEE, 2007, , .	0.0	1
107	Teaching top down design of analog/mixed signal ICs through design projects. Proceedings - Frontiers in Education Conference, FIE, 2007, , .	0.0	3
108	A 26-GHz LC-QVCO in 0.13-Î¼m CMOS. , 2007, , .		3

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109	Second harmonic 60-GHz power amplifiers in 130-nm CMOS. , 2007, , .		0
110	25 GHz and 28 GHz Wide Tuning Range 130 nm CMOS VCOs with Ferroelectric Varactors. , 2007, , .		4
111	A GaN HEMT power amplifier with variable gate bias for envelope and phase signals. , 2007, , .		5
112	A 0.25W fully integrated class-D audio power amplifier in 0.35μm CMOS. , 2007, , .		3
113	Measured CMOS Switched High-Quality Capacitors in a Reconfigurable Matching Network. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 858-862.	3.0	27
114	A polyphase filter based on CMOS inverters. Analog Integrated Circuits and Signal Processing, 2007, 50, 7-12.	1.4	7
115	Characterization of a CMOS impedance tuning unit for DVB-H. Analog Integrated Circuits and Signal Processing, 2007, 52, 79-87.	1.4	5
116	A 850/900/1800/1900MHz Quad-Band CMOS Medium Power Amplifier. , 2006, , .		3
117	A 5.8 GHz 1.7 dB NF fully integrated differential low noise amplifier in CMOS. , 2006, , .		5
118	Full oscillation cycle phase noise analysis of differential CMOS LC oscillators. Analog Integrated Circuits and Signal Processing, 2006, 48, 211-222.	1.4	1
119	MONOLITHIC INDUCTOR MODELING AND OPTIMIZATION. , 2006, , 217-240.		1
120	Low Power 0.18 μm CMOS Dual-Band Front-End. , 2005, , .		0
121	A Distributed Capacitance Analysis of Co-Planar Inductors for a CMOS QVCO with Varactor Tuned Buffer Stage. Analog Integrated Circuits and Signal Processing, 2005, 42, 7-19.	1.4	10
122	A merged CMOS LNA and mixer for a WCDMA receiver. IEEE Journal of Solid-State Circuits, 2003, 38, 1045-1050.	5.4	110
123	Highly Linear Integrated Wideband Amplifiers. , 1999, , .		1
124	A Novel Class AB CMOS Power Amplifier. Analog Integrated Circuits and Signal Processing, 1997, 12, 49-58.	1.4	3