Michael Peter Kennedy

List of Publications by Year in descending order

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#	Article	IF	CITATIONS
1	A 12.9-to-15.1-GHz Digital PLL Based on a Bang-Bang Phase Detector With Adaptively Optimized Noise Shaping. IEEE Journal of Solid-State Circuits, 2022, 57, 1723-1735.	5.4	9
2	A random pulse modulation approach to modeling the flicker and white noise of the charge pump of a fractionalâ€N frequency synthesizer. International Journal of Circuit Theory and Applications, 2022, 50, 1049-1063.	2.0	2
3	Wandering Spurs in MASH-Based Fractional-N Frequency Synthesizers. Analog Circuits and Signal Processing Series, 2022, , .	0.3	1
4	Simulation of Phase Noise in a Fractional-N Frequency Synthesizer. Analog Circuits and Signal Processing Series, 2022, , 7-24.	0.3	0
5	Wandering Spur Suppression in a 4.9-GHz Fractional- <i>N</i> Frequency Synthesizer. IEEE Journal of Solid-State Circuits, 2022, 57, 2011-2023.	5.4	1
6	Nonlinearity-Induced Spurs in Fractional- <i>N</i> Frequency Synthesizers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2617-2622.	3.0	1
7	Immunity of ENOP-based Fractional-N Frequency Synthesizer to Wandering and Horn Spurs. , 2022, , .		0
8	MASH-Based Divider Controllers for Mitigation of Wandering Spurs in a Fractional- <i>N</i> Frequency Synthesizer. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 126-137.	5.4	4
9	32.8 A 98.4fs-Jitter 12.9-to-15.1GHz PLL-Based LO Phase-Shifting System with Digital Background Phase-Offset Correction for Integrated Phased Arrays. , 2021, , .		5
10	32.3 A 12.9-to-15.1GHz Digital PLL Based on a Bang-Bang Phase Detector with Adaptively Optimized Noise Shaping Achieving 107.6fs Integrated Jitter. , 2021, , .		8
11	Spur Immunity in MASH-Based Fractional-N CP-PLLs With Polynomial Nonlinearities. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2295-2306.	5.4	8
12	A Comprehensive Phase Noise Analysis of Bang-Bang Digital PLLs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2775-2786.	5.4	21
13	Folded Noise Prediction in Nonlinear Fractional-N Frequency Synthesizers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4038-4048.	5.4	4
14	An Algorithm for Implementing a Modulator Whose Output is Spur-Free After Nonlinear Distortion. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4259-4267.	5.4	0
15	Experimental Verification of Wandering Spur Suppression Technique in a 4.9 GHz Fractional-N Frequency Synthesizer. , 2021, , .		2
16	Modelling and Verification of Nonlinear Electromechanical Coupling in Micro-Scale Kinetic Electromagnetic Energy Harvesters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 565-577.	5.4	7
17	Analysis of Wandering Spur Patterns in a Fractional-\$N\$ Frequency Synthesizer With a MASH-Based Divider Controller. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 729-742.	5.4	10
18	Jitter Minimization in Digital PLLs with Mid-Rise TDCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 743-752.	5.4	18

#	Article	IF	CITATIONS
19	Comparison of Mathematical and Physical Phase Noise Performance in Fractional-N Synthesizers. , 2020, , .		1
20	Analysis and Prediction of Spurs in a Fractional-N Frequency Synthesizer with Discontinuous Nonlinearity. , 2020, , .		1
21	Near-Limit Kinetic Energy Harvesting From Arbitrary Acceleration Waveforms: Feasibility Study by the Example of Human Motion. IEEE Access, 2020, 8, 219223-219232.	4.2	0
22	Mitigation of "Horn Spurs―in a MASH-Based Fractional-N CP-PLL. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 821-825.	3.0	4
23	Influence of Initial Condition on Wandering Spur Pattern in a MASH-Based Fractional- <i>N</i> Frequency Synthesizer. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2968-2972.	3.0	4
24	Semi-Analytical Method for the Extraction of the System Parameters in Application to Kinetic Energy Harvesters. , 2019, , .		0
25	Prediction of Phase Noise and Spurs in a Nonlinear Fractional-\${N}\$ Frequency Synthesizer. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4108-4121.	5.4	26
26	Modelling of Electromagnetic Coupling in Micro-scale Electromagnetic Energy Harvester. , 2019, , .		0
27	4.48-GHz Fractional-\${N}\$ Frequency Synthesizer With Spurious-Tone Suppression via Probability Mass Redistribution. IEEE Solid-State Circuits Letters, 2019, 2, 264-267.	2.0	11
28	Wandering Spurs in MASH 1-1 Delta-Sigma Modulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2426-2439.	5.4	5
29	MASH DDSM-Induced Spurs in a Fractional-\$N\$ Frequency Synthesizer. , 2019, , .		3
30	Fat Sensing Using Low-Cost Near-Infrared Spectroscopy. , 2019, , .		2
31	Nonlinearity-Induced Spurs in Fractional- N Frequency Synthesizers: State of the Art. , 2019, , .		4
32	Observations concerning "Horn Spurs―in a MASH-based Fractional-N CP-PLL. , 2019, , .		3
33	Another moving Spur Phenomenon observed in a MASH-based Fractional-N PLL. , 2019, , .		2
34	A Design Method for Nested MASH-SQ Hybrid Divider Controllers for Fractional- <inline-formula> <tex-math notation="LaTeX">\$N\$ </tex-math> </inline-formula> Frequency Synthesizers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3279-3290.	5.4	4
35	Observations and Analysis of Wandering Spurs in MASH-Based Fractional- <inline-formula> <tex-math notation="LaTeX">\$N\$ </tex-math> </inline-formula> Frequency Synthesizers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 662-666.	3.0	11

36 Switched Capacitor Charge Pump Voltage-Controlled Current Source. , 2018, , .

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37	Novel Approach to Modelling Electromechanical Coupling and Testing its Self-Consistency in Micro-Scale Kinetic Electromagnetic Energy Harvesters. , 2018, , .		1
38	High-Speed Nested Cascaded MASH Digital Delta-Sigma Modulator-Based Divider Controller. , 2018, , .		3
39	Chaotic Modulation Schemes. , 2018, , 151-183.		0
40	Overview of Digital Communications. , 2018, , 131-149.		1
41	Influence of Initial Conditions on the Fundamental Periods of LFSR-Dithered MASH Digital Delta–Sigma Modulators With Constant Inputs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 372-376.	3.0	7
42	Masked Dithering of MASH Digital Delta-Sigma Modulators With Constant Inputs Using Multiple Linear Feedback Shift Registers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1390-1399.	5.4	10
43	Performance limits for open-loop fractional dividers. , 2017, , .		2
44	A comparison of simulation strategies for estimating phase noise in oscillators. , 2017, , .		1
45	Observations of the differences between closed-loop behavioral and feed-forward model simulations of fractional-N frequency synthesizers. , 2017, , .		1
46	Phase noise in fractional-N frequency synthesizers employing successive requantizers and MASH-SQ hybrids. , 2017, , .		0
47	Nonlinearity-induced spurious tones and noise in digitally-assisted frequency synthesizers. , 2017, , .		2
48	Masked Dithering of MASH Digital Delta-Sigma Modulators with Constant Inputs Using Linear Feedback Shift Registers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1131-1141.	5.4	10
49	On the statistical properties of phase noise in Fractional-N frequency synthesizers using successive requantizers. , 2016, , .		2
50	Yet another spur mechanism in a charge-pump based Fractional-N PLL. , 2016, , .		3
51	Maximizing the fundamental period of a dithered digital delta-sigma modulator with constant input. , 2016, , .		0
52	A method to quantify the dependence of spur heights on offset current in a CP-PLL. , 2016, , .		0
53	Comparative analysis of differential colpitts and cross-coupled VCOs in 180 nm Si-Ge HBT technology. , 2016, , .		6
54	The low power and wide tuning range advantages of Armstrong VCOs in 180 nm Si-Ge HBT technology. , 2016, , .		1

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55	A back-to-back series varactor configuration minimizing the amplitude-to-phase noise conversion in Si-Ge HBT technology VCOs. , 2016, , .		2
56	Comparison of the simulated performance of two divider controllers in a fractional-N frequency synthesizer with a piecewise-linear charge-pump nonlinearity. , 2016, , .		0
57	Comparison of analytical predictions of the noise floor due to static charge pump mismatch in fractional-n frequency synthesizers. , 2016, , .		3
58	The noise and spur delusion in fractional-N frequency synthesizer design. , 2015, , .		6
59	Phase noise and spur performance limits for fractional-N frequency synthesizers. , 2015, , .		4
60	Spurious tones in digital delta-sigma modulators resulting from pseudorandom dither. Journal of the Franklin Institute, 2015, 352, 3325-3344.	3.4	11
61	Effective (Spur-Free) dithering of digital delta-sigma modulators with pseudorandom dither. , 2015, , .		3
62	Comparison of a feed-forward phase domain model and a time domain behavioral model for predicting mismatch-related noise floor and spurs in fractional-N frequency synthesizers. , 2015, , .		6
63	Noise-Shaping All-Digital Phase-Locked Loops. Analog Circuits and Signal Processing Series, 2014, , .	0.3	9
64	Comments on efficient dithering in digital delta-sigma modulator. , 2014, , .		5
65	0.3–4.3 GHz Frequency-Accurate Fractional-\$N\$ Frequency Synthesizer With Integrated VCO and Nested Mixed-Radix Digital \$Delta\$-\$Sigma\$ Modulator-Based Divider Controller. IEEE Journal of Solid-State Circuits, 2014, 49, 1595-1605.	5.4	3
66	Observations concerning PFD/CP operating point offset strategies for combatting static charge pump mismatch in fractional- <l>N</l> frequency synthesizers with digital delta-sigma modulators. Nonlinear Theory and Its Applications IEICE, 2014, 5, 349-364.	0.6	9
67	Phase Digitization in All-Digital PLLs. Analog Circuits and Signal Processing Series, 2014, , 7-38.	0.3	0
68	Efficient Modeling and Simulation of Accumulator-Based ADPLLs. Analog Circuits and Signal Processing Series, 2014, , 111-141.	0.3	0
69	Measurement Technique for Experimentally Estimating the Phase Sensitivity Function of an Oscillator. IEICE Proceeding Series, 2014, 1, 856-859.	0.0	0
70	Dynamically Reconfigurable Switched-Capacitor DC-DC Converters. IEICE Proceeding Series, 2014, 1, 280-283.	0.0	0
71	The Switched Injection-Locked Oscillator (SILO) Concept. IEICE Proceeding Series, 2014, 1, 868-871.	0.0	1
72	A CMOS Injection-Locked Frequency Divider Optimized for Divide-by-Two and Divide-by-Three Operation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 3126-3135.	5.4	28

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73	A high frequency "divide-by-odd number―CMOS LC injection-locked frequency divider. Analog Integrated Circuits and Signal Processing, 2013, 77, 415-421.	1.4	2
74	Spurious tones in digital delta sigma modulators with pseudorandom dither. , 2013, , .		7
75	Experimental validation of DAC with nested bus-splitting EFM4 DDSM. , 2013, , .		Ο
76	The Role of Charge Pump Mismatch in the Generation of Integer Boundary Spurs in Fractional-N Frequency Synthesizers: Why Worse Can Be Better. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 862-866.	3.0	20
77	A high-throughput spur-free hybrid nested bus-splitting/HK-MASH digital delta-sigma modulator. , 2013, , .		4
78	High speed, high accuracy fractional-N frequency synthesizer using nested mixed-radix digital Δ-Σ modulators. , 2013, , .		1
79	Programmable analog frequency divider based on <1>ρ-switching. Nonlinear Theory and Its Applications IEICE, 2013, 4, 389-399.	0.6	3
80	Recent advances in the analysis, design and optimization of Digital Delta-Sigma Modulators. Nonlinear Theory and Its Applications IEICE, 2012, 3, 258-286.	0.6	6
81	A fast charge pump PLL using a bang-bang frequency comparator with dead zone. , 2012, , .		4
82	A "divide-by-odd number" direct injection CMOS LC injection-locked frequency divider. , 2012, , .		4
83	Hardware Reduction in Digital Delta-Sigma Modulators via Bus-Splitting and Error Masking—Part II: Non-Constant Input. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1980-1991.	5.4	12
84	Hardware Reduction in Digital Delta-Sigma Modulators Via Bus-Splitting and Error Masking—Part I: Constant Input. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2137-2148.	5.4	23
85	Observations Concerning the Locking Range in a Complementary Differential \$LC\$ Injection-Locked Frequency Divider—Part II: Design Methodology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 765-776.	5.4	18
86	A novel implementation of dithered digital delta-sigma modulators via bus-splitting. , 2011, , .		3
87	Observations Concerning the Generation of Spurious Tones in Digital Delta-Sigma Modulators Followed by a Memoryless Nonlinearity. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 714-718.	3.0	20
88	Minimizing Spurious Tones in Digital Delta-Sigma Modulators. , 2011, , .		41
89	On the Synchronization Condition for Superharmonic Coupled QVCOs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 1637-1646.	5.4	25
90	Calculation of Cycle Lengths in Higher Order Error Feedback Modulators With Constant Inputs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 6-10.	3.0	6

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91	A Spur-Free MASH DDSM With High-Order Filtered Dither. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 585-589.	3.0	7
92	First order noise shaping in all digital PLLs. , 2011, , .		1
93	Phenomenological study of an injection-locked CMOS LC frequency divider with direct injection. , 2011, , .		3
94	Conventional Techniques for Maximizing Cycle Lengths. , 2011, , 43-94.		0
95	HK-EFM and HK-SQ-DDSM. , 2011, , 117-129.		0
96	On the synchronization condition of second-harmonic coupled QVCOs. , 2010, , .		1
97	A qualitative analysis of a complementary differential LC injection-locked frequency divider based on direct injection. , 2010, , .		3
98	Analysis and Design of Injection-Locked Frequency Dividers by Means of a Phase-Domain Macromodel. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2956-2966.	5.4	12
99	Prediction of the Spectrum of a Digital Delta–Sigma Modulator Followed by a Polynomial Nonlinearity. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1905-1913.	5.4	14
100	Calculation of cycle lengths in higher-order MASH DDSMs with constant inputs. , 2010, , .		1
101	Calculation of the cycle length in a HK-MASH DDSM with multilevel quantizers. , 2010, , .		0
102	Observations Concerning the Locking Range in a Complementary Differential \$LC\$ Injection-Locked Frequency Divider—Part I: Qualitative Analysis. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 179-188.	5.4	29
103	Comparison of ring and LC oscillator-based ILFDs in terms of phase noise, locking range, power consumption and quality factor. , 2009, , .		6
104	Hardware Reduction in Digital Delta–Sigma Modulators Via Error Masking—Part II: SQ-DDSM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 112-116.	3.0	14
105	Hardware Reduction in Digital Delta-Sigma Modulators Via Error Masking - Part I: MASH DDSM. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 714-726.	5.4	15
106	Calculation of cycle lengths in MASH 1-2-2 digital delta sigma modulators with a constant input. , 2009, , .		0
107	A spur-free MASH digital delta-sigma modulator with higher order shaped dither. , 2009, , .		4
108	Design methodology for a dithered reduced complexity Digital MASH Delta-Sigma Modulator. , 2008, , .		0

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109	Design methodology for a reduced complexity single quantizer digital delta-sigma modulator. , 2008, ,		0
110	Hardware reduction in digital MASH delta-sigma modulators via error masking. , 2008, , .		2
111	Statistical Properties of First-Order Bang-Bang PLL With Nonzero Loop Delay. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 1016-1020.	3.0	19
112	Architectures for Maximum-Sequence-Length Digital Delta-Sigma Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 1104-1108.	3.0	20
113	Analysis and design of an LC oscillator-based injection-locked frequency divider. , 2008, , .		Ο
114	Design methodology for a divide-by-4 LC injection-locked frequency divider based on nonlinear analysis. , 2008, , .		0
115	Optimizing the design of an injection-locked frequency divider by means of nonlinear analysis. , 2007, ,		11
116	Calculation of sequence lengths in MASH 1-1-1 digital delta sigma modulators with a constant input. , 2007, , .		10
117	Reduced Complexity MASH Delta–Sigma Modulator. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 725-729.	2.2	20
118	A novel dual-loop multi-phase frequency synthesizer. , 2007, , .		0
119	Noise reduction in fractional-N frequency synthesizers with multiphase VCO. , 2007, , .		2
120	Maximum Sequence Length MASH Digital Delta–Sigma Modulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2007, 54, 2628-2638.	5.4	82
121	Mathematical Analysis of a Prime Modulus Quantizer MASH Digital Delta–Sigma Modulator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 1105-1109.	3.0	33
122	Hard-Fault Detection and Diagnosis During the Application of Model-Based Data Converter Testing. Journal of Electronic Testing: Theory and Applications (JETTA), 2007, 23, 513-525.	1.2	2
123	Modeling and Simulation of ÂÂ Fractional-N PLL Frequency Synthesizer in Verilog-AMS. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2007, E90-A, 2141-2147.	0.3	8
124	Performance analysis of low power high speed pipelined adders for digital modulators. Electronics Letters, 2006, 42, 1442.	1.0	3
125	Use of the Step Invariant Transform to Design a 2nd Order Continuous Time Complex Sigma-Delta ADC. , 2006, , .		0
126	Test Development Through Defect and Test Escape Level Estimation for Data Converters. Journal of Electronic Testing: Theory and Applications (JETTA), 2006, 22, 313-324.	1.2	9

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127	Overcoming Test Setup Limitations by Applying Model-Based Testing to High-Precision ADCs. Journal of Electronic Testing: Theory and Applications (JETTA), 2005, 21, 299-310.	1.2	6
128	A FAST AND SIMPLE IMPLEMENTATION OF CHUA'S OSCILLATOR WITH CUBIC-LIKE NONLINEARITY. International Journal of Bifurcation and Chaos in Applied Sciences and Engineering, 2005, 15, 2959-2971.	1.7	52
129	ON THE APPROXIMATE ONE-D MAP IN CHUA'S OSCILLATOR. International Journal of Bifurcation and Chaos in Applied Sciences and Engineering, 2005, 15, 2545-2550.	1.7	1
130	Influence of noise intensity on the spectrum of an oscillator. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2005, 52, 789-793.	2.2	17
131	A General Method to Predict the Amplitude of Oscillation in Nearly Sinusoidal Oscillators. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 1586-1595.	0.1	24
132	Testing ADCs for static and dynamic INL—killing two birds with one stone. Computer Standards and Interfaces, 2004, 26, 15-20.	5.4	5
133	Heterodimensional FET With Split Drain. IEEE Electron Device Letters, 2004, 25, 737-739.	3.9	2
134	Linear Model-Based Testing of ADC Nonlinearities. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 213-217.	0.1	25
135	A FOUR-WING BUTTERFLY ATTRACTOR FROM A FULLY AUTONOMOUS SYSTEM. International Journal of Bifurcation and Chaos in Applied Sciences and Engineering, 2003, 13, 3093-3098.	1.7	46
136	EXPERIMENTAL VERIFICATION OF THE BUTTERFLY ATTRACTOR IN A MODIFIED LORENZ SYSTEM. International Journal of Bifurcation and Chaos in Applied Sciences and Engineering, 2002, 12, 1627-1632.	1.7	56
137	AN EQUATION FOR GENERATING CHAOS AND ITS MONOLITHIC IMPLEMENTATION. International Journal of Bifurcation and Chaos in Applied Sciences and Engineering, 2002, 12, 2885-2895.	1.7	41
138	Correlator-Based Chaotic Communications: Attainable Noise and Multipath Performance. World Scientific Series on Nonlinear Science, Series B, 2002, , 443-485.	0.2	2
139	Creation of a complex butterfly attractor using a novel Lorenz-Type system. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2002, 49, 527-530.	0.1	108
140	Chaotic communications with correlator receivers: theory and performance limits. Proceedings of the IEEE, 2002, 90, 711-732.	21.3	127
141	Construction of classes of circuit-independent chaotic oscillators using passive-only nonlinear devices. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2001, 48, 289-307.	0.1	215
142	Title is missing!. Journal of Electronic Testing: Theory and Applications (JETTA), 2001, 17, 409-416.	1.2	2
143	Chaotic oscillator configuration using a frequency dependent negative resistor. International Journal of Circuit Theory and Applications, 2000, 28, 69-76.	2.0	23
144	Systematic realization of a class of hysteresis chaotic oscillators. International Journal of Circuit Theory and Applications, 2000, 28, 319-334.	2.0	23

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145	Chua's circuit decomposition: a systematic design approach for chaotic oscillators. Journal of the Franklin Institute, 2000, 337, 251-265.	3.4	43
146	A low-voltage, low-power, chaotic oscillator, derived from a relaxation oscillator. Microelectronics Journal, 2000, 31, 459-468.	2.0	17
147	Digital communications using chaos. Signal Processing, 2000, 80, 1307-1320.	3.7	121
148	Chaotic Oscillators Derived from Sinusoidal Oscillators Based on the Current Feedback Op Amp. Analog Integrated Circuits and Signal Processing, 2000, 24, 239-251.	1.4	19
149	A semi-systematic procedure for producing chaos from sinusoidal oscillators using diode-inductor and FET-capacitor composites. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2000, 47, 582-590.	0.1	37
150	Performance evaluation of FM-DCSK modulation in multipath environments. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2000, 47, 1702-1711.	0.1	114
151	Novel chaotic oscillator configuration using a diode-inductor composite. International Journal of Electronics, 2000, 87, 397-406.	1.4	15
152	Nonsmooth bifurcations in a piecewise-linear model of the Colpitts oscillator. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2000, 47, 1160-1177.	0.1	72
153	GENERIC RC REALIZATIONS OF CHUA'S CIRCUIT. International Journal of Bifurcation and Chaos in Applied Sciences and Engineering, 2000, 10, 1981-1985.	1.7	24
154	THE COLPITTS OSCILLATOR: FAMILIES OF PERIODIC SOLUTIONS AND THEIR BIFURCATIONS. International Journal of Bifurcation and Chaos in Applied Sciences and Engineering, 2000, 10, 935-958.	1.7	66
155	CHAOTIC MODULATION FOR ROBUST DIGITAL COMMUNICATIONS OVER MULTIPATH CHANNELS. International Journal of Bifurcation and Chaos in Applied Sciences and Engineering, 2000, 10, 695-718.	1.7	28
156	Improved implementation of Chua's chaotic oscillator using current feedback op amp. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2000, 47, 76-79.	0.1	110
157	On the robustness of R-2R ladder DACs. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2000, 47, 109-116.	0.1	35
158	Communications using chaos≫MINUS. III. Performance bounds for correlation receivers. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2000, 47, 1673-1683.	0.1	105
159	IMPROVED NONLINEAR MODEL OF A SECOND-ORDER CHARGE-PUMP PLL. , 2000, , .		1
160	CHAOTIC OSCILLATOR CONFIGURATION USING A FREQUENCY DEPENDENT NEGATIVE RESISTOR. Journal of Circuits, Systems and Computers, 1999, 09, 229-242.	1.5	20
161	Inductorless hyperchaos generator. Microelectronics Journal, 1999, 30, 739-743.	2.0	23
162	Three-phase oscillator modified for chaos. Microelectronics Journal, 1999, 30, 863-867.	2.0	9

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163	A family of Colpitts-like chaotic oscillators. Journal of the Franklin Institute, 1999, 336, 687-700.	3.4	33
164	A rigorous exposition of the LEMMA method for analog and mixed-signal testing. IEEE Transactions on Instrumentation and Measurement, 1999, 48, 978-985.	4.7	18
165	Nonlinear analysis of the Colpitts oscillator and applications to design. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1999, 46, 1118-1130.	0.1	207
166	High frequency Wien-type chaotic oscillator. Electronics Letters, 1998, 34, 1161.	1.0	40
167	The role of synchronization in digital communications using chaos. II. Chaotic modulation and chaotic synchronization. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1998, 45, 1129-1140.	0.1	355
168	Devaney Chaos in an Approximate One-Dimensional Model of the Colpitts Oscillator. International Journal of Bifurcation and Chaos in Applied Sciences and Engineering, 1997, 07, 2561-2568.	1.7	5
169	The role of synchronization in digital communications using chaos. I . Fundamentals of digital communications. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1997, 44, 927-936.	0.1	287
170	Applications of Chaos in Communications. , 1997, , 243-261.		1
171	Electronic chaos controller. Chaos, Solitons and Fractals, 1997, 8, 1471-1484.	5.1	15
172	Experimental chaos from autonomous electronic circuits. Philosophical Transactions of the Royal Society: Physical and Engineering Sciences, 1995, 353, 13-32.	1.0	17
173	A NONLINEAR DYNAMICS INTERPRETATION OF ALGORITHMIC A/D CONVERSION. International Journal of Bifurcation and Chaos in Applied Sciences and Engineering, 1995, 05, 891-893.	1.7	4
174	SYNCHRONIZATION THEOREM FOR A CHAOTIC SYSTEM. International Journal of Bifurcation and Chaos in Applied Sciences and Engineering, 1995, 05, 297-302.	1.7	17
175	On the relationship between the chaotic Colpitts oscillator and Chua's oscillator. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1995, 42, 376-379.	0.1	43
176	Predictive Poincaré control: A control theory for chaotic systems. Physical Review E, 1995, 52, 4865-4876.	2.1	52
177	ABC (adventures in bifurcations and chaos): A program for studying chaos. Journal of the Franklin Institute, 1994, 331, 631-658.	3.4	3
178	Chaos in the Colpitts oscillator. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1994, 41, 771-774.	0.1	330
179	Synthesis of continuous threeâ€segment voltageâ€controlled piecewiseâ€linear resistors for Chua's circuit family using operational amplifiers, diodes and linear resistors. International Journal of Circuit Theory and Applications, 1993, 21, 551-558.	2.0	5
180	Chaos shift keying: modulation and demodulation of a chaotic carrier using self-synchronizing Chua's circuits. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1993, 40, 634-642.	2.2	686

#	Article	IF	CITATIONS
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