Hai Helen Li

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/8726378/publications.pdf

Version: 2024-02-01

309	6,952	270111	252626
papers	citations	25 h-index	46 g-index

311	311	311	4601
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	DyNNamic: Dynamically Reshaping, High Data-Reuse Accelerator for Compact DNNs. IEEE Transactions on Computers, 2023, 72, 880-892.	2.4	0
2	Guest Editorsâ€™ Introduction: Near-Memory and In-Memory Processing. IEEE Design and Test, 2022, 39, 46-47.	1.1	0
3	AccuReD: High Accuracy Training of CNNs on ReRAM/GPU Heterogeneous 3-D Architecture. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 971-984.	1.9	28
4	Efficient neural network using pointwise convolution kernels with linear phase constraint. Neurocomputing, 2021, 423, 572-579.	3.5	12
5	Connection-based Processing-In-Memory Engine Design Based on Resistive Crossbars. , 2021, , .		1
6	Exploring Applications of STT-RAM in GPU Architectures. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 238-249.	3.5	5
7	Line Art Correlation Matching Feature Transfer Network for Automatic Animation Colorization. , 2021, , .		7
8	RAISE: A Resistive Accelerator for Subject-Independent EEG Signal Classification. , 2021, , .		0
9	Efficient AUTOSAR-Compliant CAN-FD Frame Packing with Observed Optimality. , 2021, , .		1
10	Marvel: A Vertical Resistive Accelerator for Low-Power Deep Learning Inference in Monolithic 3D. , 2021, , .		3
11	An Efficient Programming Framework for Memristor-based Neuromorphic Computing. , 2021, , .		4
12	BitSystolic: A 26.7 TOPS/W 2b~8b NPU With Configurable Data Flows for Edge Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1134-1145.	3.5	8
13	An Efficient 3D ReRAM Convolution Processor Design for Binarized Weight Networks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1600-1604.	2.2	8
14	1S1R-Based Stable Learning through Single-Spike-Encoded Spike-Timing-Dependent Plasticity. , 2021, , .		0
15	An Overview of Hardware Security and Trust: Threats, Countermeasures, and Design Tools. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1010-1038.	1.9	56
16	Efficient FPGA Implementation of a Convolutional Neural Network for Radar Signal Processing. , 2021, , .		1
17	Defending against GAN-based DeepFake Attacks via Transformation-aware Adversarial Faces. , 2021, , .		13
18	TPrune. ACM Transactions on Cyber-Physical Systems, 2021, 5, 1-22.	1.9	20

#	Article	IF	Citations
19	Learning to Train CNNs on Faulty ReRAM-based Manycore Accelerators. Transactions on Embedded Computing Systems, 2021, 20, 1-23.	2.1	9
20	Soteria: Provable Defense against Privacy Leakage in Federated Learning from Representation Perspective. , 2021, , .		54
21	Neuromorphic Algorithm-hardware Codesign for Temporal Pattern Learning. , 2021, , .		9
22	Peripheral Circuitry Assisted Mapping Framework for Resistive Logic-In-Memory Computing. , 2021, , .		1
23	Multi-Objective Optimization of ReRAM Crossbars for Robust DNN Inferencing under Stochastic Noise. , 2021, , .		16
24	Rerec: In-ReRAM Acceleration with Access-Aware Mapping for Personalized Recommendation. , 2021, , .		9
25	Thwarting Replication Attack Against Memristor-Based Neuromorphic Computing System. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2192-2205.	1.9	10
26	A low-cost and high-speed hardware implementation of spiking neural network. Neurocomputing, 2020, 382, 106-115.	3.5	20
27	ReSiPE: ReRAM-based Single-Spiking Processing-In-Memory Engine. , 2020, , .		9
28	Lattice: An ADC/DAC-less ReRAM-based Processing-In-Memory Architecture for Accelerating Deep Convolution Neural Networks. , 2020, , .		21
29	Adversarial Attack: A New Threat to Smart Devices and How to Defend It. IEEE Consumer Electronics Magazine, 2020, 9, 49-55.	2.3	7
30	Learning Low-rank Deep Neural Networks via Singular Vector Orthogonality Regularization and Singular Value Sparsification. , 2020, , .		13
31	Redistributing and Re-Stylizing Features for Training a Fast Photorealistic Stylizer. , 2020, , .		0
32	Neuromorphic Computing Systems with Emerging Nonvolatile Memories: A Circuits and Systems Perspective. , 2020, , .		0
33	Leveraging 3D Vertical RRAM to Developing Neuromorphic Architecture for Pattern Classification. , 2020, , .		6
34	Introduction to the Special Issue on the 2nd IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS 2020). IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 403-405.	2.7	1
35	Conditional Transferring Features: Scaling GANs to Thousands of Classes with 30% Less High-Quality Data for Training. , 2020, , .		3
36	Lifetime Enhancement for RRAM-based Computing-In-Memory Engine Considering Aging and Thermal Effects. , 2020, , .		19

#	Article	IF	Citations
37	Structural Sparsification for Far-Field Speaker Recognition with IntelÂ® Gna. , 2020, , .		0
38	GRAMARCH: A GPU-ReRAM based Heterogeneous Architecture for Neural Image Segmentation. , 2020, , .		5
39	A Pulse-width Modulation Neuron with Continuous Activation for Processing-In-Memory Engines. , 2020, , .		4
40	FCDM: A Methodology Based on Sensor Pattern Noise Fingerprinting for Fast Confidence Detection to Adversarial Attacks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4791-4804.	1.9	1
41	AccPar: Tensor Partitioning for Heterogeneous Deep Learning Accelerators. , 2020, , .		24
42	Enhancing Generalization of Wafer Defect Detection by Data Discrepancy-aware Preprocessing and Contrast-varied Augmentation. , 2020, , .		0
43	Parallelism in Deep Learning Accelerators. , 2020, , .		0
44	PARC: A Processing-in-CAM Architecture for Genomic Long Read Pairwise Alignment using ReRAM. , 2020, , .		15
45	RED: A ReRAM-Based Efficient Accelerator for Deconvolutional Computation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4736-4747.	1.9	8
46	Neural Predictor for Neural Architecture Search. Lecture Notes in Computer Science, 2020, , 660-676.	1.0	47
47	3D-ReG. ACM Journal on Emerging Technologies in Computing Systems, 2020, 16, 1-24.	1.8	14
48	AutoGrow: Automatic Layer Growing in Deep Convolutional Networks. , 2020, , .		8
49	ReTransformer. , 2020, , .		35
50	A Case for 3D Integrated System Design for Neuromorphic Computing and AI Applications. International Journal of Semantic Computing, 2020, 14, 457-475.	0.4	2
51	Highly efficient neuromorphic computing systems with emerging nonvolatile memories. , 2020, , .		0
52	ReBoc: Accelerating Block-Circulant Neural Networks in ReRAM. , 2020, , .		3
53	AutoShrink: A Topology-Aware NAS for Discovering Efficient Neural Architecture. Proceedings of the AAAI Conference on Artificial Intelligence, 2020, 34, 6829-6836.	3.6	8
54	Reliable and Robust RRAM-based Neuromorphic Computing. , 2020, , .		6

#	Article	IF	Citations
55	MobiLatice. , 2020, , .		7
56	Fast IR drop estimation with machine learning. , 2020, , .		15
57	Resistive Memoryâ€Based Inâ€Memory Computing: From Device and Largeâ€Scale Integration System Perspectives. Advanced Intelligent Systems, 2019, 1, 1900068.	3.3	54
58	Exploration of Automatic Mixed-Precision Search for Deep Neural Networks. , 2019, , .		2
59	MobiEye. , 2019, , .		9
60	Learning Efficient Sparse Structures in Speech Recognition. , 2019, , .		3
61	ReBNN: in-situ acceleration of binarized neural networks in ReRAM using complementary resistive cell. CCF Transactions on High Performance Computing, 2019, 1, 196-208.	1.1	11
62	Enhance the Robustness to Time Dependent Variability of ReRAM-Based Neuromorphic Computing Systems with Regularization and 2R Synapse. , 2019, , .		4
63	An Overview of In-memory Processing with Emerging Non-volatile Memory for Data-intensive Applications. , 2019, , .		24
64	RRAM-based Spiking Nonvolatile Computing-In-Memory Processing Engine with Precision-Configurable In Situ Nonlinear Activation. , 2019, , .		40
65	RED: A ReRAM-based Deconvolution Accelerator. , 2019, , .		12
66	Aging-aware Lifetime Enhancement for Memristor-based Neuromorphic Computing. , 2019, , .		37
67	Build reliable and efficient neuromorphic design with memristor technology. , 2019, , .		17
68	AdverQuil. , 2019, , .		0
69	Towards Decentralized Deep Learning with Differential Privacy. Lecture Notes in Computer Science, 2019, , 130-145.	1.0	8
70	ZARA. , 2019, , .		24
71	REGENT: A Heterogeneous ReRAM/GPU-based Architecture Enabled by NoC for Training CNNs. , 2019, , .		13
72	HyPar: Towards Hybrid Parallelism for Deep Learning Accelerator Array. , 2019, , .		64

#	Article	IF	Citations
73	NeuralHMC. , 2019, , .		9
74	Feedback Learning for Improving the Robustness of Neural Networks. , 2019, , .		2
75	Joint Regularization on Activations and Weights for Efficient Neural Network Pruning. , 2019, , .		2
76	DASNet: Dynamic Activation Sparsity for Neural Network Efficiency Improvement. , 2019, , .		7
77	MSNet: Structural Wired Neural Architecture Search for Internet of Things. , 2019, , .		10
78	Taming extreme heterogeneity via machine learning based design of autonomous manycore systems. , 2019, , .		3
79	How to Obtain and Run Light and Efficient Deep Learning Networks. , 2019, , .		1
80	Feature Space Perturbations Yield More Transferable Adversarial Examples. , 2019, , .		80
81	On Designing Efficient and Reliable Nonvolatile Memory-Based Computing-In-Memory Accelerators. , 2019, , .		5
82	RC-NVM: Dual-Addressing Non-Volatile Memory Architecture Supporting Both Row and Column Memory Accesses. IEEE Transactions on Computers, 2019, 68, 239-254.	2.4	8
83	Exploiting Spin-Orbit Torque Devices As Reconfigurable Logic for Circuit Obfuscation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 57-69.	1.9	21
84	Exploring Bit-Slice Sparsity in Deep Neural Networks for Efficient ReRAM-Based Deployment. , 2019, , .		5
85	Thread Batching for High-performance Energy-efficient GPU Memory Design. ACM Journal on Emerging Technologies in Computing Systems, 2019, 15, 1-21.	1.8	1
86	Spintronics based stochastic computing for efficient Bayesian inference system. , 2018, , .		15
87	Guest Editorial Circuit and System Design Automation for Internet of Things. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 3-6.	1.9	2
88	TriZone: A Design of MLC STT-RAM Cache for Combined Performance, Energy, and Reliability Optimizations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1985-1998.	1.9	3
89	Modeling of biaxial magnetic tunneling junction for multi-level cell STT-RAM realization. , 2018, , .		2
90	GraphR: Accelerating Graph Processing Using ReRAM. , 2018, , .		169

#	Article	IF	Citations
91	ReRAM-based accelerator for deep learning. , 2018, , .		21
92	RC-NVM: Enabling Symmetric Row and Column Memory Accesses for In-memory Databases. , 2018, , .		14
93	Low-Power, Adaptive Neuromorphic Systems: Recent Progress and Future Directions. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 6-27.	2.7	78
94	Process variation aware data management for magnetic skyrmions racetrack memory. , 2018, , .		8
95	A compact model for selectors based on metal doped electrolyte. Applied Physics A: Materials Science and Processing, 2018, 124, 1.	1.1	2
96	Running sparse and low-precision neural network: When algorithm meets hardware. , 2018, , .		12
97	Shift-Optimized Energy-Efficient Racetrack-Based Main Memory. Journal of Circuits, Systems and Computers, 2018, 27, 1850081.	1.0	5
98	Neuromorphic computing's yesterday, today, and tomorrow â€“ an evolutional view. The Integration VLSI Journal, 2018, 61, 49-61.	1.3	25
99	SPN dash. , 2018, , .		1
100	Real-Time Cardiac Arrhythmia Classification Using Memristor Neuromorphic Computing System. , 2018, 2018, 2567-2570.		6
101	A Neuromorphic Design Using Chaotic Mott Memristor with Relaxation Oscillation. , 2018, , .		1
102	EMAT. , 2018, , .		8
103	Guest Editorial: Special Issue on Large-Scale Memristive Systems and Neurochips for Computational Intelligence. IEEE Transactions on Emerging Topics in Computational Intelligence, 2018, 2, 320-323.	3.4	3
104	Atomlayer. , 2018, , .		63
105	(Invited) Beyond CMOS: Memristor and Its Application for Next Generation Storage and Computing. ECS Transactions, 2018, 85, 115-125.	0.3	1
106	Neu-NoC: A high-efficient interconnection network for accelerated neuromorphic systems. , 2018, , .		40
107	A Quantized Training Method to Enhance Accuracy of ReRAM-based Neuromorphic Systems. , 2018, , .		9
108	A neuromorphic design using chaotic mott memristor with relaxation oscillation. , 2018, , .		0

#	Article	IF	Citations
109	Challenges of memristor based neuromorphic computing system. Science China Information Sciences, 2018, 61, 1.	2.7	17
110	Design and Data Management for Magnetic Racetrack Memory. , 2018, , .		2
111	Exploring the opportunity of implementing neuromorphic computing systems with spintronic devices. , 2018, , .		3
112	ReCom: An efficient resistive accelerator for compressed deep neural networks. , 2018, , .		46
113	Guest Editorial Low-Power, Adaptive Neuromorphic Systems: Devices, Circuit, Architectures and Algorithms. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 1-5.	2.7	0
114	MAT: A Multi-strength Adversarial Training Method to Mitigate Adversarial Attacks. , 2018, , .		12
115	Pulse-Width Modulation based Dot-Product Engine for Neuromorphic Computing System using Memristor Crossbar Array. , 2018, , .		17
116	In-place Logic Obfuscation for Emerging Nonvolatile FPGAs. , 2017, , 277-293.		0
117	Extending the lifetime of object-based NAND flash device with STT-RAM/DRAM hybrid buffer. , 2017, , .		3
118	Classification accuracy improvement for neuromorphic computing systems with one-level precision synapses. , 2017, , .		11
119	Cross-Layer Optimization for Multilevel Cell STT-RAM Caches. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1807-1820.	2.1	11
120	A memristor-based neuromorphic engine with a current sensing scheme for artificial neural network applications. , 2017, , .		21
121	PipeLayer: A Pipelined ReRAM-Based Accelerator for Deep Learning. , 2017, , .		525
122	Giant Spin-Hall assisted STT-RAM and logic design. The Integration VLSI Journal, 2017, 58, 253-261.	1.3	5
123	Group Scissor. , 2017, , .		26
124	Hybrid spiking-based multi-layered self-learning neuromorphic system based on memristor crossbar arrays. , 2017, , .		9
125	Understanding the design of IBM neurosynaptic system and its tradeoffs: A user perspective. , 2017, , .		17
126	An Energy-Efficient GPGPU Register File Architecture Using Racetrack Memory. IEEE Transactions on Computers, 2017, 66, 1478-1490.	2.4	15

#	Article	IF	Citations
127	Recent Technology Advances of Emerging Memories. IEEE Design and Test, 2017, 34, 8-22.	1.1	21
128	Looking Ahead for Resistive Memory Technology: A broad perspective on ReRAM technology for future storage and computing. IEEE Consumer Electronics Magazine, 2017, 6, 94-103.	2.3	31
129	Brain-inspired computing accelerated by memristor technology. , 2017, , .		2
130	Hardware implementation of echo state networks using memristor double crossbar arrays. , 2017, , .		26
131	Rescuing Memristor-based Neuromorphic Design with High Defects. , 2017, , .		158
132	An FPGA Design Framework for CNN Sparsification and Acceleration. , 2017, , .		17
133	A Compact Memristor-Based Dynamic Synapse for Spiking Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1353-1366.	1.9	81
134	FlexLevel NAND Flash Storage System Design to Reduce LDPC Latency. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1167-1180.	1.9	14
135	MobiCore: An adaptive hybrid approach for power-efficient CPU management on Android devices. , 2017, , .		5
136	A quantization-aware regularized learning method in multilevel memristor-based neuromorphic computing system. , 2017, , .		21
137	Guest Editorial Special Issue on Nanoelectronic Devices and Circuits for Next Generation Sensing and Information Processing. IEEE Nanotechnology Magazine, 2017, 16, 383-386.	1.1	1
138	A Compact DNN: Approaching GoogLeNet-Level Accuracy of Classification and Domain Adaptation. , 2017, , .		39
139	Coordinating Filters for Faster Deep Neural Networks. , 2017, , .		72
140	The New Large-Scale RNNLM System Based on Distributed Neuron. , 2017, , .		3
141	Understanding the trade-offs of device, circuit and application in ReRAM-based neuromorphic computing systems. , 2017, , .		11
142	A closed-loop design to enhance weight stability of memristor based neural network chips. , 2017, , .		27
143	MeDNN: A distributed mobile system with enhanced partition and deployment for large-scale DNNs. , 2017, , .		58
144	AdaLearner: An adaptive distributed mobile learning system for neural networks. , 2017, , .		7

#	Article	IF	Citations
145	The Prospect of STT-RAM Scaling. , 2017, , 71-104.		0
146	Array organization and data management exploration in racetrack memory. IEEE Transactions on Computers, 2016, 65, 1041-1054.	2.4	23
147	Built-in selectors self-assembled into memristors. , 2016, , .		1
148	Design techniques of eNVM-enabled neuromorphic computing systems. , 2016, , .		4
149	ApesNet. , 2016, , .		6
150	Security of neuromorphic systems: Challenges and solutions. , 2016, , .		10
151	A data locality-aware design framework for reconfigurable sparse matrix-vector multiplication kernel. , 2016, , .		8
152	RAM and TCAM designs by using STT-MRAM. , 2016, , .		5
153	A new learning method for inference accuracy, core occupation, and performance co-optimization on TrueNorth chip. , 2016, , .		20
154	Security of neuromorphic computing. , 2016, , .		11
155	Security challenges in smart surveillance systems and the solutions based on emerging nano-devices. , 2016, , .		0
156	A novel PUF based on cell error rate distribution of STT-RAM. , 2016, , .		10
157	Leveraging Stochastic Memristor Devices in Neuromorphic Hardware Systems. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2016, 6, 235-246.	2.7	15
158	TEMP. , 2016, , .		8
159	A Memristor Crossbar Based Computing Engine Optimized for High Speed and Accuracy. , 2016, , .		33
160	Heterogeneous systems with reconfigurable neuromorphic computing accelerators. , 2016, , .		6
161	Design and Implementation of a 4Kb STT-MRAM with Innovative 200nm Nano-ring Shaped MTJ. , 2016, , .		2
162	Neural processor design enabled by memristor technology. , 2016, , .		4

#	Article	IF	Citations
163	A neuromorphic ASIC design using one-selector-one-memristor crossbar. , 2016, , .		13
164	ApesNet: a pixelâ€wise efficient segmentation network for embedded devices. IET Cyber-Physical Systems: Theory and Applications, 2016, 1, 78-85.	1.9	12
165	Guest editorial: Design and applications of neuromorphic computing system. IEEE Transactions on Multi-Scale Computing Systems, 2016, 2, 223-224.	2.5	2
166	Library-Based Placement and Routing in FPGAs with Support of Partial Reconfiguration. ACM Transactions on Design Automation of Electronic Systems, 2016, 21, 1-26.	1.9	3
167	Harmonica: A Framework of Heterogeneous Computing Systems With Memristor-Based Neuromorphic Computing Accelerators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 617-628.	3.5	49
168	Spintronic Memristor as Interface Between DNA and Solid State Devices. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2016, 6, 212-221.	2.7	3
169	A Neuromorphic Architecture for Context Aware Text Image Recognition. Journal of Signal Processing Systems, 2016, 84, 355-369.	1.4	10
170	Radiation-Induced Soft Error Analysis of STT-MRAM: A Device to Circuit Approach. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 380-393.	1.9	29
171	Small-world Hopfield neural networks with weight salience priority and memristor synapses for digit recognition. Neural Computing and Applications, 2016, 27, 837-844.	3.2	50
172	Compact lowâ€power instant store and restore D flipâ€flop using a selfâ€complementing spintronic device. Electronics Letters, 2016, 52, 1238-1240.	0.5	3
173	Objnandsim: object-based NAND flash device simulator. , 2016, , .		5
174	The Applications of NVM Technology in Hardware Security. , 2016, , .		6
175	A Holistic Tri-region MLC STT-RAM Design with Combined Performance, Energy, and Reliability Optimizations. , 2016, , .		3
176	Hierarchical Library Based Power Estimator for Versatile FPGAs. , 2015, , .		5
177	Hardware acceleration for neuromorphic computing: An evolving view. , 2015, , .		0
178	Hierarchical library based power estimator for versatile FPGAs. , 2015, , .		0
179	The evolutionary spintronic technologies and their usage in high performance computing. , 2015, , .		1
180	Giant Spin Hall Effect (GSHE) Logic Design for Low Power Application. , 2015, , .		20

#	Article	IF	Citations
181	Energy Efficient RRAM Spiking Neural Network for Real Time Classification. , 2015, , .		35
182	An overview on memristor crossabr based neuromorphic circuit and architecture. , 2015, , .		9
183	A Novel True Random Number Generator Design Leveraging Emerging Memristor Technology. , 2015, , .		34
184	Vortex. , 2015, , .		136
185	RENO. , 2015, , .		111
186	A High-Speed Robust NVM-TCAM Design Using Body Bias Feedback. , 2015, , .		9
187	Quantitative modeling of racetrack memory, a tradeoff among area, performance, and power. , 2015, , .		26
188	A spiking neuromorphic design with resistive crossbar. , 2015, , .		91
189	Cloning your mind. , 2015, , .		8
190	The applications of memristor devices in next-generation cortical processor designs. , 2015, , .		5
191	FlexLevel. , 2015, , .		18
192	VWS. , 2015, , .		5
193	FPGA Acceleration of Recurrent Neural Network Based Language Model. , 2015, , .		77
194	An efficient STT-RAM-based register file in GPU architectures. , 2015, , .		19
195	Spiking-based matrix computation by leveraging memristor crossbar array. , 2015, , .		1
196	A new self-reference sensing scheme for TLC MRAM. , 2015, , .		6
197	Spin-hall assisted STT-RAM design and discussion. , 2015, , .		4
198	Read Performance: The Newest Barrier in Scaled STT-RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1170-1174.	2.1	28

#	Article	IF	Citations
199	ICE: Inline calibration for memristor crossbar-based computing engine. , 2014, , .		5
200	A Novel Memristive Multilayer Feedforward Small-World Neural Network with Its Applications in PID Control. Scientific World Journal, The, 2014, 2014, 1-12.	0.8	13
201	Design exploration of racetrack lower-level caches. , 2014, , .		21
202	Reduction and IR-drop compensations techniques for reliable neuromorphic computing systems. , 2014, , .		91
203	Emerging memristor technology enabled next generation cortical processor. , 2014, , .		2
204	A heterogeneous computing system with memristor-based neuromorphic accelerators. , 2014, , .		0
205	Optimizing MLC-based STT-RAM caches by dynamic block size reconfiguration. , 2014, , .		20
206	Neuromorphic acceleration for context aware text image recognition. , 2014, , .		5
207	The stochastic modeling of TiO<inf>2</inf> memristor and its usage in neuromorphic system design. , 2014, , .		16
208	An adjustable memristor model and its application in small-world neural networks. , 2014, , .		6
209	A coherent hybrid SRAM and STT-RAM L1 cache architecture for shared memory multicores. , 2014, , .		24
210	STDP learning rule based on memristor with STDP property. , 2014, , .		5
211	STT-RAM Cache Hierarchy Design and Exploration with Emerging Magnetic Devices. , 2014, , 169-199.		1
212	Neuromorphic hardware acceleration enabled by emerging technologies (Invited paper). , 2014, , .		0
213	The Rhesus Rhadinovirus CD200 Homologue Affects Immune Responses and Viral Loads during In Vivo Infection. Journal of Virology, 2014, 88, 10635-10654.	1.5	15
214	Bio-inspired computing with resistive memories — models, architectures and applications. , 2014, , .		8
215	STT-RAM Cache Hierarchy With Multiretention MTJ Designs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1281-1293.	2.1	36
216	Memristor Crossbar-Based Neuromorphic Computing System: A Case Study. IEEE Transactions on Neural Networks and Learning Systems, 2014, 25, 1864-1878.	7.2	314

#	Article	IF	Citations
217	ICE: Inline calibration for memristor crossbar-based computing engine. , 2014, , .		11
218	A Weighted Sensing Scheme for ReRAM-Based Cross-Point Memory Array. , 2014, , .		26
219	Memristor Modeling -- Static, Statistical, and Stochastic Methodologies. , 2014, , .		1
220	Exploration of GPGPU Register File Architecture Using Domain-wall-shift-write based Racetrack Memory. , 2014, , .		32
221	A New Field-assisted Access Scheme of STT-RAM with Self-reference Capability. , 2014, , .		5
222	Spintronic Memristor as Interface Between DNA and Solid State Devices. , 2014, , 281-298.		0
223	A hardware security scheme for RRAM-based FPGA. , 2013, , .		3
224	BSB training scheme implementation on memristor-based circuit. , 2013, , .		14
225	A pseudo-weighted sensing scheme for memristor based cross-point memory. , 2013, , .		2
226	Bio-inspired ultra lower-power neuromorphic computing engine for embedded systems. , 2013, , .		0
227	A neuromorphic architecture for anomaly detection in autonomous large-area traffic monitoring. , 2013, , .		7
228	ADAMS: Asymmetric differential STT-RAM cell structure for reliable and high-performance applications. , 2013, , .		11
229	DA-RAID-5: A Disturb Aware Data Protection Technique for NAND Flash Storage Systems. , 2013, , .		9
230	Common-source-line array. ACM Transactions on Design Automation of Electronic Systems, 2013, 18, 1-18.	1.9	7
231	Digital-assisted noise-eliminating training for memristor crossbar-based analog neuromorphic computing engine. , 2013, , .		54
232	Cross-layer racetrack memory design for ultra high density and low power consumption. , 2013, , .		87
233	Impacting Factors and Improvement for Within-Shot IDSAT Uniformity. ECS Transactions, 2013, 52, 129-134.	0.3	0
234	Unleashing the potential of MLC STT-RAM caches. , 2013, , .		29

#	Article	IF	Citations
235	STT-RAM Designs Supporting Dual-Port Accesses. , 2013, , .		8
236	Memristor-based synapse design and a case study in reconfigurable systems. , 2013, , .		2
237	On-chip caches built on multilevel spin-transfer torque RAM cells and its optimizations. ACM Journal on Emerging Technologies in Computing Systems, 2013, 9, 1-22.	1.8	85
238	Coordinating prefetching and STT-RAM based last-level cache management for multicore systems. , 2013, , .		13
239	A practical low-power memristor-based analog neural branch predictor. , 2013, , .		6
240	Nonvolatile Memories as the Data Storage System for Implantable ECG Recorder. ACM Journal on Emerging Technologies in Computing Systems, 2012, 8, 1-16.	1.8	4
241	Hardware realization of BSB recall function using memristor crossbar arrays. , 2012, , .		155
242	Process variation aware data management for STT-RAM cache design. , 2012, , .		17
243	Magnetic tunnel junction design margin exploration for self-reference sensing scheme. Journal of Applied Physics, 2012, 111, 07C726.	1.1	2
244	Architecting a common-source-line array for bipolar non-volatile memory devices. , 2012, , .		11
245	A Look Up Table design with 3D bipolar RRAMs. , 2012, , .		4
246	VOLTAGE DRIVEN NONDESTRUCTIVE SELF-REFERENCE SENSING FOR STT-RAM YIELD ENHANCEMENT. Spin, 2012, 02, 1240008.	0.6	0
247	A novel peripheral circuit for RRAM-based LUT. , 2012, , .		15
248	Spintronic memristor based temperature sensor design with CMOS current reference. , 2012, , .		0
249	Fine-grained dynamic voltage scaling on OLED display. , 2012, , .		10
250	A 130 nm 1.2 V/3.3 V 16 Kb Spin-Transfer Torque Random Access Memory With Nondestructive Self-Reference Sensing Scheme. IEEE Journal of Solid-State Circuits, 2012, 47, 560-573.	3.5	64
251	Non-volatile 3D stacking RRAM-based FPGA. , 2012, , .		39
252	The 3-D Stacking Bipolar RRAM for High Density. IEEE Nanotechnology Magazine, 2012, 11, 948-956.	1.1	23

#	Article	IF	Citations
253	uBRAM-based run-time reconfigurable FPGA and corresponding reconfiguration methodology. , 2012, , .		4
254	Probabilistic design methodology to improve run-time stability and performance of STT-RAM caches. , 2012, , .		62
255	Voltage Driven Nondestructive Self-Reference Sensing Scheme of Spin-Transfer Torque Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2020-2030.	2.1	31
256	Analysis and Optimization of Thermal Effect on STT-RAM Based 3-D Stacked Cache Design. , 2012, , .		11
257	STT-RAM Cell Design Considering CMOS and MTJ Temperature Dependence. IEEE Transactions on Magnetics, 2012, 48, 3821-3824.	1.2	24
258	Statistical Memristor Model and Its Applications in Neuromorphic Computing. , 2012, , 107-131.		0
259	Statistical memristor modeling and case study in neuromorphic computing. , 2012, , .		19
260	A dual-mode architecture for fast-switching STT-RAM. , 2012, , .		23
261	Memristor crossbar based hardware realization of BSB recall function. , 2012, , .		48
262	Memristor-based synapse design and training scheme for neuromorphic computing architecture. , 2012, , .		9
263	Memristor in neuromorphic computing. , 2012, , .		1
264	Spintronic devices: From memory to memristor. , 2012, , .		1
265	3D-HIM: A 3D High-density Interleaved Memory for bipolar RRAM design. , 2011, , .		15
266	Fast statistical model of TiO<inf>2</inf> thin-film memristor and design implication. , 2011, , .		3
267	Universal statistical cure for predicting memory loss. , 2011, , .		2
268	Geometry variations analysis of TiO<inf>2</inf> thin-film and spintronic memristors. , 2011, , .		32
269	Emerging sensing techniques for emerging memories. , 2011, , .		1
270	Current Switching in MgO-Based Magnetic Tunneling Junctions. IEEE Transactions on Magnetics, 2011, 47, 156-160.	1.2	19

#	Article	IF	Citations
271	Processor caches built using multi-level spin-transfer torque RAM cells. , 2011, , .		43
272	Emerging non-volatile memories. , 2011, , .		165
273	Multi retention level STT-RAM cache designs with a dynamic refresh scheme. , 2011, , .		177
274	Stacking magnetic random access memory atop microprocessors: an architecture-level evaluation. IET Computers and Digital Techniques, 2011, 5, 213.	0.9	8
275	Nonpersistent Errors Optimization in Spin-MOS Logic and Storage Circuitry. IEEE Transactions on Magnetics, 2011, 47, 3860-3863.	1.2	5
276	STT-RAM Cell Optimization Considering MTJ and CMOS Variations. IEEE Transactions on Magnetics, 2011, 47, 2962-2965.	1.2	44
277	Performance, Power, and Reliability Tradeoffs of STT-RAM Cell Subject to Architecture-Level Requirement. IEEE Transactions on Magnetics, 2011, 47, 2356-2359.	1.2	31
278	3D-ICML: A 3D bipolar ReRAM design with interleaved complementary memory layers. , 2011, , .		1
279	Spintronic Memristor: Compact Model and Statistical Analysis. Journal of Low Power Electronics, 2011, 7, 234-244.	0.6	2
280	Emerging non-volatile memory technologies: From materials, to device, circuit, and architecture. , 2010, , .		2
281	A nondestructive self-reference scheme for Spin-Transfer Torque Random Access Memory (STT-RAM). , 2010, , .		7
282	Variation tolerant sensing scheme of Spin-Transfer Torque Memory for yield improvement. , 2010, , .		12
283	Spin Transfer Torque Memory With Thermal Assist Mechanism: A Case Study. IEEE Transactions on Magnetics, 2010, 46, 860-865.	1.2	12
284	Access scheme of Multi-Level Cell Spin-Transfer Torque Random Access Memory and its optimization. , 2010, , .		55
285	Compact model of memristors and its application in computing systems. , 2010, , .		3
286	Variable-Latency Adder (VL-Adder) Designs for Low Power and NBTI Tolerance. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1621-1624.	2.1	30
287	The application of spintronic devices in magnetic bio-sensing. , 2010, , .		6
288	Design Margin Exploration of Spin-Transfer Torque RAM (STT-RAM) in Scaled Technologies. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1724-1734.	2.1	72

#	Article	IF	Citations
289	PCMO Device With High Switching Stability. IEEE Electron Device Letters, 2010, 31, 866-868.	2.2	11
290	Applications of TMR devices in solid state circuits and systems. , 2010, , .		0
291	Scalability of PCMO-based resistive switch device in DSM technologies. , 2010, , .		0
292	Spintronic Memristor Temperature Sensor. IEEE Electron Device Letters, 2010, 31, 20-22.	2.2	60
293	Patents Relevant to Cross-Point Memory Array. Recent Patents on Electrical Engineering, 2010, 3, 114-124.	0.4	0
294	Tolerating process variations in large, set-associative caches. Transactions on Architecture and Code Optimization, 2009, 6, 1-34.	1.6	20
295	Spintronic Memristor Through Spin-Torque-Induced Magnetization Motion. IEEE Electron Device Letters, 2009, 30, 294-297.	2.2	314
296	An overview of non-volatile memory technology and the implication for tools and architectures. , 2009, , .		5
297	Gated Decap: Gate Leakage Control of On-Chip Decoupling Capacitors in Scaled Technologies. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1749-1752.	2.1	5
298	Thermal-Assisted Spin Transfer Torque Memory (STT-RAM) Cell Design Exploration. , 2009, , .		4
299	Spin Torque Random Access Memory Down to 22 nm Technology. IEEE Transactions on Magnetics, 2008, 44, 2479-2482.	1.2	46
300	VOSCH: Voltage scaled cache hierarchies. , 2007, , .		2
301	Combined circuit and architectural level variable supply-voltage scaling for low power. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 564-576.	2.1	16
302	Cascaded carry-select adder (C/sup 2/SA): a new structure for low-power CSA design. , 2005, , .		5
303	DCG: deterministic clock-gating for low-power microprocessor design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2004, 12, 245-254.	2.1	45
304	A single-V/sub t/ low-leakage gated-ground cache for deep submicron. IEEE Journal of Solid-State Circuits, 2003, 38, 319-328.	3.5	106
305	DRG-cache: a data retention gated-ground cache for low power. , 2002, , .		43
306	A high performance IDDQ testable cache for scaled CMOS technologies. , 0, , .		12

#	Article	IF	Citations
307	Deterministic clock gating for microprocessor power reduction. , 0, , .		42
308	VSV: L2-miss-driven variable supply-voltage scaling for low power. , 0, , .		13
309	Gated decap: gate leakage control of on-chip decoupling capacitors in scaled technologies. , 0, , .		6