Soonyoung Cha

List of Publications by Year
in descending order

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9 papers	54 citations	1937685 4 h-index	1872680 6 g-index
9 all docs	9 docs citations	9 times ranked	37 citing authors

#	Article	IF	Citations
1	Negative Bias Temperature Instability and Gate Oxide Breakdown Modeling in Circuits With Die-to-Die Calibration Through Power Supply and Ground Signal Measurements. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2271-2284.	3.1	6
2	Adaptive supply voltage and duty cycle controller for yield-power optimization of ICs. , 2017, , .		0
3	Design for reliability: A duty-cycle management system for timing violations. , 2016, , .		1
4	Built-in self-test for bias temperature instability, hot-carrier injection, and gate oxide breakdown in embedded DRAMs. Microelectronics Reliability, 2015, 55, 2113-2118.	1.7	5
5	Processor-level reliability simulator for time-dependent gate dielectric breakdown. Microprocessors and Microsystems, 2015, 39, 950-960.	2.8	8
6	MBIST and statistical hypothesis test for time dependent dielectric breakdowns due to GOBD vs. BTDDB in an SRAM array. , 2015, , .		2
7	System-level variation-aware aging simulator using a unified novel gate-delay model for bias temperature instability, hot carrier injection, and gate oxide breakdown. Microelectronics Reliability, 2015, 55, 1334-1340.	1.7	25
8	The die-to-die calibrated combined model of negative bias temperature instability and gate oxide breakdown from device to system. Microelectronics Reliability, 2015, 55, 1404-1411.	1.7	4
9	AVERT: An elaborate model for simulating variable retention time in DRAMs. Microelectronics Reliability, 2015, 55, 1313-1319.	1.7	3