Rajesh Saha

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/8669188/publications.pdf

Version: 2024-02-01

42	485	687363 13	752698 20
papers	citations	h-index	g-index

43	43	43	189
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Temperature effect on RF/analog and linearity parameters in DMG FinFET. Applied Physics A: Materials Science and Processing, 2018, 124, 1.	2.3	62
2	Sensitivity Analysis on Dielectric Modulated Ge-Source DMDG TFET Based Label-Free Biosensor. IEEE Nanotechnology Magazine, 2021, 20, 552-560.	2.0	32
3	Simulation study on ferroelectric layer thickness dependence RF/Analog and linearity parameters in ferroelectric tunnel junction TFET. Microelectronics Journal, 2021, 113, 105081.	2.0	30
4	Statistical Dependence of Gate Metal Work Function on Various Electrical Parameters for an n-Channel Si Step-FinFET. IEEE Transactions on Electron Devices, 2017, 64, 969-976.	3.0	29
5	Analysis on effect of lateral straggle on analog, high frequency and <scp>DC</scp> parameters in Geâ€source <scp>DMDG TFET</scp>. International Journal of RF and Microwave Computer-Aided Engineering, 2021, 31, e22579.	1.2	25
6	3D analytical modeling of surface potential, threshold voltage, and subthreshold swing in dual-material-gate (DMG) SOI FinFETs. Journal of Computational Electronics, 2018, 17, 153-162.	2.5	24
7	Deep insight into DC, RF/analog, and digital inverter performance due to variation in straggle parameter for gate modulated TFET. Materials Science in Semiconductor Processing, 2019, 91, 102-107.	4.0	23
8	Dependence of RF/Analog and Linearity Figure of Merits on Temperature in Ferroelectric FinFET: A Simulation Study. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 2020, 67, 2433-2439.	3.0	23
9	Si and Ge step-FinFETs: Work function variability, optimization and electrical parameters. Superlattices and Microstructures, 2017, 107, 5-16.	3.1	19
10	Comparative Analysis Among Single Material Gate, Double Material Gate, and Triple Material Gate FinFETs: RF/Analog and Digital Inverter Performance. Journal of Nanoelectronics and Optoelectronics, 2018, 13, 803-811.	0.5	19
11	Analytical modelling for surface potential of dual material gate overlapped-on-drain TFET(DM-DMG-TFET) for label-free biosensing application. AEU - International Journal of Electronics and Communications, 2022, 151, 154225.	2.9	18
12	Methods to Reduce Ambipolar Current of Various TFET Structures: a Review. Silicon, 2022, 14, 6507-6515.	3.3	16
13	Impact of WFV on electrical parameters due to high-k/metal gate in SiGe channel tunnel FET. Microelectronic Engineering, 2019, 214, 1-4.	2.4	14
14	Effects of temperature on electrical parameters in GaAs SOI FinFET and application as digital inverter. , 2017, , .		13
15	Performance evaluation of hetero-stacked TFET for variation in lateral straggle and its application as digital inverter. Applied Physics A: Materials Science and Processing, 2018, 124, 1.	2.3	13
16	Analysis on DC and RF/Analog Performance in Multifin-FinFET for Wide Variation in Work Function of Metal Gate. Silicon, 2021, 13, 73-77.	3.3	13
17	Impact of lateral straggle on linearity performance in gate-modulated (GM) TFET. Applied Physics A: Materials Science and Processing, 2020, 126, 1.	2.3	12
18	Effect of gate dielectric on electrical parameters due to metal gate WFV in nâ€channel Si step FinFET. Micro and Nano Letters, 2018, 13, 1007-1010.	1.3	11

#	Article	IF	Citations
19	Effect of Ge Mole Fraction on Electrical Parameters of Si1â^'xGex Source Step-FinFET and its Application as an Inverter. Silicon, 2019, 11, 209-219.	3.3	9
20	Study on impact of ferroelectric layer thickness on <scp>RF</scp> /analog and linearity parameters in <scp>ferroelectricâ€FinFET</scp>. International Journal of RF and Microwave Computer-Aided Engineering, 2021, 31, e22704.	1.2	9
21	Analytical threshold voltage and subthreshold swing model for TMG FinFET. International Journal of Electronics, 2019, 106, 553-566.	1.4	8
22	Effect of Drain Engineering on DC and RF Characteristics in Ge-source SD-ZHP-TFET. , 2021, , .		8
23	Effect of Temperature on Performance of 5-nm Node Silicon Nanosheet Transistors for Analog Applications. Silicon, 2022, 14, 10581-10589.	3.3	8
24	Air-spacers as analog-performance booster for 5 nm-node N-channel nanosheet transistor. Semiconductor Science and Technology, 2021, 36, 095037.	2.0	7
25	<scp>DC</scp> and <scp>RF</scp>/analog parameters in Geâ€source split drain<scp>â€ZHPâ€TFET</scp>: Drain and pocket engineering technique. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2022, 35, e2967.	1.9	7
26	Quantum modeling of threshold voltage in Ge dual material gate (DMG) FinFET. Solid-State Electronics, 2019, 159, 129-134.	1.4	4
27	Linearity Parameters Evaluation due to Lateral Straggle in Ge-Source DMDG-TFET. Silicon, 2022, 14, 567-571.	3.3	4
28	A 3D statistical simulation study of titanium metal gate WFV on electrical parameters in n-channel Ge step-FinFET. Applied Physics A: Materials Science and Processing, 2018, 124, 1.	2.3	3
29	Deep insights into electrical parameters due to metal gate WFV for different gate oxide thickness in Si step FinFET. Micro and Nano Letters, 2019, 14, 384-388.	1.3	3
30	Impact of Mole Fractions due to Work Function Variability (WFV) of Metal Gate on Electrical Parameters in Strained SOI-FinFET. Silicon, 2020, 12, 577-583.	3.3	3
31	Impact of work function on analog/RF and linearity parameters in step-FinFET. Indian Journal of Physics, 2021, 95, 2387-2392.	1.8	3
32	Dependence of metal gate work function variation for various ferroelectric thickness on electrical parameters in NC-FinFET. Ferroelectrics, 2021, 570, 67-76.	0.6	3
33	Comprehensive investigation of radiofrequency/analog parameters in a ferroelectric tunnel field-effect transistor. Semiconductor Science and Technology, 2022, 37, 035008.	2.0	3
34	Performance Evaluation of Epitaxial Layer Based Gate Modulated TFET (GM-TFET). Silicon, 2022, 14, 5713-5718.	3.3	2
35	Study of effect of oxide thickness variation on electrical parameters and high frequency characteristics induced by work-function variation for delta-doped germanium-source vertical TFET. Semiconductor Science and Technology, 2020, 35, 105009.	2.0	2
36	Quantum Analytical Modeling of Inversion Charge and Threshold Voltage in Modified Bi-Level FinFET (BL-FinFET). ECS Journal of Solid State Science and Technology, 2018, 7, Q8-Q15.	1.8	1

#	Article	IF	Citations
37	TCAD simulation study on reliability issue of heterojunction heterodielectric FinFET: Effect of interface trap charge, BOX height and temperature. Pramana - Journal of Physics, 2021, 95, 1.	1.8	1
38	Comparison of RF/Analog and Linearity Performance of Various TFETs Using Source Engineering. Silicon, 0, , .	3.3	1
39	Dependence of Lateral Straggle Parameter on DC, RF/Analog, and Linearity Performance in SOI FinFET. IETE Journal of Research, 0, , 1-9.	2.6	0
40	Influence of dielectric material near tunnel junction on analog/ RF and linearity figure of merits in hetero dielectric (HG) TFET : A detailed study. International Journal of RF and Microwave Computer-Aided Engineering, 0, , e22915.	1.2	0
41	Hot carrier effect in Ferro-FinFET for variation in temperature, work function, and FE layer thickness. Integrated Ferroelectrics, 2021, 221, 168-179.	0.7	0
42	RF/Analog Parameters in DMG-FinFET for Channel Material Beyond Si. , 2022, , .		0