Ryszard Szplet

List of Publications by Year in descending order

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29	622	840776 11	888059 17
papers	citations	h-index	g-index

29	29	29	332
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Bubble-Proof Algorithm for Wave Union TDCs. Electronics (Switzerland), 2022, 11, 30.	3.1	6
2	A brief review of wave union TDCs. , 2021, , .		5
3	Two-Stage Clock-Free Time-to-Digital Converter Based on Vernier and Tapped Delay Lines in FPGA Device. Electronics (Switzerland), 2021, 10, 2190.	3.1	7
4	Efficient Implementation of Multiple Time Coding Lines-Based TDC in an FPGA Device. IEEE Transactions on Instrumentation and Measurement, 2020, 69, 7353-7364.	4.7	31
5	Multisampling wave union time-to-digital converter. , 2020, , .		8
6	Precise Time Digitizer Based on Counting Method and Multiphase In-Period Interpolation. , 2019, , .		1
7	Measurement Uncertainty of Precise Interpolating Time Counters. IEEE Transactions on Instrumentation and Measurement, 2019, 68, 4348-4356.	4.7	20
8	5 ps Jitter Programmable Time Interval/Frequency Generator. Metrology and Measurement Systems, 2017, 24, 57-68.	1.4	11
9	Picosecond-precision multichannel autonomous time and frequency counter. Review of Scientific Instruments, 2017, 88, 125101.	1.3	13
10	High-Precision Time Digitizer Based on Multiedge Coding in Independent Coding Lines. IEEE Transactions on Instrumentation and Measurement, 2016, 65, 1884-1894.	4.7	17
11	An Eight-Channel 4.5-ps Precision Timestamps-Based Time Interval Counter in FPGA Chip. IEEE Transactions on Instrumentation and Measurement, 2016, 65, 2088-2100.	4.7	36
12	Time interval measurement module implemented in SoC FPGA device. International Journal of Electronics and Telecommunications, 2016, 62, 237-246.	0.6	2
13	Measurement subsystem for evaluation of local atomic clocks quality. Przeglad Elektrotechniczny, 2016, 1, 41-44.	0.2	0
14	Precise three-channel integrated time counter. , 2015, , .		1
15	A comparison of methods for time-to-digital conversion based on independent coding lines and multi-edge coding. , 2015, , .		1
16	A combination of multi-edge coding and independent coding lines for time-to-digital conversion. , 2014, , .		1
17	Modular time interval counter. , 2014, , .		3
18	Subpicosecond-resolution time-to-digital converter with multi-edge coding in independent coding lines. , 2014, , .		10

#	Article	IF	Citations
19	Time-to-Digital Converters. Signals and Communication Technology, 2014, , 211-246.	0.5	20
20	Interpolating time counter with multi-edge coding. , 2013, , .		5
21	11-ps resolution time interval counter in CMOS ASIC. , 2012, , .		2
22	An FPGA-Integrated Time-to-Digital Converter Based on Two-Stage Pulse Shrinking. IEEE Transactions on Instrumentation and Measurement, 2010, 59, 1663-1670.	4.7	62
23	A two-stage time-to-digital converter based on cyclic pulse shrinking. , 2009, , .		1
24	Interpolating time counter with 100 ps resolution on a single FPGA device. IEEE Transactions on Instrumentation and Measurement, 2000, 49, 879-883.	4.7	101
25	Delay-locked loop technique for temperature stabilisation of internal delays of CMOS FPGA devices. Electronics Letters, 2000, 36, 1184.	1.0	8
26	Single-chip low-cost time counter for distance measurements with 3 cm resolution. Journal of Optics, 1998, 29, 199-205.	0.3	4
27	Field-programmable-gate-array-based time-to-digital converter with 200-ps resolution. IEEE Transactions on Instrumentation and Measurement, 1997, 46, 51-55.	4.7	131
28	Nonlinearity correction of the integrated time-to-digital converter with direct coding. IEEE Transactions on Instrumentation and Measurement, 1997, 46, 449-453.	4.7	53
29	Single-chip interpolating time counter with 200-ps resolution and 43-s range. IEEE Transactions on Instrumentation and Measurement, 1997, 46, 851-856.	4.7	62