Garrett S Rose

List of Publications by Year
in descending order

143 papers	2,992 citations	331259 21 h-index	264894 42 g-index
146 all docs	146 docs citations	146 times ranked	1951 citing authors

#	Article	IF	Citations
1	Benchmark Comparisons of Spike-based Reconfigurable Neuroprocessor Architectures for Control Applications. , 2022, , .		2
2	Physically Unclonable and Reconfigurable Computing System (PURCS) for Hardware Security Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 405-418.	1.9	22
3	Design of a Robust Memristive Spiking Neuromorphic System with Unsupervised Learning in Hardware. ACM Journal on Emerging Technologies in Computing Systems, 2021, 17, 1-26.	1.8	7
4	A Multi-Context Neural Core Design for Reconfigurable Neuromorphic Arrays. , 2021, , .		3
5	Scaling Constraints for Memristor-based Programmable Interconnect in Reconfigurable Computing Arrays. , 2021, , .		1
6	Capacitor-Less Memristive Integrate-and-Fire Neuron with Stochastic Behavior. , 2021, , .		0
7	Short-Term Facilitation-Then-Depression Enables Adaptive Processing of Sensory Inputs by Ion Channels in Biomolecular Synapses. ACS Applied Electronic Materials, 2021, 3, 4448-4458.	2.0	5
8	A system designÂperspective on neuromorphic computer processors. Neuromorphic Computing and Engineering, 2021, 1, 022001.	2.8	8
9	TCAD Modeling of Resistive-Switching of HfO2 Memristors: Efficient Device-Circuit Co-Design for Neuromorphic Systems. Frontiers in Nanotechnology, 2021, 3, .	2.4	13
10	A Chaos-Based Complex Micro-instruction Set for Mitigating Instruction Reverse Engineering. Journal of Hardware and Systems Security, 2020, 4, 69-85.	0.8	11
11	Scaled-up Neuromorphic Array Communications Controller (SNACC) for Large-scale Neural Networks. , 2020, , .		0
12	Automated Design of Neuromorphic Networks for Scientific Applications at the Edge. , 2020, , .		1
13	Circuit Techniques for Efficient Implementation of Memristor Based Reservoir Computing. , 2020, , .		2
14	Modeling Emerging Semiconductor Devices for Circuit Simulation. , 2020, , .		0
15	GRANT: Ground-Roaming Autonomous Neuromorphic Targeter. , 2020, , .		3
16	Single Photon Avalanche Diode based Vision Sensor with On-Chip Memristive Spiking Neuromorphic Processing. , 2020, , .		3
17	Device-aware Circuit Design for Robust Memristive Neuromorphic Systems with STDP-based Learning. ACM Journal on Emerging Technologies in Computing Systems, 2020, 16, 1-25.	1.8	4
18	Towards Synaptic Behavior of Nanoscale ReRAM Devices for Neuromorphic Computing Applications. ACM Journal on Emerging Technologies in Computing Systems, 2020, 16, 1-18.	1.8	13

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19	Design of an Enhanced Reconfigurable Chaotic Oscillator using G⁴FET-NDR Based Discrete Map. , 2020, , .		9
20	Robust Implementation of Memristive Reservoir Computing with Crossbar Based Readout Layer. , 2020, , .		3
21	Dynamical nonlinear memory capacitance in biomimetic membranes. Nature Communications, 2019, 10, 3239.	5.8	51
22	Design of a Lightweight Reconfigurable PRNG Using Three Transistor Chaotic Map. , 2019, , .		5
23	A Review of Spiking Neuromorphic Hardware Communication Systems. IEEE Access, 2019, 7, 135606-135620.	2.6	57
24	On the Theoretical Analysis of Memristor based True Random Number Generator. , 2019, , .		11
25	A Multi-Driver Write Scheme for Reliable and Energy Efficient 1S1R ReRAM Crossbar Arrays. , 2019, , .		1
26	Memristor Crossbar PUF based Lightweight Hardware Security for IoT. , 2019, , .		4
27	Assembly and Characterization of Biomolecular Memristors Consisting of Ion Channel-doped Lipid Membranes. Journal of Visualized Experiments, 2019, , .	0.2	6
28	Multivariate Cubic Spline: A Versatile DC Modeling Technique Suitable for Different Deep Submicron Transistors. , 2019, , .		1
29	Evaluation, optimization, and Enhancement of Chaos Based Reconfigurable Logic Design. , 2019, , .		3
30	Stochasticity in Neuromorphic Computing: Evaluating Randomness for Improved Performance. , 2019, , .		0
31	A Scan Register Based Access Scheme for Multilevel Non-Volatile Memristor Memory. , 2019, , .		0
32	Shortest Path and Neighborhood Subgraph Extraction on a Spiking Memristive Neuromorphic Implementation. , 2019, , .		20
33	Design Considerations for Insulator Metal Transition based Artificial Neurons. , 2019, , .		0
34	A Secure Integrity Checking System for Nanoelectronic Resistive RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 416-429.	2.1	3
35	SPICE Modeling of Insulator Metal Transition: Model of the Critical Temperature. IEEE Journal of the Electron Devices Society, 2019, 7, 18-25.	1.2	10
36	Macromodel of G4FET Enabling Fast and Reliable SPICE Simulation for Innovative Circuit Applications. Selected Topics in Electornics and Systems, 2019, , 17-36.	0.2	0

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37	Analysis and Modeling of Electroforming in Transition Metal Oxide-Based Memristors and Its Impact on Crossbar Array Density. IEEE Electron Device Letters, 2018, 39, 19-22.	2.2	11
38	Memristive Mixed-Signal Neuromorphic Systems: Energy-Efficient Learning at the Circuit-Level. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 125-136.	2.7	38
39	High-Level Simulation for Spiking Neuromorphic Computing Systems. , 2018, , .		1
40	Memristive Ion Channel-Doped Biomembranes as Synaptic Mimics. ACS Nano, 2018, 12, 4702-4711.	7.3	107
41	Design Considerations for Memristive Crossbar Physical Unclonable Functions. ACM Journal on Emerging Technologies in Computing Systems, 2018, 14, 1-23.	1.8	12
42	Macromodel of G⁴FET Enabling Fast and Reliable SPICE Simulation for Innovative Circuit Applications. International Journal of High Speed Electronics and Systems, 2018, 27, 1840015.	0.3	3
43	A MOS-JFET Macromodel of SOI Four-Gate Transistors (G⁴FET) to Aid Innovative Circuit Design. , 2018, , .		2
44	A Soft-Matter Biomolecular Memristor Synapse for Neuromorphic Systems. , 2018, , .		6
45	A Practical Sense Amplifier Design for Memristive Crossbar Circuits (PUF). , 2018, , .		5
46	Response of a Memristive Biomembrane and Demonstration of Potential Use in Online Learning. , 2018, , .		4
47	Design of a Reconfigurable Chaos Gate with Enhanced Functionality Space in 65nm CMOS. , 2018, , .		11
48	A Twin Memristor Synapse for Spike Timing Dependent Learning in Neuromorphic Systems. , 2018, , .		9
49	Biomimetic, Soft-Material Synapse for Neuromorphic Computing: from Device to Network. , 2018, , .		14
50	Synaptic Behavior of Nanoscale ReRAM Devices for the Implementation in a Dynamic Neural Network Array. , 2018, , .		0
51	Neuromorphic Array Communications Controller to Support Large-Scale Neural Networks. , 2018, , .		1
52	The TENNLab Exploratory Neuromorphic Computing Framework. IEEE Letters of the Computer Society, 2018, 1, 17-20.	1.1	41
53	Practical realisation of a return map immune Lorenzâ€based chaotic stream cipher in circuitry. IET Computers and Digital Techniques, 2018, 12, 297-305.	0.9	9
54	Nanoelectronic Security Designs for Resource-Constrained Internet of Things Devices: Finding Security Solutions with Nanoelectronic Hardwares. IEEE Consumer Electronics Magazine, 2018, 7, 15-22.	2.3	5

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55	Guest Editorial: Hardwareâ€Assisted Techniques for Security and Protection of ConsumerElectronics. IET Computers and Digital Techniques, 2018, 12, 249-250.	0.9	0
56	A Novel Scan-In Scheme for CMOS/ReRAM Programmable Logic Circuits. , 2018, , .		1
57	A bi-memristor synapse with spike-timing-dependent plasticity for on-chip learning in memristive neuromorphic systems. , 2018, , .		7
58	Chaos computing for mitigating side channel attack. , 2018, , .		20
59	DANNA 2. , 2018, , .		20
60	A Comparison of Neuromorphic Classification Tasks. , 2018, , .		10
61	A Study of Complex Deep Learning Networks on High-Performance, Neuromorphic, and Quantum Computers. ACM Journal on Emerging Technologies in Computing Systems, 2018, 14, 1-21.	1.8	39
62	Adiabatic Quantum Computation Applied to Deep Learning Networks. Entropy, 2018, 20, 380.	1.1	19
63	A Mixed-Mode Neuron with On-chip Tunability for Generic Use in Memristive Neuromorphic Systems. , 2018, , .		1
64	Energy and Area Efficiency in Neuromorphic Computing for Resource Constrained Devices. , 2018, , .		10
65	Robustness Analysis of a Memristive Crossbar PUF Against Modeling Attacks. IEEE Nanotechnology Magazine, 2017, 16, 396-405.	1.1	56
66	Circuit Techniques for Online Learning of Memristive Synapses in CMOS-Memristor Neuromorphic Systems. , 2017, , .		10
67	A programming framework for neuromorphic systems with emerging technologies. , 2017, , .		4
68	Exploiting Memristive Crossbar Memories as Dual-Use Security Primitives in IoT Devices. , 2017, , .		1
69	Simulating and Estimating the Behavior of a Neuromorphic Co-Processor. , 2017, , .		3
70	Design techniques for in-field memristor forming circuits. , 2017, , .		6
71	A mixed-signal approach to memristive neuromorphic system design. , 2017, , .		5
72	A practical hafnium-oxide memristor model suitable for circuit design and simulation. , 2017, , .		42

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73	A Unified Hardware/Software Co-Design Framework for Neuromorphic Computing Devices and Applications. , 2017, , .		13
74	NeoN: Neuromorphic control for autonomous robotic navigation. , 2017, , .		23
75	Evaluating online-learning in memristive neuromorphic circuits. , 2017, , .		2
76	Neuromorphic computing for temporal scientific data classification. , 2017, , .		7
77	A synchronized axon hillock neuron for memristive neuromorphic systems. , 2017, , .		3
78	A Chaotic Logic-Based Physical Unclonable Computing System. , 2017, , 327-342.		0
79	Extensions and enhancements for the DANNA neuromorphic architecture. , 2016, , .		1
80	Sneak path enabled authentication for memristive crossbar memories. , 2016, , .		6
81	Techniques for Improved Reliability in Memristive Crossbar PUF Circuits. , 2016, , .		21
82	A Designer's Rationale for Nanoelectronic Hardware Security Primitives. , 2016, , .		4
83	An Application Development Platform for neuromorphic computing. , 2016, , .		6
84	Security Meets Nanoelectronics for Internet of Things Applications. , 2016, , .		11
85	A two-dimensional chaotic logic gate for improved computer security. , 2015, , .		8
86	Fault Analysis-Based Logic Encryption. IEEE Transactions on Computers, 2015, 64, 410-424.	2.4	352
87	Nano Meets Security: Exploring Nanoelectronic Devices for Security Applications. Proceedings of the IEEE, 2015, 103, 829-849.	16.4	102
88	Performance analysis of a memristive crossbar PUF design. , 2015, , .		33
89	Power Profile Obfuscation Using Nanoscale Memristive Devices to Counter DPA Attacks. IEEE Nanotechnology Magazine, 2015, 14, 26-35.	1.1	14
90	Improving Tolerance to Variations in Memristor-Based Applications Using Parallel Memristors. IEEE Transactions on Computers, 2015, 64, 733-746.	2.4	34

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91	On designing circuit primitives for cortical processors with memristive hardware. , 2014, , .		0
92	Design of Neuromorphic Architectures with Memristors. Advances in Information Security, 2014, , 93-103.	0.9	2
93	Memristor Crossbar-Based Neuromorphic Computing System: A Case Study. IEEE Transactions on Neural Networks and Learning Systems, 2014, 25, 1864-1878.	7.2	314
94	A Chaos-Based Arithmetic Logic Unit and Implications for Obfuscation. , 2014, , .		16
95	Nanoelectronics and Hardware Security. Advances in Information Security, 2014, , 105-123.	0.9	4
96	Memristor-Based Neural Logic Blocks for Nonlinearly Separable Functions. IEEE Transactions on Computers, 2013, 62, 1597-1606.	2.4	35
97	Hardware security strategies exploiting nanoelectronic circuits. , 2013, , .		28
98	BSB training scheme implementation on memristor-based circuit. , 2013, , .		14
99	Foundations of memristor based PUF architectures. , 2013, , .		47
100	A write-time based memristive PUF for hardware security applications. , 2013, , .		62
101	Hardware realization of BSB recall function using memristor crossbar arrays. , 2012, , .		155
102	RRAM-based adaptive neural logic block for implementing non-linearly separable functions in a single layer. , 2012, , .		7
103	Leveraging Memristive Systems in the Construction of Digital Logic Circuits. Proceedings of the IEEE, 2012, 100, 2033-2049.	16.4	103
104	Nano-PPUF: A Memristor-Based Security Primitive. , 2012, , .		78
105	Stochastic Gradient Descent Inspired Training Technique for a CMOS/Nano Memristive Trainable Threshold Gate Array. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1051-1060.	3.5	26
106	Design Considerations for Multilevel CMOS/Nano Memristive Memory. ACM Journal on Emerging Technologies in Computing Systems, 2012, 8, 1-22.	1.8	50
107	Memristor crossbar based hardware realization of BSB recall function. , 2012, , .		48
108	An Energy-Efficient Memristive Threshold Logic Circuit. IEEE Transactions on Computers, 2012, 61, 474-487.	2.4	79

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109	An Approach to Tolerate Process Related Variations in Memristor-Based Applications. , 2011, , .		31
110	Exploration of CMOS-Memristive Neuromorphic Circuits. , 2011, , .		0
111	Parallel memristors: Improving variation tolerance in memristive digital circuits. , 2011, , .		4
112	A low-power memristive neuromorphic circuit utilizing a global/local training mechanism. , 2011, , .		16
113	A read-monitored write circuit for 1T1M multi-level memristor memories. , 2011, , .		44
114	3D NOC for many-core processors. Microelectronics Journal, 2011, 42, 1380-1390.	1.1	14
115	A hierarchical 3-D floorplanning algorithm for many-core CMP networks. , 2011, , .		2
116	Exploiting memristance for low-energy neuromorphic computing hardware. , 2011, , .		8
117	Highly-scalable 3D CLOS NOC for many-core CMPs. , 2010, , .		8
118	Overview: Memristive devices, circuits and systems. , 2010, , .		8
119	Design considerations for variation tolerant multilevel CMOS/Nano memristor memory. , 2010, , .		70
120	Memristor based programmable threshold logic array. , 2010, , .		42
121	A Hybrid CMOS-Nano FPGA Based on Majority Logic: From Devices to Architecture. , 2010, , 139-161.		3
122	Improved performance and yield with chip master planning design methodology. , 2009, , .		0
123	Non-overlapping transition encoding for global on-chip interconnect. , 2009, , .		1
124	Inversion schemes for sublithographic programmable logic arrays. IET Computers and Digital Techniques, 2009, 3, 625.	0.9	45
125	A process variation tolerant self-compensating FinFET based sense amplifier design. , 2009, , .		1
126	The effects of logic partitioning in a majority logic based CMOS-NANO FPGA. , 2009, , .		0

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127	A dual-MOSFET equivalent resistor thermal sensor. , 2009, , .		0
128	Hybrid CMOS/Molecular Integrated Circuits. Springer Series in Materials Science, 2009, , 257-280.	0.4	1
129	A hybrid cmos/nano fpga architecture built fromprogrammable majority logic arrays. , 2008, , .		5
130	The Effect of Device Parameter Variations on Programmable Majority Logic Arrays. , 2008, , .		1
131	Testing molecular devices in CMOS/nano integrated circuits. , 2007, , .		0
132	On-chip characterization of molecular electronic devices using CMOS. , 2007, , .		3
133	Designing CMOS/molecular memories while considering device parameter variations. ACM Journal on Emerging Technologies in Computing Systems, 2007, 3, 3.	1.8	26
134	A Programmable Majority Logic Array Using Molecular Scale Electronics. IEEE Transactions on Circuits and Systems I: Regular Papers, 2007, 54, 2380-2390.	3.5	26
135	Designs for Ultra-Tiny, Special-Purpose Nanoelectronic Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2007, 54, 2528-2540.	3.5	30
136	Reducing stray currents in molecular memory through data encoding. , 2007, , .		2
137	Architectures and Simulations for Nanoprocessor Systems Integrated on the Molecular Scale. , 2006, , 479-512.		9
138	Design approaches for hybrid CMOS/molecular memory based on experimental device data. , 2006, , .		19
139	Hybrid CMOS/Molecular Electronic Circuits. , 2006, , .		6
140	A programmable majority logic array using molecular scale electronics. , 2006, , .		0
141	Large-signal two-terminal device model for nanoelectronic circuit analysis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2004, 12, 1201-1208.	2.1	18
142	A universal device model for nanoelectronic circuit simulation. , 0, , .		15
143	Memory arrays based on molecular RTD devices. , 0, , .		11