# Ramiro Taco

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/8639278/publications.pdf

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|---|---|---|---|
| 24 papers | 168 citations | 1478505 6 h-index | 1372567 10 g-index |
| 24 all docs | 24 docs citations | 24 times ranked | 102 citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | A Method for Mitigation of Droop Timing Errors Including a 500 MHz Droop Detector and Dual Mode Logic. IEEE Journal of Solid-State Circuits, 2022, 57, 596-608. | 5.4 | 3 |
| 2 | From 32 nm to TFET Technology: New Perspectives for Ultra-Scaled RF-DC Multiplier Circuits. Electronics (Switzerland), 2022, 11, 525. | 3.1 | 1 |
| 3 | Performance Benchmarking of TFET and FinFET Digital Circuits from a Synthesis-Based Perspective. Electronics (Switzerland), 2022, 11, 632. | 3.1 | 2 |
| 4 | Voltage and Technology Scaling of DMTJ-based STT-MRAMs for Energy-Efficient Embedded Memories. , 2022, , . | | 1 |
| 5 | DMTJ-Based Non-Volatile Ternary Content Addressable Memory for Energy-Efficient High-Performance Systems. , 2022, , . | | 0 |
| 6 | Energy-Efficient FinFET-Versus TFET-Based STT-MRAM Bitcells. , 2022, , . | | 1 |
| 7 | High-Speed and Low-Energy Dual-Mode Logic based Single-Clack-Cycle Binary Comparator. , 2021, , . | | 1 |
| 8 | Energy Efficient Self-Adaptive Dual Mode Logic Address Decoder. Electronics (Switzerland), 2021, 10, 1052. | 3.1 | 5 |
| 9 | Live Demonstration: A 0.8V, 1.54 pJ / 940 MHz Dual Mode Logic-Based 16x16-Bit Booth Multiplier in 16-nm FinFET. , 2021, , . | | 0 |
| 10 | Live Demo: Silicon Evaluation of Multimode Dual Mode Logic for PVT-Aware Datapaths. , 2021, , . | | 0 |
| 11 | Ultralow Voltage FinFET- Versus TFET-Based STT-MRAM Cells for IoT Applications. Electronics (Switzerland), 2021, 10, 1756. | 3.1 | 14 |
| 12 | Assessment of 10 nm Tunnel- FETs and FinFETs transistors for ultra-low voltage and high-speed digital circuits. , 2021, , . | | 0 |
| 13 | Robust Dual Mode Pass Logic (DMPL) for Energy Efficiency and High Performance. , 2020, , . | | 3 |
| 14 | A 0.8-V, 1.54-pJ/940-MHz Dual-Mode Logic-Based 16Ã—16-b Booth Multiplier in 16-nm FinFET. IEEE Solid-State Circuits Letters, 2020, 3, 314-317. | 2.0 | 17 |
| 15 | Exploiting Single-Well Design for Energy-Efficient Ultra-Wide Voltage Range Dual Mode Logic-Based Digital Circuits in 28nm FD-SOI Technology. , 2020, , . | | 0 |
| 16 | Dual Mode Logic Address Decoder. , 2020, , . | | 4 |
| 17 | Silicon Evaluation of Multimode Dual Mode Logic for PVT-Aware Datapaths. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1639-1643. | 3.0 | 10 |
| 18 | An 88-fJ/40-MHz [0.4 V]â€“0.61-pJ/1-GHz [0.9 V] Dual-Mode Logic 8 <inline-formula> <tex-math notation="LaTeX">$imes$ </tex-math> </inline-formula> 8 bit Multiplier Accumulator With a Self-Adjustment Mechanism in 28-nm FD-SOI. IEEE Journal of Solid-State Circuits, 2019, 54, 560-568. | 5.4 | 31 |

| # | Article | IF | Citations |
|---|---|---|---|
| 19 | Extended exploration of low granularity back biasing control in 28nm UTBB FD-SOI technology. , 2016, , . | | 7 |
| 20 | Low voltage logic circuits exploiting gate level dynamic body biasing in 28 nm UTBB FD-SOI. Solid-State Electronics, 2016, 117, 185-192. | 1.4 | 38 |
| 21 | Ultra-Low-Voltage Self-Body Biasing Scheme and Its Application to Basic Arithmetic Circuits. VLSI Design, 2015, 2015, 1-10. | 0.5 | 8 |
| 22 | Low voltage ripple carry adder with low-granularity dynamic forward back-biasing in 28 nm UTBB FD-SOI. , 2015, , . | | 2 |
| 23 | Exploring back biasing opportunities in 28nm UTBB FD-SOI technology for subthreshold digital design. , 2014, , . | | 10 |
| 24 | Dynamic gate-level body biasing for subthreshold digital design. , 2014, , . | | 10 |