

# Ramiro Taco

## List of Publications by Year in descending order

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24  
papers

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citations

1478505

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docs citations

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times ranked

102  
citing authors

#	ARTICLE	IF	CITATIONS
1	Low voltage logic circuits exploiting gate level dynamic body biasing in 28 nm UTBB FD-SOI. Solid-State Electronics, 2016, 117, 185-192.	1.4	38
2	An 88-fj/40-MHz [0.4 V]â€“0.61-pj/1-GHz [0.9 V] Dual-Mode Logic & 8 bit Multiplier Accumulator With a Self-Adjustment Mechanism in 28-nm FD-SOI. IEEE Journal of Solid-State Circuits, 2019, 54, 560-568.	5.4	31
3	A 0.8-V, 1.54-pj/940-MHz Dual-Mode Logic-Based 16Ã—16-b Booth Multiplier in 16-nm FinFET. IEEE Solid-State Circuits Letters, 2020, 3, 314-317.	2.0	17
4	Ultralow Voltage FinFET- Versus TFET-Based STT-MRAM Cells for IoT Applications. Electronics (Switzerland), 2021, 10, 1756.	3.1	14
5	Exploring back biasing opportunities in 28nm UTBB FD-SOI technology for subthreshold digital design. , 2014, , .		10
6	Dynamic gate-level body biasing for subthreshold digital design. , 2014, , .		10
7	Silicon Evaluation of Multimode Dual Mode Logic for PVT-Aware Datapaths. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1639-1643.	3.0	10
8	Ultra-Low-Voltage Self-Body Biasing Scheme and Its Application to Basic Arithmetic Circuits. VLSI Design, 2015, 2015, 1-10.	0.5	8
9	Extended exploration of low granularity back biasing control in 28nm UTBB FD-SOI technology. , 2016, , .		7
10	Energy Efficient Self-Adaptive Dual Mode Logic Address Decoder. Electronics (Switzerland), 2021, 10, 1052.	3.1	5
11	Dual Mode Logic Address Decoder. , 2020, , .		4
12	Robust Dual Mode Pass Logic (DMPL) for Energy Efficiency and High Performance. , 2020, , .		3
13	A Method for Mitigation of Droop Timing Errors Including a 500 MHz Droop Detector and Dual Mode Logic. IEEE Journal of Solid-State Circuits, 2022, 57, 596-608.	5.4	3
14	Low voltage ripple carry adder with low-granularity dynamic forward back-biasing in 28 nm UTBB FD-SOI. , 2015, , .		2
15	Performance Benchmarking of TFET and FinFET Digital Circuits from a Synthesis-Based Perspective. Electronics (Switzerland), 2022, 11, 632.	3.1	2
16	High-Speed and Low-Energy Dual-Mode Logic based Single-Clack-Cycle Binary Comparator. , 2021, , .		1
17	From 32 nm to TFET Technology: New Perspectives for Ultra-Scaled RF-DC Multiplier Circuits. Electronics (Switzerland), 2022, 11, 525.	3.1	1
18	Voltage and Technology Scaling of DMTJ-based STT-MRAMs for Energy-Efficient Embedded Memories. , 2022, , .		1

#	ARTICLE	IF	CITATIONS
19	Energy-Efficient FinFET-Versus TFET-Based STT-MRAM Bitcells. , 2022, , .		1
20	Exploiting Single-Well Design for Energy-Efficient Ultra-Wide Voltage Range Dual Mode Logic-Based Digital Circuits in 28nm FD-SOI Technology. , 2020, , .		0
21	Live Demonstration: A 0.8V, 1.54 pJ / 940 MHz Dual Mode Logic-Based 16x16-Bit Booth Multiplier in 16-nm FinFET. , 2021, , .		0
22	Live Demo: Silicon Evaluation of Multimode Dual Mode Logic for PVT-Aware Datapaths. , 2021, , .		0
23	Assessment of 10 nm Tunnel- FETs and FinFETs transistors for ultra-low voltage and high-speed digital circuits. , 2021, , .		0
24	DMTJ-Based Non-Volatile Ternary Content Addressable Memory for Energy-Efficient High-Performance Systems. , 2022, , .		0