Pedro Reviriego

List of Publications by Year
in descending order

173 papers	2,506 citations	279487 23 h-index	344852 36 g-index
175 all docs	175 docs citations	175 times ranked	1258 citing authors

#	Article	IF	Citations
1	Correction Masking: A Technique to Implement Efficient SET Tolerant Error Correction Decoders. IEEE Transactions on Device and Materials Reliability, 2022, 22, 36-41.	1.5	1
2	A Near-Sensor ECG Delineation and Arrhythmia Classification System. IEEE Sensors Journal, 2022, 22, 14217-14227.	2.4	4
3	Detection of Limited Magnitude Errors in Emerging Multilevel Cell Memories by One-Bit Parity (OBP) or Two-Bit Parity (TBP). IEEE Transactions on Emerging Topics in Computing, 2021, 9, 1792-1802.	3.2	14
4	Reduced Precision Redundancy for Reliable Processing of Data. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 1960-1971.	3.2	6
5	Voting Margin: A Scheme for Error-Tolerant k Nearest Neighbors Classifiers for Machine Learning. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 2089-2098.	3.2	7
6	Soft Error Tolerant Count Min Sketches. IEEE Transactions on Computers, 2021, 70, 284-290.	2.4	5
7	Less-is-Better Protection (LBP) for memory errors in kNNs classifiers. Future Generation Computer Systems, 2021, 117, 401-411.	4.9	1
8	Protecting Memories against Soft Errors: The Case for Customizable Error Correction Codes. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 651-663.	3.2	2
9	Fault Tolerant Polyphase Filters-based Decimators for SRAM-based FPGA Implementations. IEEE Transactions on Emerging Topics in Computing, 2021, , 1-1.	3.2	2
10	VR-ZYCAP: A Versatile Resourse-Level ICAP Controller for ZYNQ SOC. Electronics (Switzerland), 2021, 10, 899.	1.8	2
11	Ensemble of Pruned Networks for Reliable Classifiers. , 2021, , .		2
12	Avoiding Flow Size Overestimation in Count-Min Sketch With Bloom Filter Constructions. IEEE Transactions on Network and Service Management, 2021, 18, 3662-3676.	3.2	7
13	Improving Packet Flow Counting With Fingerprint Counting. IEEE Communications Letters, 2020, 24, 76-80.	2.5	4
14	Exploiting Asymmetry in eDRAM Errors for Redundancy-Free Error-Tolerant Design. IEEE Transactions on Emerging Topics in Computing, 2020, , 1-1.	3.2	4
15	Cuckoo Filters and Bloom Filters: Comparison and Application to Packet Classification. IEEE Transactions on Network and Service Management, 2020, 17, 2690-2701.	3.2	23
16	Error-Tolerant Computation for Voting Classifiers With Multiple Classes. IEEE Transactions on Vehicular Technology, 2020, 69, 13718-13727.	3.9	7
17	Isolation Design Flow Effectiveness Evaluation Methodology for Zynq SoCs. Electronics (Switzerland), 2020, 9, 814.	1.8	1
18	Fast Updates for Line-Rate HyperLogLog-Based Cardinality Estimation. IEEE Communications Letters, 2020, 24, 2737-2741.	2.5	3

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19	A Microprocessor Protection Architecture against Hardware Trojans in Memories. , 2020, , .		13
20	Codes for Limited Magnitude Error Correction in Multilevel Cell Memories. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1615-1626.	3.5	5
21	BPR-TCAMâ€"Block and Partial Reconfiguration based TCAM on Xilinx FPGAs. Electronics (Switzerland), 2020, 9, 353.	1.8	7
22	Toward a Fault-Tolerant Star Tracker for Small Satellite Applications. IEEE Transactions on Aerospace and Electronic Systems, 2020, 56, 3421-3431.	2.6	7
23	Security of HyperLogLog (HLL) Cardinality Estimation: Vulnerabilities and Protection. IEEE Communications Letters, 2020, 24, 976-980.	2.5	17
24	Scheme for periodical concurrent fault detection in parallel CRC circuits. IET Computers and Digital Techniques, 2020, 14, 80-85.	0.9	2
25	Denial of Service Attack on Cuckoo Filter Based Networking Systems. IEEE Communications Letters, 2020, 24, 1428-1432.	2.5	12
26	Adaptive Cuckoo Filters. Journal of Experimental Algorithmics, 2020, 25, 1-20.	0.7	14
27	Constructions and Applications for Accurate Counting of the Bloom Filter False Positive Free Zone. , 2020, , .		11
28	Faking Elephant Flows on the Count Min Sketch. IEEE Networking Letters, 2020, 2, 199-202.	1.5	3
29	Reliable Classification with Ensemble Convolutional Neural Networks. , 2020, , .		1
30	Reduction of Parity Overhead in a Subset of Orthogonal Latin Square Codes. , 2020, , .		1
31	Protection Scheme for Star Tracker Images. IEEE Transactions on Aerospace and Electronic Systems, 2019, 55, 486-492.	2.6	4
32	Reliability characterization and activity analysis of lowRISC internal modules against single event upsets using fault injection and RTL simulation. Microprocessors and Microsystems, 2019, 71, 102871.	1.8	4
33	Design and Implementation of Configuration Memory SEU-Tolerant Viterbi Decoders in SRAM-Based FPGAs. IEEE Nanotechnology Magazine, 2019, 18, 691-699.	1.1	12
34	Protecting Large Word Size Memories against MCUs with 3-bit Burst Error Correction. , 2019, , .		1
35	Efficient Concurrent Error Detection for SEC-DAEC Encoders. , 2019, , .		1
36	The Tandem Counting Bloom Filter - It Takes Two Counters to Tango. IEEE/ACM Transactions on Networking, 2019, 27, 2252-2265.	2.6	9

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37	CFBF: Reducing the Insertion Time of Cuckoo Filters With an Integrated Bloom Filter. IEEE Communications Letters, 2019, 23, 1857-1861.	2.5	9
38	Low delay Single Error Correction and Double Adjacent Error Correction (SEC-DAEC) codes. Microelectronics Reliability, 2019, 97, 31-37.	0.9	12
39	Low Delay 3-Bit Burst Error Correction Codes. Journal of Electronic Testing: Theory and Applications (JETTA), 2019, 35, 413-420.	0.9	6
40	PR-TCAM: Efficient TCAM Emulation on Xilinx FPGAs Using Partial Reconfiguration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1952-1956.	2.1	25
41	An ALU Protection Methodology for Soft Processors on SRAM-Based FPGAs. IEEE Transactions on Computers, 2019, 68, 1404-1410.	2.4	20
42	A Radiation Tolerant 10/100 Ethernet Transceiver for Space Applications. , 2019, , .		1
43	Reliability Evaluation of Polyphase-filter based Decimators Implemented on SRAM-FPGAs. , 2019, , .		2
44	Two Bit Overlap: A Class of Double Error Correction One Step Majority Logic Decodable Codes. IEEE Transactions on Computers, 2019, 68, 798-803.	2.4	2
45	Error Detection and Correction in SRAM Emulated TCAMs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 486-490.	2.1	18
46	Improving Instruction TLB Reliability with Efficient Multi-bit Soft Error Protection. Microelectronics Reliability, 2019, 93, 29-38.	0.9	2
47	Efficient Implementations of Reduced Precision Redundancy (RPR) Multiply and Accumulate (MAC). IEEE Transactions on Computers, 2019, 68, 784-790.	2.4	24
48	A Scheme to Design Concurrent Error Detection Techniques for the Fast Fourier Transform Implemented in SRAM-Based FPGAs. IEEE Transactions on Computers, 2018, 67, 1039-1045.	2.4	11
49	Evaluating the Impact of the Instruction Set on Microprocessor Reliability to Soft Errors. IEEE Transactions on Device and Materials Reliability, 2018, 18, 70-79.	1.5	19
50	Opcode vector: An efficient scheme to detect soft errors in instructions. Microelectronics Reliability, 2018, 86, 92-97.	0.9	1
51	Majority Voting-Based Reduced Precision Redundancy Adders. IEEE Transactions on Device and Materials Reliability, 2018, 18, 122-124.	1.5	20
52	Fault tolerant encoders for Single Error Correction and Double Adjacent Error Correction codes. Microelectronics Reliability, 2018, 81, 167-173.	0.9	6
53	A Double Error Correction Code for 32-Bit Data Words With Efficent Decoding. IEEE Transactions on Device and Materials Reliability, 2018, 18, 125-127.	1.5	10
54	A Fast Technique to Reduce Power Consumption on Linear Block Codes Used to Protect Registers. IEEE Transactions on Device and Materials Reliability, 2018, 18, 189-196.	1.5	1

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55	An Efficient Methodology for On-Chip SEU Injection in Flip-Flops for Xilinx FPGAs. IEEE Transactions on Nuclear Science, 2018, 65, 989-996.	1.2	19
56	Efficient Implementations of 4-Bit Burst Error Correction for Memories. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 2037-2041.	2.2	18
57	EMOMA: Exact Match in One Memory Access. IEEE Transactions on Knowledge and Data Engineering, 2018, 30, 2120-2133.	4.0	13
58	Modular fault tolerant processor architecture on a SoC for space. Microelectronics Reliability, 2018, 83, 84-90.	0.9	3
59	Efficient Fault-Tolerant Design for Parallel Matched Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 366-370.	2.2	7
60	An Efficient Fault-Tolerance Design for Integer Parallel Matrixâ€“Vector Multiplications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 211-215.	2.1	3
61	Reducing the Power Consumption of Fault Tolerant Registers Through Hybrid Protection. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1293-1302.	3.5	4
62	Efficient Protection of the Register File in Soft-Processors Implemented on Xilinx FPGAs. IEEE Transactions on Computers, 2018, 67, 299-304.	2.4	15
63	Protecting Image Processing Pipelines against Configuration Memory Errors in SRAM-Based FPGAs. Electronics (Switzerland), 2018, 7, 322.	1.8	4
64	Multiple Cell Upset Injection in BRAMs for Xilinx FPGAs. IEEE Transactions on Device and Materials Reliability, 2018, 18, 636-638.	1.5	5
65	Analysis of the Effects of Single Event Upsets (SEUs) on User Memory in FPGA Implemented Viterbi Decoders. , 2018, , .		2
66	Enhancing Instruction TLB Resilience to Soft Errors. IEEE Transactions on Computers, 2018, , 1-1.	2.4	4
67	Seu and Sefi error detection and correction on a ddr3 memory system. Microelectronics Reliability, 2018, 91, 23-30.	0.9	1
68	Dependability Solutions. , 2018, , 155-188.		2
69	Cuckoo Cache a Technique to Improve Flow Monitoring Throughput. IEEE Internet Computing, 2018, , 1-1.	3.2	0
70	Comments on â€œExtend orthogonal Latin square codes for 32-bit data protection in memory applicationsâ€•Microelectron. Reliab. 63, 278â€“283 (2016). Microelectronics Reliability, 2017, 69, 126-129.	0.9	1
71	Combined Modular Key and Data Error Protection for Content-Addressable Memories. IEEE Transactions on Computers, 2017, 66, 1085-1090.	2.4	4
72	Error Detection Technique for a Median Filter. IEEE Transactions on Nuclear Science, 2017, , 1-1.	1.2	16

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73	Single Event Transient Tolerant Bloom Filter Implementations. IEEE Transactions on Computers, 2017, 66, 1831-1836.	2.4	11
74	Evaluating Direct Compare for Double Error-Correction Codes. IEEE Transactions on Device and Materials Reliability, 2017, 17, 802-804.	1.5	7
75	A Scheme to Improve the Intrinsic Error Detection of the Instruction Set Architecture. IEEE Computer Architecture Letters, 2017, 16, 103-106.	1.0	12
76	Detecting errors in instructions with bloom filters. , 2017, , .		5
77	SEFI Protection for Nanosat 16-Bit Chip Onboard Computer Memories. IEEE Transactions on Device and Materials Reliability, 2017, 17, 698-707.	1.5	11
78	Flexible Packet Matching with Single Double Cuckoo Hash. , 2017, 55, 212-217.		11
79	Improving counting Bloom filter performance with fingerprints. Information Processing Letters, 2016, 116, 304-309.	0.4	26
80	Reducing the Cost of Triple Adjacent Error Correction in Double Error Correction Orthogonal Latin Square Codes. IEEE Transactions on Device and Materials Reliability, 2016, 16, 269-271.	1.5	7
81	Combined SEU and SEFI Protection for Memories Using Orthogonal Latin Square Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1933-1943.	3.5	16
82	Optimizing the Implementation of SECâ€“DAEC Codes in FPGAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3538-3542.	2.1	4
83	Cuckoo Cache: A Technique to Improve Flow Monitoring Throughput. IEEE Internet Computing, 2016, 20, 46-53.	3.2	4
84	Implementing Double Error Correction Orthogonal Latin Squares Codes in SRAM-based FPGAs. Microelectronics Reliability, 2016, 56, 221-227.	0.9	6
85	Unequal Error Protection Codes Derived from Double Error Correction Orthogonal Latin Square Codes. IEEE Transactions on Computers, 2016, 65, 2932-2938.	2.4	5
86	OMASS: One Memory Access Set Separation. IEEE Transactions on Knowledge and Data Engineering, 2016, 28, 1940-1943.	4.0	10
87	Oddâ€weightâ€column SECâ€“DEDâ€“TAED codes. Electronics Letters, 2016, 52, 119-120.	0.5	3
88	A Method to Design Single Error Correction Codes With Fast Decoding for a Subset of Critical Bits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 171-175.	2.2	10
89	Parallel d-Pipeline: A Cuckoo Hashing Implementation for Increased Throughput. IEEE Transactions on Computers, 2016, 65, 326-331.	2.4	23
90	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 769-773.	2.1	21

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91	Efficient Coding Schemes for Fault-Tolerant Parallel Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 666-670.	2.2	9
92	MCU Tolerance in SRAMs Through Low-Redundancy Triple Adjacent Error Correction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2332-2336.	2.1	53
93	Packet Coalescing Strategies for Energy Efficient High-Speed Communications Over Plastic Optical Fibers. Journal of Optical Communications and Networking, 2015, 7, 253.	3.3	2
94	Low Delay Single Symbol Error Correction Codes Based on Reed Solomon Codes. IEEE Transactions on Computers, 2015, 64, 1497-1501.	2.4	30
95	FastTag: A Technique to Protect Cache Tags Against Soft Errors. IEEE Transactions on Device and Materials Reliability, 2014, 14, 935-937.	1.5	14
96	A Method to Design SEC-DED-DAEC Codes With Optimized Decoding. IEEE Transactions on Device and Materials Reliability, 2014, 14, 884-889.	1.5	36
97	Hamming SEC-DAED and Extended Hamming SEC-DED-TAED Codes Through Selective Shortening and Bit Placement. IEEE Transactions on Device and Materials Reliability, 2014, 14, 574-576.	1.5	57
98	Energy Efficient Exact Matching for Flow Identification with Cuckoo Affinity Hashing. IEEE Communications Letters, 2014, 18, 885-888.	2.5	6
99	Optimized parallel decoding of difference set codes for high speed memories. Microelectronics Reliability, 2014, 54, 2645-2648.	0.9	3
100	A Method to Extend Orthogonal Latin Square Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1635-1639.	2.1	15
101	Improving the performance of Invertible Bloom Lookup Tables. Information Processing Letters, 2014, 114, 185-191.	0.4	10
102	Error Correction Coding for Electronic Circuits. , 2014, , 137-168.		3
103	Error Detection in Majority Logic Decoding of Euclidean Geometry Low Density Parity Check (EG-LDPC) Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 156-159.	2.1	34
104	A Method to Construct Low Delay Single Error Correction Codes for Protecting Data Bits Only. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 479-483.	1.9	42
105	Introducing energy efficiency in the VDE 0885-763 standard for high speed communication over plastic optical fibers. , 2013, 51, 97-102.		6
106	Reducing the Cost of Single Error Correction With Parity Sharing. IEEE Transactions on Device and Materials Reliability, 2013, 13, 420-422.	1.5	4
107	Efficient single event upset-tolerant FIR filter design based on residue number for OBP satellite communication systems. China Communications, 2013, 10, 55-67.	2.0	5
108	Enhanced Duplication: a Technique to Correct Soft Errors in Narrow Values. IEEE Computer Architecture Letters, 2013, 12, 13-16.	1.0	3

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109	Low Complexity Concurrent Error Detection for Complex Multiplication. IEEE Transactions on Computers, 2013, 62, 1899-1903.	2.4	11
110	An Efficient Technique to Protect Serial Shift Registers Against Soft Errors. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 512-516.	2.2	4
111	Soft error tolerant Content Addressable Memories (CAMs) using error detection codes and duplication. Microprocessors and Microsystems, 2013, 37, 1103-1107.	1.8	3
112	Performance analysis of Energy Efficient Ethernet on video streaming servers. Computer Networks, 2013, 57, 599-608.	3.2	6
113	Efficient Arithmetic-Residue-Based SEU-Tolerant FIR Filter Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 497-501.	2.2	13
114	Using Single Error Correction Codes to Protect Against Isolated Defects and Soft Errors. IEEE Transactions on Reliability, 2013, 62, 238-243.	3.5	8
115	Concurrent Error Detection for Orthogonal Latin Squares Encoders and Syndrome Computation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 2334-2338.	2.1	20
116	Reducing the Cost of Implementing Error Correction Codes in Content Addressable Memories. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 432-436.	2.2	6
117	Diverse Double Modular Redundancy: A New Direction for Soft-Error Detection and Correction. IEEE Design and Test, 2013, 30, 87-95.	1.1	24
118	Verification of SRAM MСUs calculation technique for experiment time optimization. , 2013, , .		3
119	Area efficient concurrent error detection and correction for parallel filters. Electronics Letters, 2012, 48, 1258.	0.5	17
120	Low-cost single error correction multiple adjacent error correction codes. Electronics Letters, 2012, 48, 1470.	0.5	10
121	A (64,45) Triple Error Correction Code for Memory Applications. IEEE Transactions on Device and Materials Reliability, 2012, 12, 101-106.	1.5	20
122	Comparison of the Susceptibility to Soft Errors of SRAM-Based FPGA Error Correction Codes Implementations. IEEE Transactions on Nuclear Science, 2012, 59, 619-624.	1.2	12
123	Network monitoring for energy efficiency in large-scale networks: the case of the Spanish Academic Network. Journal of Supercomputing, 2012, 62, 1284-1304.	2.4	1
124	Implementing Concurrent Error Detection in Infinite-Impulse-Response Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 583-586.	2.2	5
125	Low Power embedded DRAM caches using BCH code partitioning. , 2012, , .		7
126	Enhanced Detection of Double and Triple Adjacent Errors in Hamming Codes Through Selective Bit Placement. IEEE Transactions on Device and Materials Reliability, 2012, 12, 357-362.	1.5	44

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127	Efficient error detection in Double Error Correction BCH codes for memory applications. Microelectronics Reliability, 2012, 52, 1528-1530.	0.9	26
128	Multiple Cell Upset Correction in Memories Using Difference Set Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 2592-2599.	3.5	32
129	On the Use of Euclidean Geometry Codes for Efficient Multibit Error Correction on Memory Systems. IEEE Transactions on Nuclear Science, 2012, 59, 824-828.	1.2	6
130	Error-Detection Enhanced Decoding of Difference Set Codes for Memory Applications. IEEE Transactions on Device and Materials Reliability, 2012, 12, 335-340.	1.5	9
131	Efficient Majority Logic Fault Detection With Difference-Set Codes for Memory Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 148-156.	2.1	62
132	Structural DMR: A Technique for Implementation of Soft-Error-Tolerant FIR Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 512-516.	2.2	27
133	Memory Reliability Model for Accumulated and Clustered Soft Errors. IEEE Transactions on Nuclear Science, 2011, 58, 2483-2492.	1.2	13
134	Increasing Reliability of FPGA-Based Adaptive Equalizers in the Presence of Single Event Upsets. IEEE Transactions on Nuclear Science, 2011, 58, 1072-1077.	1.2	17
135	Improving Memory Reliability Against Soft Errors Using Block Parity. IEEE Transactions on Nuclear Science, 2011, 58, 981-986.	1.2	15
136	A Simple Analytical Model for Energy Efficient Ethernet. IEEE Communications Letters, 2011, 15, 773-775.	2.5	45
137	Mitigating the effects of large multiple cell upsets (MCUs) in memories. ACM Transactions on Design Automation of Electronic Systems, 2011, 16, 1-10.	1.9	3
138	A fast and efficient technique to apply Selective TMR through optimization. Microelectronics Reliability, 2011, 51, 2388-2401.	0.9	8
139	An Initial Evaluation of Energy Efficient Ethernet. IEEE Communications Letters, 2011, 15, 578-580.	2.5	76
140	Offset DMR: A Low Overhead Soft Error Detection and Correction Technique for Transform-Based Convolution. IEEE Transactions on Computers, 2011, 60, 1511-1516.	2.4	4
141	Fault Tolerant Single Error Correction Encoders. Journal of Electronic Testing: Theory and Applications (JETTA), 2011, 27, 215-218.	0.9	13
142	Towards an energy efficient 10 Gb/s optical ethernet: Performance analysis and viability. Optical Switching and Networking, 2011, 8, 131-138.	1.2	23
143	Designing ad-hoc scrubbing sequences to improve memory reliability against soft errors. , 2011, , .		1
144	Soft error tolerant Infinite Impulse Response filters using reduced precision replicas. , 2011, , .		7

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145	Reliability analysis of memories protected with BICS and a per-word parity bit. ACM Transactions on Design Automation of Electronic Systems, 2010, 15, 1-15.	1.9	5
146	Enhanced Implementations of Hamming Codes to Protect FIR Filters. IEEE Transactions on Nuclear Science, 2010, 57, 2112-2118.	1.2	6
147	Matrix-Based Codes for Adjacent Error Correction. IEEE Transactions on Nuclear Science, 2010, 57, 2106-2111.	1.2	37
148	IEEE 802.3az: the road to energy efficient ethernet. , 2010, 48, 50-56.		255
149	Burst Transmission in Energy Efficient Ethernet. IEEE Internet Computing, 2010, , .	3.2	51
150	Energy Efficiency in Industrial Ethernet: The Case of Powerlink. IEEE Transactions on Industrial Electronics, 2010, 57, 2896-2903.	5.2	27
151	Number of Events and Time to Failure Distributions for Error Correction Protected Memories. IEEE Transactions on Device and Materials Reliability, 2010, 10, 381-389.	1.5	3
152	Optimizing Scrubbing Sequences for Advanced Computer Memories. IEEE Transactions on Device and Materials Reliability, 2010, 10, 192-200.	1.5	11
153	Protection of Memories Suffering MCUs Through the Selection of the Optimal Interleaving Distance. IEEE Transactions on Nuclear Science, 2010, 57, 2124-2128.	1.2	38
154	Efficient Soft Error-Tolerant Adaptive Equalizers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2032-2040.	3.5	11
155	Soft error detection and correction for FFT based convolution using different block lengths. , 2009, , .		3
156	Reliability of Single-Error Correction Protected Memories. IEEE Transactions on Reliability, 2009, 58, 193-201.	3.5	21
157	A method to eliminate the event accumulation problem from a memory affected by multiple bit upsets. Microelectronics Reliability, 2009, 49, 707-715.	0.9	4
158	Assembly admission control based on random packet selection at border nodes in Optical Burst-Switched networks. Photonic Network Communications, 2009, 18, 39-48.	1.4	3
159	Efficient error detection codes for multiple-bit upset correction in SRAMs with BICS. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-10.	1.9	14
160	Performance Evaluation and Design of Polymorphous OBS Networks With Guaranteed TDM Services. Journal of Lightwave Technology, 2009, 27, 2495-2505.	2.7	6
161	A Methodology for Automatic Insertion of Selective TMR in Digital Circuits Affected by SEUs. IEEE Transactions on Nuclear Science, 2009, 56, 2091-2102.	1.2	55
162	Performance evaluation of energy efficient ethernet. IEEE Communications Letters, 2009, 13, 697-699.	2.5	112

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163	Study of the Effects of Multibit Error Correction Codes on the Reliability of Memories in the Presence of MBUs. IEEE Transactions on Device and Materials Reliability, 2009, 9, 31-39.	1.5	21
164	Selection of the Optimal Memory Configuration in a System Affected by Soft Errors. IEEE Transactions on Device and Materials Reliability, 2009, 9, 403-411.	1.5	10
165	Blocking models of optical burst switches with shared wavelength converters: exact formulations and analytical approximations. Photonic Network Communications, 2008, 16, 61-70.	1.4	4
166	Analysis of Blocking Probability of Data Bursts With Continuous-Time Variable Offsets in Single-Wavelength OBS Switches. Journal of Lightwave Technology, 2008, 26, 1559-1568.	2.7	11
167	Study of the effects of MBUs on the reliability of a 150 nm SRAM device. , 2008, , .		22
168	Efficient Protection Techniques Against SEUs for Adaptive Filters: An Echo Canceller Case Study. IEEE Transactions on Nuclear Science, 2008, 55, 1700-1707.	1.2	18
169	Reliability Analysis of Memories Suffering Multiple Bit Upsets. IEEE Transactions on Device and Materials Reliability, 2007, 7, 592-601.	1.5	57
170	New Protection Techniques Against SEUs for Moving Average Filters in a Radiation Environment. IEEE Transactions on Nuclear Science, 2007, 54, 957-964.	1.2	28
171	Analysis of average burst-assembly delay and applications in proportional service differentiation. Photonic Network Communications, 2007, 14, 183-197.	1.4	9
172	New Alternatives to the Estimation Problem in Hardware-Software Codesign of Complex Embedded Systems: The H.261 Video Co-dec Case Study. Design Automation for Embedded Systems, 2004, 9, 193-210.	0.7	0
173	Energy Efficiency in Ethernet. , 0, , 277-290.		0