Macarena C MartÃ-nez-RodrÃ-guez

List of Publications by Year
in descending order

21 papers	103 citations	1684188 5 h-index	1588992 8 g-index
22 all docs	22 docs citations	22 times ranked	76 citing authors

#	Article	IF	Citations
1	Multi-Unit Serial Polynomial Multiplier to Accelerate NTRU-Based Cryptographic Schemes in IoT Embedded Systems. Sensors, 2022, 22, 2057.	3.8	5
2	Timing-Optimized Hardware Implementation to Accelerate Polynomial Multiplication in the NTRU Algorithm. ACM Journal on Emerging Technologies in Computing Systems, 2021, 17, 1-16.	2.3	6
3	A Configurable RO-PUF for Securing Embedded Systems Implemented on Programmable Devices. Electronics (Switzerland), 2021, 10, 1957.	3.1	6
4	SoK: Remote Power Analysis. , 2021, , .		3
5	Design Flow to Evaluate the Performance of Ring Oscillator PUFs on FPGAs. , 2021, , .		1
6	Hardware Implementation of Authenticated Ciphers for Embedded Systems. IEEE Latin America Transactions, 2020, 18, 1581-1591.	1.6	2
7	Accelerating the Development of NTRU Algorithm on Embedded Systems. , 2020, , .		3
8	VLSI Design of Trusted Virtual Sensors. Sensors, 2018, 18, 347.	3.8	7
9	A comparative analysis of VLSI trusted virtual sensors. Microprocessors and Microsystems, 2018, 61, 108-116.	2.8	1
10	CMOS digital design of a trusted virtual sensor. , 2017, , .		1
11	Application specific integrated circuit solution for multiâ€input multiâ€output piecewiseâ€affine functions. International Journal of Circuit Theory and Applications, 2016, 44, 4-20.	2.0	5
12	Dedicated hardware IP module for fingerprint recognition. , 2015, , .		1
13	Programmable ASICs for model predictive control. , 2015, , .		2
14	Digital VLSI Implementation of Piecewise-Affine Controllers Based on Lattice Approach. IEEE Transactions on Control Systems Technology, 2015, 23, 842-854.	5.2	12
15	Dedicated hardware IP module for extracting singular points from fingerprints. , 2014, , .		0
16	A Programmable and Configurable ASIC to Generate Piecewise-Affine Functions Defined Over General Partitions. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 3182-3194.	5.4	8
17	Reducing bit flipping problems in SRAM physical unclonable functions for chip identification. , 2012, , .		16
18	ASIC-in-the-loop methodology for verification of piecewise affine controllers. , 2012, , .		2

#	Article	IF	Citations
19	Design methodology for FPGA implementation of lattice piecewise-affine functions. , 2011, , .		6
20	Digital implementation of hierarchical piecewise-affine controllers. , 2011, , .		10
21	Circuit implementation of piecewise-affine functions based on lattice representation. , 2011, , .		6