Paulo Flores

List of Publications by Year
in descending order

61	641	759233 12	713466 21
papers	citations	h-index	g-index

63	63	63	252
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Radixâ€2 ^r recoding with common subexpression elimination for multiple constant multiplication. IET Circuits, Devices and Systems, 2020, 14, 990-994.	1.4	1
2	A variable RADIX-2^ralgorithm for single constant multiplication. , 2017, , .		1
3	A novel method for the approximation of multiplierless constant matrix vector multiplication. Eurasip Journal on Embedded Systems, 2016, 2016, .	1.2	6
4	A Novel Method for the Approximation of Multiplierless Constant Matrix Vector Multiplication. , 2015, , .		2
5	Approximation of multiple constant multiplications using minimum look-up tables on FPGA. , 2015, , .		3
6	Exact and Approximate Algorithms for the Filter Design Optimization Problem. IEEE Transactions on Signal Processing, 2015, 63, 142-154.	5.3	12
7	Quaternary Logic Lookup Table in Standard CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 306-316.	3.1	14
8	Multicore SIMD ASIP for Next-Generation Sequencing and Alignment Biochip Platforms. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1287-1300.	3.1	21
9	Multiplierless Design of Folded DSP Blocks. ACM Transactions on Design Automation of Electronic Systems, 2014, 20, 1-24.	2.6	6
10	Optimization of design complexity in time-multiplexed constant multiplications. , 2014, , .		0
11	ECHO: A novel method for the multiplierless design of constant array vector multiplication. , 2014, , .		3
12	Efficient design of FIR filters using hybrid multiple constant multiplications on FPGA. , 2014, , .		5
13	A Tutorial on Multiplierless Design of FIR Filters: Algorithms and Architectures. Circuits, Systems, and Signal Processing, 2014, 33, 1689-1719.	2.0	32
14	Optimized ASIP architecture for compressed BWT-indexed search in bioinformatics applications. , 2014, , .		2
15	Optimization of design complexity in time-multiplexed constant multiplications. , 2014, , .		1
16	Configurable and scalable class of high performance hardware accelerators for simultaneous DNA sequence alignment. Concurrency Computation Practice and Experience, 2013, 25, 1319-1339.	2.2	4
17	BioBlaze: Multi-core SIMD ASIP for DNA sequence alignment. , 2013, , .		8
18	Standard CMOS voltage-mode QLUT using a clock boosting technique. , 2013, , .		0

#	Article	IF	Citations
19	Towards the least complex time-multiplexed constant multiplication. , 2013, , .		0
20	Exploration of tradeoffs in the design of integer cosine transforms for image compression. , 2013, , .		0
21	Design of Digit-Serial FIR Filters: Algorithms, Architectures, and a CAD Tool. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 498-511.	3.1	23
22	SIREN. , 2013, , .		1
23	Optimization Algorithms for the Multiplierless Realization of Linear Transforms. ACM Transactions on Design Automation of Electronic Systems, 2012, 17, 1-27.	2.6	15
24	Multiple tunable constant multiplications. , 2012, , .		6
25	Design and characterization of a QLUT in a standard CMOS process. , 2012, , .		1
26	Integrated Hardware Architecture for Efficient Computation of the n-Best Bio-Sequence Local Alignments in Embedded Platforms. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1262-1275.	3.1	13
27	Design of low-complexity digital finite impulse response filters on FPGAs. , 2012, , .		6
28	Hardware accelerator architecture for simultaneous short-read DNA sequences alignment with enhanced traceback phase. Microprocessors and Microsystems, 2012, 36, 96-109.	2.8	8
29	High-level algorithms for the optimization of gate-level area in digit-serial multiple constant multiplications. The Integration VLSI Journal, 2012, 45, 294-306.	2.1	4
30	Multiplierless Design of Linear DSP Transforms. International Federation for Information Processing, 2012, , 73-93.	0.4	11
31	A hybrid algorithm for the optimization of area and delay in linear DSP transforms. , 2011, , .		1
32	Optimization of area in digit-serial Multiple Constant Multiplications at gate-level. , 2011, , .		10
33	Design of low-power multiple constant multiplications using low-complexity minimum depth operations. , 2011, , .		7
34	Finding the optimal tradeoff between area and delay in multiple constant multiplications. Microprocessors and Microsystems, 2011, 35, 729-741.	2.8	16
35	Efficient shift-adds design of digit-serial multiple constant multiplications. , 2011, , .		8
36	Optimization of gate-level area in high throughput Multiple Constant Multiplications. , 2011, , .		3

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37	Low Power Multiple-Value Voltage-Mode Look-Up Table for Quaternary Field Programmable Gate Arrays. Journal of Low Power Electronics, 2011, 7, 294-301.	0.6	0
38	Search algorithms for the multiple constant multiplications problem: Exact and approximate. Microprocessors and Microsystems, 2010, 34, 151-162.	2.8	75
39	Voltage-mode quaternary FPGAs: An evaluation of interconnections. , 2010, , .		0
40	Design of low-complexity and high-speed digital Finite Impulse Response filters. , 2010, , .		1
41	A new quaternary FPGA based on a voltage-mode multi-valued circuit. , 2010, , .		7
42	Optimization of Area and Delay at Gate-Level in Multiple Constant Multiplications. , 2010, , .		9
43	Integrated accelerator architecture for DNA sequences alignment with enhanced traceback phase. , 2010, , .		4
44	Generating realistic stimuli for accurate power grid analysis. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-26.	2.6	8
45	Power and delay comparison of binary and quaternary arithmetic circuits. , 2009, , .		5
46	Generating Worst-Case Stimuli for Accurate Power Grid Analysis. Lecture Notes in Computer Science, 2009, , 247-257.	1.3	8
47	Exact and Approximate Algorithms for the Optimization of Area and Delay in Multiple Constant Multiplications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1013-1026.	2.7	92
48	VHDL generation of optimized FIR filters. , 2008, , .		18
49	An Exact Breadth-First Search Algorithm for the Multiple Constant Multiplications Problem. , 2008, , .		28
50	Application Specific Programmable IP Core for Motion Estimation: Technology Comparison Targeting Efficient Embedded Co-Processing Units. , 2008, , .		2
51	Minimum number of operations under a general number representation for digital filter synthesis. , 2007, , .		7
52	Generating Realistic Stimuli for Accurate Power Grid Analysis. , 2007, , .		3
53	Effect of Number Representation on the Achievable Minimum Number of Operations in Multiple Constant Multiplications. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2007, , .	0.0	8
54	Optimization of area in digital FIR filters using gate-level metrics. Proceedings - Design Automation Conference, 2007, , .	0.0	13

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55	Optimization of Area in Digital FIR Filters using Gate-Level Metrics. Proceedings - Design Automation Conference, 2007, , .	0.0	11
56	ASSUMEs: Heuristic Algorithms for Optimization of Area and Delay in Digital Filter Synthesis. , 2006, , .		1
57	Optimization of area under a delay constraint in digital filter synthesis using SAT-based integer linear programming. , 2006, , .		2
58	Exploiting general coefficient representation for the optimal sharing of partial products in MCMs. , 2006, , .		4
59	An exact solution to the minimum size test pattern problem. ACM Transactions on Design Automation of Electronic Systems, 2001, 6, 629-644.	2.6	24
60	Maximal sharing of partial terms in MCM under minimal signed digit representation. , 0, , .		6
61	An exact algorithm for the maximal sharing of partial terms in multiple constant multiplications. , 0, , .		28