Cuong Pham-Quoc

List of Publications by Year
in descending order

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		1683934	1588896
34	110	5	8
papers	citations	h-index	g-index

36	36	36	62
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Highâ€performance anomaly intrusion detection system with ensemble neural networks on reconfigurable hardware. Concurrency Computation Practice and Experience, 2023, 35, e6370.	1.4	2
2	Building a smart traffic light system based on Internet of Things using â€calculus. Concurrency Computation Practice and Experience, 2022, 34, .	1.4	0
3	Low-Cost Area-Efficient FPGA-Based Multi-Functional ECDSA/EdDSA. Cryptography, 2022, 6, 25.	1.4	6
4	Towards An FPGA-targeted Hardware/Software Co-design Framework for CNN-based Edge Computing. Mobile Networks and Applications, 2022, 27, 2024-2035.	2.2	6
5	An FPGA-based Convolution IP Core for Deep Neural Networks Acceleration. REV Journal on Electronics and Communications, 2022, 12, .	0.2	3
6	A highâ€performance FPGAâ€based BWAâ€MEM DNA sequence alignment. Concurrency Computation Practice and Experience, 2021, 33, e5328.	1.4	9
7	Estimating Land Surface Temperature from Landsat-8 Images Based on a Cloud-Based Automated Processing Service. Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering, 2021, , 55-64.	0.2	0
8	Hardware/Software Co-design for Convolutional Neural Networks Acceleration: A Survey and Open Issues. Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering, 2021, , 164-178.	0.2	2
9	Heterogeneous Hardware-based Network Intrusion Detection System with Multiple Approaches for SDN. Mobile Networks and Applications, 2020, 25, 1178-1192.	2.2	13
10	Heterogeneous Hardware-assisted Parallel Processing for BWA-MEM DNA Alignment. , 2020, , .		0
11	Automatic FPGA-based Hardware Accelerator Design: A Case Study with Image Processing Applications. EAI Endorsed Transactions on Context-aware Systems and Applications, 2020, 7, 164497.	0.1	1
12	Hardware-assisted High-performance DNA Alignment System. , 2020, , .		0
13	Design Framework for FPGA-based Hardware Accelerators with Heterogeneous Interconnect. , 2019, , .		0
14	High-Throughput Machine Learning Approaches for Network Attacks Detection on FPGA. Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering, 2019, , 47-60.	0.2	5
15	HPOFS: A High Performance and Secured OpenFlow Switch Architecture for FPGA. Advances in Electrical and Computer Engineering, 2019, 19, 19-28.	0.5	2
16	IoT-Based Air-Pollution Hazard Maps Systems for Ho Chi Minh City. Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering, 2019, , 61-73.	0.2	1
17	An Efficient High-Throughput and Low-Latency SYN Flood Defender for High-Speed Networks. Security and Communication Networks, 2018, 2018, 1-14.	1.0	2
18	An FPGA-Based Seed Extension IP Core for BWA-MEM DNA Alignment. , 2018, , .		5

#	Article	IF	Citations
19	FPGA-based Multicore Architecture for Integrating Multiple DDoS Defense Mechanisms. Computer Architecture News, 2017, 44, 14-19.	2.5	7
20	Adaptable VLIW processor: The reconfigurable technology approach. , 2017, , .		1
21	An efficient runtime adaptable floating-point Gaussian filtering core. , 2017, , .		1
22	BKVex: An Adaptable VLIW Processor and Design Framework for Reconfigurable Computing Platforms. , 2017, , .		0
23	A Scalable FPGA-based Floating-Point Gaussian Filtering Architecture. , 2017, , .		2
24	A Secured OpenFlow-Based Switch Architecture. , 2016, , .		1
25	A reconfigurable heterogeneous multicore architecture for DDoS protection. , 2016, , .		0
26	Heterogeneous Hardware Accelerators with Hybrid Interconnect: An Automated Design Approach. , 2015, , .		1
27	Automated Hybrid Interconnect Design for FPGA Accelerators Using Data Communication Profiling. , 2014, , .		1
28	Heterogeneous hardware accelerators interconnect: An overview. , 2013, , .		7
29	Hybrid Interconnect Design for Heterogeneous Hardware Accelerators. , 2013, , .		7
30	Heterogeneous hardware accelerator architecture for streaming image processing. , 2013, , .		1
31	A heuristic-based communication-aware hardware optimization approach in heterogeneous multicore systems. , 2012, , .		5
32	Automatic generation of area constraints for FPGA implementation. , 2011, , .		1
33	Hazard-free Muller Gates for Implementing Asynchronous Circuits on Xilinx FPGA. , 2010, , .		10
34	New approaches to design asynchronous circuits on FPGAs. , 2009, , .		8