Jie Gu

List of Publications by Year
in descending order

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30 papers	226 citations	1163117 8 h-index	1125743 13 g-index
30 all docs	30 docs citations	30 times ranked	210 citing authors

#	Article	IF	Citations
1	A Dynamic Timing Enhanced DNN Accelerator With Compute-Adaptive Elastic Clock Chain Technique. IEEE Journal of Solid-State Circuits, 2021, 56, 55-65.	5.4	9
2	High-Throughput Dynamic Time Warping Accelerator for Time-Series Classification With Pipelined Mixed-Signal Time-Domain Computing. IEEE Journal of Solid-State Circuits, 2021, 56, 624-635.	5.4	14
3	A Gesture Classification SoC for Rehabilitation With ADC-Less Mixed-Signal Feature Extraction and Training Capable Neural Network Classifier. IEEE Journal of Solid-State Circuits, 2021, 56, 876-886.	5.4	3
4	Visualizing Thermally Activated Memristive Switching in Percolating Networks of Solutionâ€Processed 2D Semiconductors. Advanced Functional Materials, 2021, 31, 2107385.	14.9	17
5	An Adaptive Clock Scheme Exploiting Instruction-Based Dynamic Timing Slack for a GPGPU Architecture. IEEE Journal of Solid-State Circuits, 2020, 55, 2259-2269.	5.4	5
6	31.3 A Compute-Adaptive Elastic Clock-Chain Technique with Dynamic Timing Enhancement for 2D PE-Array-Based Accelerators. , 2020, , .		8
7	A Fully-integrated Gesture and Gait Processing SoC for Rehabilitation with ADC-less Mixed-signal Feature Extraction and Deep Neural Network for Classification and Online Training. , 2020, , .		3
8	R-Accelerator: An RRAM-Based CGRA Accelerator With Logic Contraction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2655-2667.	3.1	4
9	Digital Compatible Synthesis, Placement and Implementation of Mixed-Signal Time-Domain Computing. , 2019, , .		5
10	An Instruction-Driven Adaptive Clock Management Through Dynamic Phase Scaling and Compiler Assistance for a Low Power Microprocessor. IEEE Journal of Solid-State Circuits, 2019, 54, 2327-2338.	5.4	10
11	19.4 An Adaptive Clock Management Scheme Exploiting Instruction-Based Dynamic Timing Slack for a General-Purpose Graphics Processor Unit with Deep Pipeline and Out-of-Order Execution. , 2019, , .		10
12	19.7 A Scalable Pipelined Time-Domain DTW Engine for Time-Series Classification Using Multibit Time Flip-Flops With 140Giga-Cell-Updates/s Throughput. , 2019, , .		7
13	A Time-Domain Computing Accelerated Image Recognition Processor With Efficient Time Encoding and Non-Linear Logic Operation. IEEE Journal of Solid-State Circuits, 2019, 54, 3226-3237.	5.4	13
14	Design and optimization of edge computing distributed neural processor for biomedical rehabilitation with sensor fusion. , 2018, , .		7
15	Holistic Energy Management with Î¼Processor Co-Optimization in Fully Integrated Battery-Less IoTs. , 2018, , .		1
16	R-Accelerator: A Reconfigurable Accelerator with RRAM Based Logic Contraction and Resource Optimization for Application Specific Computing. , 2018, , .		1
17	A Fully-integrated LC-Oscillator Based Buck Regulator with Autonomous Resonant Switching for Low-Power Applications. , 2018, , .		0
18	An Image Recognition Processor with Time-domain Accelerators using Efficient Time Encoding and Non-linear Logic Operation. , 2018, , .		4

#	Article	IF	Citations
19	Compiler-guided instruction-level clock scheduling for timing speculative processors. , 2018, , .		1
20	An Instruction Driven Adaptive Clock Phase Scaling with Timing Encoding and Online Instruction Calibration for a Low Power Microprocessor. , 2018, , .		4
21	Design and Synthesis of Self-Healing Memristive Circuits for Timing Resilient Processor Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2648-2660.	3.1	1
22	A Comprehensive Stochastic Design Methodology for Hold-Timing Resiliency in Voltage-Scalable Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2118-2131.	3.1	4
23	A Fully Integrated Buck Regulator With 2-GHz Resonant Switching for Low-Power Applications. IEEE Journal of Solid-State Circuits, 2018, 53, 2663-2674.	5.4	13
24	Greybox Design Methodology. , 2017, , .		8
25	Cell-to-array thermal-aware analysis of stacked RRAM. , 2017, , .		0
26	(Invited) Software-guided greybox design methodology with integrated power and clock management. , 2017, , .		0
27	Comprehensive Analysis, Modeling and Design for Hold-Timing Resiliency in Voltage Scalable Design. , 2016, , .		1
28	Analysis and Design of Energy Efficient Time Domain Signal Processing. , 2016, , .		10
29	The Effect of Random Dopant Fluctuations on Logic Timing at Low Voltage. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 911-924.	3.1	26
30	A 28 nm 0.6 V Low Power DSP for Mobile Applications. IEEE Journal of Solid-State Circuits, 2012, 47, 35-46.	5.4	37