# Jason Cong

## List of Publications by Year in Descending Order



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|---|---|---|---|
| 105 papers | 3,272 citations | 23 h-index | 55 g-index |
| 112 ext. papers | 4,509 ext. citations | 3.8 avg, IF | 5.62 L-index |

| # | Paper | IF | Citations |
|---|---|---|---|
| 105 | AutoDSE: Enabling Software Programmers to Design Efficient FPGA Accelerators. *ACM Transactions on Design Automation of Electronic Systems*, **2022**, 27, 1-27 | 1.5 | 3 |
| 104 | Extending High-Level Synthesis for Task-Parallel Programs **2021**, 2021, | | 4 |
| 103 | Optimality Study of Existing Quantum Computing Layout Synthesis Tools. *IEEE Transactions on Computers*, **2021**, 70, 1363-1373 | 2.5 | 11 |
| 102 | HBM Connect: High-Performance HLS Interconnect for FPGA HBM **2021**, 2021, 116-126 | | 9 |
| 101 | Crane: Mitigating Accelerator Under-utilization Caused by Sparsity Irregularities in CNNs. *IEEE Transactions on Computers*, **2020**, 69, 931-943 | 2.5 | 3 |
| 100 | . *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 4828-4841 | 2.5 | 3 |
| 99 | SACNN: Self-Attention Convolutional Neural Network for Low-Dose CT Denoising With Self-Supervised Perceptual Loss Network. *IEEE Transactions on Medical Imaging*, **2020**, 39, 2289-2301 | 11.7 | 62 |
| 98 | Optimal layout synthesis for quantum computing **2020**, | | 9 |
| 97 | BLINK **2020**, | | 4 |
| 96 | Bonsai: High-Performance Adaptive Merge Tree Sorting **2020**, | | 9 |
| 95 | Frequency Improvement of Systolic Array-Based CNNs on FPGAs **2019**, | | 8 |
| 94 | Overcoming Data Transfer Bottlenecks in FPGA-based DNN Accelerators via Layer Conscious Memory Management **2019**, | | 18 |
| 93 | HeteroCL **2019**, | | 24 |
| 92 | Rapid Cycle-Accurate Simulator for High-Level Synthesis **2019**, | | 4 |
| 91 | LANMC **2019**, | | 3 |
| 90 | A Millimeter-Wave CMOS Transceiver With Digitally Pre-Distorted PAM-4 Modulation for Contactless Communications. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 1600-1612 | 5.5 | 6 |
| 89 | Hardware Acceleration of Long Read Pairwise Overlapping in Genome Sequencing: A Race Between FPGA and GPU **2019**, | | 12 |

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| 88 | Dataflow Systolic Array Implementations of Matrix Decomposition Using High Level Synthesis **2019** , | | 3 |
| 87 | RC-NVM: Dual-Addressing Non-Volatile Memory Architecture Supporting Both Row and Column Memory Accesses. *IEEE Transactions on Computers*, **2019**, 68, 239-254 | 2.5 | 5 |
| 86 | . *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 2072-2085 | 2.5 | 84 |
| 85 | . *Proceedings of the IEEE*, **2019**, 107, 185-203 | 14.3 | 2 |
| 84 | Scaling for edge inference of deep neural networks. *Nature Electronics*, **2018**, 1, 216-222 | 28.4 | 149 |
| 83 | SODA **2018**, | | 29 |
| 82 | PolySA **2018**, | | 26 |
| 81 | Computed Tomography Image Enhancement Using 3D Convolutional Neural Network. *Lecture Notes in Computer Science*, **2018**, 291-299 | 0.9 | 6 |
| 80 | Automatic Interior I/O Elimination in Systolic Array Architecture **2018**, | | 1 |
| 79 | S2FA **2018**, | | 12 |
| 78 | Throughput optimization for streaming applications on CPU-FPGA heterogeneous systems **2017**, | | 6 |
| 77 | FPGA-based accelerator for long short-term memory recurrent neural networks **2017**, | | 77 |
| 76 | Automated Systolic Array Architecture Synthesis for High Throughput CNN Inference on FPGAs **2017**, | | 153 |
| 75 | HLScope: High-Level Performance Debugging for FPGA Designs **2017**, | | 10 |
| 74 | HLScope+,: Fast and accurate performance estimation for FPGA HLS **2017**, | | 12 |
| 73 | Energy-Efficient CNN Implementation on a Deeply Pipelined FPGA Cluster **2016**, | | 96 |
| 72 | Software Infrastructure for Enabling FPGA-Based Accelerations in Data Centers **2016**, | | 10 |
| 71 | A quantitative analysis on microarchitectures of modern CPU-FPGA platforms **2016**, | | 51 |

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| 70 | ARACompiler: a prototyping flow and evaluation framework for accelerator-rich architectures **2015** , | | 4 |
| 69 | A Novel High-Throughput Acceleration Engine for Read Alignment **2015**, | | 22 |
| 68 | Optimizing FPGA-based Accelerator Design for Deep Convolutional Neural Networks **2015**, | | 829 |
| 67 | Impact of loop transformations on software reliability **2015**, | | 3 |
| 66 | An automated lung segmentation approach using bidirectional chain codes to improve nodule detection accuracy. *Computers in Biology and Medicine*, **2015**, 57, 139-49 | 7 | 67 |
| 65 | Accelerator-Rich Architectures Computing Beyond Processors **2015**, 1-17 | | |
| 64 | Better-Than-Worst-Case Design: Progress and Opportunities. *Journal of Computer Science and Technology*, **2014**, 29, 656-663 | 1.7 | 1 |
| 63 | FPGA Implementation of EM Algorithm for 3D CT Reconstruction **2014**, | | 5 |
| 62 | A Fully Pipelined and Dynamically Composable Architecture of CGRA **2014**, | | 27 |
| 61 | A scalable, high-performance customized priority queue **2014**, | | 8 |
| 60 | FPGA Simulation Engine for Customized Construction of Neural Microcircuits **2013**, 2013, 229 | | 2 |
| 59 | FPGA simulation engine for customized construction of neural microcircuits **2013**, | | 2 |
| 58 | Energy-efficient computing using adaptive table lookup based on nonvolatile memories **2013**, | | 11 |
| 57 | Accelerator-rich CMPs: From concept to real hardware **2013**, | | 21 |
| 56 | An Analytical Placement Framework for 3-D ICs and Its Extension on Thermal Awareness. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 510-523 | 2.5 | 30 |
| 55 | Composable accelerator-rich microprocessor enhanced for adaptivity and longevity **2013**, | | 15 |
| 54 | Improving high level synthesis optimization opportunity through polyhedral transformations **2013**, | | 38 |
| 53 | Utilizing Radio-Frequency Interconnect for a Many-DIMM DRAM System. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2012**, 2, 210-227 | 5.2 | 8 |

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| 52 | An integrated and automated memory optimization flow for FPGA behavioral synthesis **2012**, | | 9 |
| 51 | Compilation and architecture support for customized vector instruction extension **2012**, | | 2 |
| 50 | A Hybrid Architecture for Compressive Sensing 3-D CT Reconstruction. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2012**, 2, 616-625 | 5.2 | 12 |
| 49 | Task-Level Data Model for Hardware Synthesis Based on Concurrent Collections. *Journal of Electrical and Computer Engineering*, **2012**, 2012, 1-24 | 1.9 | 0 |
| 48 | Combining module selection and replication for throughput-driven streaming programs **2012**, | | 11 |
| 47 | Platform characterization for Domain-Specific Computing **2012**, | | 12 |
| 46 | mrFPGA: A novel FPGA architecture with memristor-based reconfiguration **2011**, | | 88 |
| 45 | EM+TV Based Reconstruction for Cone-Beam CT with Reduced Radiation. *Lecture Notes in Computer Science*, **2011**, 1-10 | 0.9 | 11 |
| 44 | Combined loop transformation and hierarchy allocation for data reuse optimization **2011**, | | 10 |
| 43 | An 8M Polygons/s 3-D Graphics SoC With Full Hardware Geometric and Rendering Engine for Mobile Applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1490-1495 | 2.6 | 2 |
| 42 | High-Level Synthesis for FPGAs: From Prototyping to Deployment. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 473-491 | 2.5 | 405 |
| 41 | Pattern-Mining for Behavioral Synthesis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 939-944 | 2.5 | 2 |
| 40 | ATree-based topology synthesis for on-chip network **2011**, | | 5 |
| 39 | An energy-efficient adaptive hybrid cache **2011**, | | 21 |
| 38 | Accelerating vision and navigation applications on a customizable platform **2011**, | | 6 |
| 37 | Multilevel Granularity Parallelism Synthesis on FPGAs **2011**, | | 24 |
| 36 | Domain-specific processor with 3D integration for medical image processing **2011**, | | 8 |
| 35 | 3D recursive Gaussian IIR on GPU and FPGAs □A case for accelerating bandwidth-bounded applications **2011**, | | 4 |

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| 34 | Assuring application-level correctness against soft errors **2011**, | | 17 |
| 33 | Rethinking thermal via planning with timing-power-temperature dependence for 3D ICs **2011**, | | 4 |
| 32 | A unified optimization framework for simultaneous gate sizing and placement under density constraints **2011**, | | 2 |
| 31 | Accelerating Fluid Registration Algorithm on Multi-FPGA Platforms **2011**, | | 12 |
| 30 | The DIMM tree architecture: A high bandwidth and scalable memory system **2011**, | | 12 |
| 29 | Logic-on-logic 3D integration and placement **2010**, | | 11 |
| 28 | Evaluating Statistical Power Optimization. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 1750-1762 | 2.5 | 3 |
| 27 | Technology Mapping and Clustering for FPGA Architectures With Dual Supply Voltages. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 1709-1722 | 2.5 | 6 |
| 26 | A Comparative Study on the Architecture Templates for Dynamic Nested Loops **2010**, | | 2 |
| 25 | A 3D physical design flow based on Open Access **2009**, | | 7 |
| 24 | Logic synthesis for better than worst-case designs **2009**, | | 12 |
| 23 | Synthesis Algorithm for Application-Specific Homogeneous Processor Networks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 1318-1329 | 2.6 | 7 |
| 22 | Energy efficient multiprocessor task scheduling under input-dependent variation **2009**, | | 20 |
| 21 | On the futility of statistical power optimization **2009**, | | 1 |
| 20 | FCUDA: Enabling efficient compilation of CUDA kernels onto FPGAs **2009**, | | 83 |
| 19 | Evaluation of Static Analysis Techniques for Fixed-Point Precision Optimization **2009**, | | 15 |
| 18 | Highly Efficient Gradient Computation for Density-Constrained Analytical Placement. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2008**, 27, 2133-2144 | 2.5 | 12 |
| 17 | Behavioral synthesis with activating unused flip-flops for reducing glitch power in FPGA **2008**, | | 2 |

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| 16 | Scheduling with integer time budgeting for low-power optimization **2008**, | | 5 |
| 15 | MC-Sim: An efficient simulation tool for MPSoC designs **2008**, | | 14 |
| 14 | Fine grain 3D integration for microarchitecture design through cube packing exploration **2007**, | | 14 |
| 13 | Routability-driven placement and white space allocation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 858-871 | 2.5 | 5 |
| 12 | Optimality Study of Logic Synthesis for LUT-Based FPGAs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 230-239 | 2.5 | 34 |
| 11 | Thermal-Aware 3D IC Placement Via Transformation **2007**, | | 80 |
| 10 | High-Level Power Estimation and Low-Power Design Space Exploration for FPGAs **2007**, | | 29 |
| 9 | Platform-Based Resource Binding Using a Distributed Register-File Microarchitecture. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2006**, | | 7 |
| 8 | Architecture and Compiler Optimizations for Data Bandwidth Improvement in Configurable Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2006**, 14, 986-997 | 2.6 | 6 |
| 7 | Protecting Combinational Logic Synthesis Solutions. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2006**, 25, 2687-2696 | 2.5 | 22 |
| 6 | Large-scale circuit placement: gap and promise **2003**, | | 2 |
| 5 | Wire width planning for interconnect performance optimization. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2002**, 21, 319-329 | 2.5 | 14 |
| 4 | Via design rule consideration in multilayer maze routing algorithms. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2000**, 19, 215-223 | 2.5 | 9 |
| 3 | Channel Density Minimization by Pin Permutation. *VLSI Design*, **1994**, 2, 171-183 | | |
| 2 | Architectural synthesis Integrated with global placement for multi-cycle communication | | 2 |
| 1 | An efficient approach to simultaneous transistor and interconnect sizing | | 11 |