

Jason Cong

List of Publications by Citations

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

105
papers

3,272
citations

23
h-index

55
g-index

112
ext. papers

4,509
ext. citations

3.8
avg. IF

5.62
L-index

#	Paper	IF	Citations
105	Optimizing FPGA-based Accelerator Design for Deep Convolutional Neural Networks 2015 ,		829
104	High-Level Synthesis for FPGAs: From Prototyping to Deployment. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2011 , 30, 473-491	2.5	405
103	Automated Systolic Array Architecture Synthesis for High Throughput CNN Inference on FPGAs 2017 ,		153
102	Scaling for edge inference of deep neural networks. <i>Nature Electronics</i> , 2018 , 1, 216-222	28.4	149
101	Energy-Efficient CNN Implementation on a Deeply Pipelined FPGA Cluster 2016 ,		96
100	mrFPGA: A novel FPGA architecture with memristor-based reconfiguration 2011 ,		88
99	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2019 , 38, 2072-2085	2.5	84
98	FCUDA: Enabling efficient compilation of CUDA kernels onto FPGAs 2009 ,		83
97	Thermal-Aware 3D IC Placement Via Transformation 2007 ,		80
96	FPGA-based accelerator for long short-term memory recurrent neural networks 2017 ,		77
95	An automated lung segmentation approach using bidirectional chain codes to improve nodule detection accuracy. <i>Computers in Biology and Medicine</i> , 2015 , 57, 139-49	7	67
94	SACNN: Self-Attention Convolutional Neural Network for Low-Dose CT Denoising With Self-Supervised Perceptual Loss Network. <i>IEEE Transactions on Medical Imaging</i> , 2020 , 39, 2289-2301	11.7	62
93	A quantitative analysis on microarchitectures of modern CPU-FPGA platforms 2016 ,		51
92	Improving high level synthesis optimization opportunity through polyhedral transformations 2013 ,		38
91	Optimality Study of Logic Synthesis for LUT-Based FPGAs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2007 , 26, 230-239	2.5	34
90	An Analytical Placement Framework for 3-D ICs and Its Extension on Thermal Awareness. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2013 , 32, 510-523	2.5	30
89	High-Level Power Estimation and Low-Power Design Space Exploration for FPGAs 2007 ,		29

88	SODA 2018 ,		29
87	A Fully Pipelined and Dynamically Composable Architecture of CGRA 2014 ,		27
86	PolySA 2018 ,		26
85	HeteroCL 2019 ,		24
84	Multilevel Granularity Parallelism Synthesis on FPGAs 2011 ,		24
83	A Novel High-Throughput Acceleration Engine for Read Alignment 2015 ,		22
82	Protecting Combinational Logic Synthesis Solutions. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2006 , 25, 2687-2696	2.5	22
81	Accelerator-rich CMPs: From concept to real hardware 2013 ,		21
80	An energy-efficient adaptive hybrid cache 2011 ,		21
79	Energy efficient multiprocessor task scheduling under input-dependent variation 2009 ,		20
78	Overcoming Data Transfer Bottlenecks in FPGA-based DNN Accelerators via Layer Conscious Memory Management 2019 ,		18
77	Assuring application-level correctness against soft errors 2011 ,		17
76	Composable accelerator-rich microprocessor enhanced for adaptivity and longevity 2013 ,		15
75	Evaluation of Static Analysis Techniques for Fixed-Point Precision Optimization 2009 ,		15
74	MC-Sim: An efficient simulation tool for MPSoC designs 2008 ,		14
73	Fine grain 3D integration for microarchitecture design through cube packing exploration 2007 ,		14
72	Wire width planning for interconnect performance optimization. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2002 , 21, 319-329	2.5	14
71	Hardware Acceleration of Long Read Pairwise Overlapping in Genome Sequencing: A Race Between FPGA and GPU 2019 ,		12

70	HLScope+,: Fast and accurate performance estimation for FPGA HLS 2017 ,		12
69	A Hybrid Architecture for Compressive Sensing 3-D CT Reconstruction. <i>IEEE Journal on Emerging and Selected Topics in Circuits and Systems</i> , 2012 , 2, 616-625	5.2	12
68	Logic synthesis for better than worst-case designs 2009 ,		12
67	Accelerating Fluid Registration Algorithm on Multi-FPGA Platforms 2011 ,		12
66	The DIMM tree architecture: A high bandwidth and scalable memory system 2011 ,		12
65	Platform characterization for Domain-Specific Computing 2012 ,		12
64	Highly Efficient Gradient Computation for Density-Constrained Analytical Placement. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2008 , 27, 2133-2144	2.5	12
63	S2FA 2018 ,		12
62	Energy-efficient computing using adaptive table lookup based on nonvolatile memories 2013 ,		11
61	EM+TV Based Reconstruction for Cone-Beam CT with Reduced Radiation. <i>Lecture Notes in Computer Science</i> , 2011 , 1-10	0.9	11
60	Logic-on-logic 3D integration and placement 2010 ,		11
59	Combining module selection and replication for throughput-driven streaming programs 2012 ,		11
58	An efficient approach to simultaneous transistor and interconnect sizing		11
57	Optimality Study of Existing Quantum Computing Layout Synthesis Tools. <i>IEEE Transactions on Computers</i> , 2021 , 70, 1363-1373	2.5	11
56	Software Infrastructure for Enabling FPGA-Based Accelerations in Data Centers 2016 ,		10
55	HLScope: High-Level Performance Debugging for FPGA Designs 2017 ,		10
54	Combined loop transformation and hierarchy allocation for data reuse optimization 2011 ,		10
53	An integrated and automated memory optimization flow for FPGA behavioral synthesis 2012 ,		9

52	Via design rule consideration in multilayer maze routing algorithms. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2000 , 19, 215-223	2.5	9
51	Optimal layout synthesis for quantum computing 2020 ,		9
50	Bonsai: High-Performance Adaptive Merge Tree Sorting 2020 ,		9
49	HBM Connect: High-Performance HLS Interconnect for FPGA HBM 2021 , 2021, 116-126		9
48	Frequency Improvement of Systolic Array-Based CNNs on FPGAs 2019 ,		8
47	A scalable, high-performance customized priority queue 2014 ,		8
46	Utilizing Radio-Frequency Interconnect for a Many-DIMM DRAM System. <i>IEEE Journal on Emerging and Selected Topics in Circuits and Systems</i> , 2012 , 2, 210-227	5.2	8
45	Domain-specific processor with 3D integration for medical image processing 2011 ,		8
44	A 3D physical design flow based on Open Access 2009 ,		7
43	Synthesis Algorithm for Application-Specific Homogeneous Processor Networks. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2009 , 17, 1318-1329	2.6	7
42	Platform-Based Resource Binding Using a Distributed Register-File Microarchitecture. <i>IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers</i> , 2006 ,		7
41	Throughput optimization for streaming applications on CPU-FPGA heterogeneous systems 2017 ,		6
40	A Millimeter-Wave CMOS Transceiver With Digitally Pre-Distorted PAM-4 Modulation for Contactless Communications. <i>IEEE Journal of Solid-State Circuits</i> , 2019 , 54, 1600-1612	5.5	6
39	Technology Mapping and Clustering for FPGA Architectures With Dual Supply Voltages. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2010 , 29, 1709-1722	2.5	6
38	Accelerating vision and navigation applications on a customizable platform 2011 ,		6
37	Architecture and Compiler Optimizations for Data Bandwidth Improvement in Configurable Processors. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2006 , 14, 986-997	2.6	6
36	Computed Tomography Image Enhancement Using 3D Convolutional Neural Network. <i>Lecture Notes in Computer Science</i> , 2018 , 291-299	0.9	6
35	FPGA Implementation of EM Algorithm for 3D CT Reconstruction 2014 ,		5

34	A-Tree-based topology synthesis for on-chip network 2011 ,		5
33	Scheduling with integer time budgeting for low-power optimization 2008 ,		5
32	Routability-driven placement and white space allocation. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2007 , 26, 858-871	2.5	5
31	RC-NVM: Dual-Addressing Non-Volatile Memory Architecture Supporting Both Row and Column Memory Accesses. <i>IEEE Transactions on Computers</i> , 2019 , 68, 239-254	2.5	5
30	Rapid Cycle-Accurate Simulator for High-Level Synthesis 2019 ,		4
29	ARACompiler: a prototyping flow and evaluation framework for accelerator-rich architectures 2015 ,		4
28	3D recursive Gaussian IIR on GPU and FPGAs: A case for accelerating bandwidth-bounded applications 2011 ,		4
27	Rethinking thermal via planning with timing-power-temperature dependence for 3D ICs 2011 ,		4
26	BLINK 2020 ,		4
25	Extending High-Level Synthesis for Task-Parallel Programs 2021 , 2021,		4
24	LANMC 2019 ,		3
23	Crane: Mitigating Accelerator Under-utilization Caused by Sparsity Irregularities in CNNs. <i>IEEE Transactions on Computers</i> , 2020 , 69, 931-943	2.5	3
22	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2020 , 39, 4828-4841	2.5	3
21	Impact of loop transformations on software reliability 2015 ,		3
20	Evaluating Statistical Power Optimization. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2010 , 29, 1750-1762	2.5	3
19	AutoDSE: Enabling Software Programmers to Design Efficient FPGA Accelerators. <i>ACM Transactions on Design Automation of Electronic Systems</i> , 2022 , 27, 1-27	1.5	3
18	Dataflow Systolic Array Implementations of Matrix Decomposition Using High Level Synthesis 2019 ,		3
17	FPGA Simulation Engine for Customized Construction of Neural Microcircuits 2013 , 2013, 229		2

16	FPGA simulation engine for customized construction of neural microcircuits 2013 ,		2
15	Compilation and architecture support for customized vector instruction extension 2012 ,		2
14	An 8M Polygons/s 3-D Graphics SoC With Full Hardware Geometric and Rendering Engine for Mobile Applications. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2011 , 19, 1490-1495 ^{2.6}		2
13	Pattern-Mining for Behavioral Synthesis. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2011 , 30, 939-944	2.5	2
12	A Comparative Study on the Architecture Templates for Dynamic Nested Loops 2010 ,		2
11	A unified optimization framework for simultaneous gate sizing and placement under density constraints 2011 ,		2
10	Behavioral synthesis with activating unused flip-flops for reducing glitch power in FPGA 2008 ,		2
9	Large-scale circuit placement: gap and promise 2003 ,		2
8	Architectural synthesis Integrated with global placement for multi-cycle communication		2
7	. <i>Proceedings of the IEEE</i> , 2019 , 107, 185-203	14.3	2
6	Better-Than-Worst-Case Design: Progress and Opportunities. <i>Journal of Computer Science and Technology</i> , 2014 , 29, 656-663	1.7	1
5	On the futility of statistical power optimization 2009 ,		1
4	Automatic Interior I/O Elimination in Systolic Array Architecture 2018 ,		1
3	Task-Level Data Model for Hardware Synthesis Based on Concurrent Collections. <i>Journal of Electrical and Computer Engineering</i> , 2012 , 2012, 1-24	1.9	0
2	Channel Density Minimization by Pin Permutation. <i>VLSI Design</i> , 1994 , 2, 171-183		
1	Accelerator-Rich Architectures [Computing Beyond Processors 2015 , 1-17		