Rui Martins

List of Publications by Year
in descending order

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444	7,586	71061	114418
papers	citations	41 h-index	63 g-index

455	455	455	4448
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Constant-Frequency and Noncommunication-Based Inductive Power Transfer Converter for Battery Charging. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2022, 10, 2147-2162.	3.7	20
2	Mismatch Analysis of DTCs With an Improved BIST-TDC in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 196-206.	3.5	4
3	Switched-Capacitor Bandgap Voltage Reference for IoT Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 16-29.	3.5	10
4	A Low-Power Multiband Blocker-Tolerant Receiver With a Steep Filtering Slope Using an N-Path LNA With Feedforward OB Blocker Cancellation and Filtering-by-Aliasing Baseband Amplifiers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 220-231.	3.5	5
5	A Single-Opamp Third Order CT Î”Î£ Modulator With SAB-ELD-Merged Integrator and Three-Stage Hybrid Compensation Opamp. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 64-74.	3.5	5
6	An Inherent Gain Error Tolerance Noise-Shaping SAR-Assisted Pipeline ADC With Code-Counter-Based Offset Calibration. IEEE Journal of Solid-State Circuits, 2022, 57, 1480-1491.	3.5	4
7	A 0.0285-mm² 0.68-pJ/bit Single-Loop Full-Rate Bang-Bang CDR Without Reference and Separate FD Pulling Off an 8.2-Gb/s/Î¼s Acquisition Speed of the PAM-4 Input in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2022, 57, 546-561.	3.5	9
8	A 529-Î¼W Fractional-N All-Digital PLL Using TDC Gain Auto-Calibration and an Inverse-Class-F DCO in 65-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 51-63.	3.5	13
9	A 3.3-GS/s 6-b Fully Dynamic Pipelined ADC With Linearized Dynamic Amplifier. IEEE Journal of Solid-State Circuits, 2022, 57, 1673-1683.	3.5	8
10	A Millimeter-Wave CMOS VCO Featuring a Mode-Ambiguity-Aware Multi-Resonant-RLCM Tank. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 172-185.	3.5	18
11	A 4T/Cell Amplifier-Chain-Based XOR PUF With Strong Machine Learning Attack Resilience. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 366-377.	3.5	15
12	A Scalable High-Current High-Accuracy Dual-Loop Four-Phase Switching LDO for Microprocessors. IEEE Journal of Solid-State Circuits, 2022, 57, 1841-1853.	3.5	8
13	A 3.3-GHz Integer N-Type-II Sub-Sampling PLL Using a BFSK-Suppressed Pushâ€“Pull SS-PD and a Fast-Locking FLL Achieving â^'82.2-dBc REF Spur and â^'255-dB FOM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 238-242.	2.1	17
14	RF Rectifiers With Wide Incident Angle of Incoming Waves Based on Rat-Race Couplers. IEEE Transactions on Microwave Theory and Techniques, 2022, 70, 1983-1993.	2.9	5
15	A 20 MHz Bandwidth 79 dB SNDR SAR-Assisted Noise-Shaping Pipeline ADC With Gain and Offset Calibrations. IEEE Journal of Solid-State Circuits, 2022, 57, 745-756.	3.5	7
16	A Sub-0.25-pJ/bit 47.6-to-58.8-Gb/s Reference-Less FD-Less Single-Loop PAM-4 Bang-Bang CDR With a Deliberate-Current-Mismatch Frequency Acquisition Technique in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2022, 57, 1358-1371.	3.5	8
17	A 0.15-V, 44.73% PCE charge pump with CMOS differential ring-VCO for energy harvesting systems. Analog Integrated Circuits and Signal Processing, 2022, 111, 35-43.	0.9	6
18	One-shot high-resolution melting curve analysis for KRAS point-mutation discrimination on a digital microfluidics platform. Lab on A Chip, 2022, 22, 537-549.	3.1	11

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19	A 1.7â€“3.6 GHz 20 MHz-Bandwidth Channel-Selection N-Path Passive-LNA Using a Switched-Capacitor-Transformer Network Achieving 23.5 dBm OB-IIPâ,ƒ and 3.4â€“4.8 dB NF. IEEE Journal of Solid-State Circuits, 2022, 57, 413-422.	3.5	9
20	A Swing-Enhanced Class-D VCO Using a Periodically Time-Varying (PTV) Inductor. IEEE Solid-State Circuits Letters, 2022, 5, 25-28.	1.3	3
21	Background Timing Mismatch Calibration Techniques in High-Speed Time-Interleaved ADCs: A Tutorial Review. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2564-2569.	2.2	0
22	A Reconfigurable Single-Stage Asymmetrical Full-Wave Step-Down Rectifier for Bidirectional Device-to-Device Wireless Fast Charging. IEEE Journal of Solid-State Circuits, 2022, 57, 1888-1898.	3.5	2
23	Wideband Continuous-Time MASH Delta-Sigma Modulators: A Tutorial Review. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2623-2628.	2.2	7
24	A 4A 12-to-1 Flying Capacitor Cross-Connected DC-DC Converter with Inserted D>0.5 Control Achieving >2x Transient Inductor Current Slew Rate and 0.73Ã— Theoretical Minimum Output Undershoot of DSD. , 2022, , .		10
25	Miniaturized Energy Harvesting Systems Using Switched-Capacitor DC-DC Converters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2629-2634.	2.2	7
26	Arithmetic Progression Switched-Capacitor DCâ€“DC Converter Topology With Soft VCR Transitions and Quasi-Symmetric Two-Phase Charge Delivery. IEEE Journal of Solid-State Circuits, 2022, 57, 2919-2933.	3.5	5
27	All Rivers Flow to the Sea: A High Power Density Wireless Power Receiver with Split-Dual-Path Rectification and Hybrid-Quad-Path Step-Down Conversion. , 2022, , .		0
28	A 0.1-V V_{IN} Subthreshold 3-Stage Dual-Branch Charge Pump With 43.4% Peak Power Conversion Efficiency Using Advanced Dynamic Gate-Bias. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3929-3933.	2.2	9
29	An FPGA-Based Energy-Efficient Reconfigurable Depthwise Separable Convolution Accelerator for Image Recognition. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 4003-4007.	2.2	7
30	A Multimode CMOS Vision Sensor With On-Chip Motion Direction Detection and Simultaneous Energy Harvesting Capabilities. IEEE Sensors Journal, 2022, 22, 12808-12819.	2.4	4
31	A Highly Integrated Tri-Path Hybrid Buck Converter With Reduced Inductor Current and Self-Balanced Flying Capacitor Voltage. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 3841-3850.	3.5	7
32	High-Performance Harmonic-Rich Single-Core VCO With Multi-LC Tank: A Tutorial. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3115-3121.	2.2	21
33	Fully-Integrated Timers for Ultra-Low-Power Internet-of-Things Nodesâ€”Fundamentals and Design Techniques. IEEE Access, 2022, 10, 65936-65950.	2.6	6
34	A Fully-Integrated Ambient RF Energy Harvesting System with 423-Î¼W Output Power. Sensors, 2022, 22, 4415.	2.1	12
35	An Analog Multiplier Controlled Buck-Boost Converter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 4173-4177.	2.2	3
36	A Reconfigurable CMOS Rectifier With 14-dB Power Dynamic Range Achieving >36-dB/mm² FoM for RF-Based Hybrid Energy Harvesting. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1533-1537.	2.1	13

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37	A Capacitor-Cross-Connected Boost Converter With Duty Cycle < 0.5 Control for Extended Conversion-Ratio and Soft Start-Up. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 4272-4283.	3.5	0
38	An FPGA-Based Self-Reconfigurable Arc Fault Detection System for Smart Meters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 4133-4137.	2.2	2
39	A 0.14-to-0.29-pJ/bit 14-GBaud/s Trimodal (NRZ/PAM-4/PAM-8) Half-Rate Bang-Bang Clock and Data Recovery (BBCDR) Circuit in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 89-102.	3.5	19
40	Startup Time and Energy-Reduction Techniques for Crystal Oscillators in the IoT Era. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 30-35.	2.2	7
41	Review of Analog-Assisted-Digital and Digital-Assisted-Analog Low Dropout Regulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 24-29.	2.2	15
42	A Fully Integrated FVF LDO With Enhanced Full-Spectrum Power Supply Rejection. IEEE Transactions on Power Electronics, 2021, 36, 4326-4337.	5.4	48
43	A Wide-PCE-Dynamic-Range CMOS Cross-Coupled Differential-Drive Rectifier for Ambient RF Energy Harvesting. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1743-1747.	2.2	23
44	A High-Efficiency Dual-Antenna RF Energy Harvesting System Using Full-Energy Extraction With Improved Input Power Response. IEEE Open Journal of Circuits and Systems, 2021, 2, 436-444.	1.4	3
45	Wideband Variable-Gain Amplifiers Based on a Pseudo-Current-Steering Gain-Tuning Technique. IEEE Access, 2021, 9, 35814-35823.	2.6	4
46	20.1 A 5.0-to-6.36GHz Wideband-Harmonic-Shaping VCO Achieving 196.9dBc/Hz Peak FoM and 90-to-180kHz 1/f³ PN Corner Without Harmonic Tuning. , 2021, , .		20
47	A 7-bit 2 GS/s Time-Interleaved SAR ADC With Timing Skew Calibration Based on Current Integrating Sampler. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 557-568.	3.5	27
48	Bird'sâ€eye view of analog and mixedâ€signal chips for the 21st century. International Journal of Circuit Theory and Applications, 2021, 49, 746-761.	1.3	7
49	An 800 MHz-to-3.3 GHz 20-MHz Channel Bandwidth WPD CMOS Power Amplifier For Multiband Uplink Radio Transceivers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1178-1182.	2.2	4
50	Discrete-Time MASH Delta-Sigma Modulator with Second-Order Digital Noise Coupling for Wideband High-Resolution Applications. , 2021, , .		7
51	A 3.52-GHz Harmonic-Rich-Shaping VCO with Noise Suppression and Circulation, Achieving -151-dBc/Hz Phase Noise at 10-MHz Offset. , 2021, , .		12
52	A 3-Phase Resonant Switched-Capacitor Converter for Data Center 48-V Rack Power Distribution. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2714-2724.	3.5	18
53	A 0.003-mm² 440fs_{RMS}-Jitter and â^'64dBc-Reference-Spur Ring-VCO-Based Type-I PLL Using a Current-Reuse Sampling Phase Detector in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2307-2316.	3.5	12
54	A Sub-0.25pJ/bit 47.6-to-58.8Gb/s Reference-Less FD-Less Single-Loop PAM-4 Bang-Bang CDR with a Deliberately-Current-Mismatch Frequency Acquisition Technique in 28nm CMOS. , 2021, , .		8

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55	A 40-MHz Bandwidth 75-dB SNDR Partial-Interleaving SAR-Assisted Noise-Shaping Pipeline ADC. IEEE Journal of Solid-State Circuits, 2021, 56, 1772-1783.	3.5	10
56	A Highly Integrated 3-Phase 4:1 Resonant Switched-Capacitor Converter With Parasitic Loss Reduction and Fast Pre-Charge Startup. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2608-2612.	2.2	10
57	A Hybrid Boost Converter With Cross-Connected Flying Capacitors. IEEE Journal of Solid-State Circuits, 2021, 56, 2102-2112.	3.5	18
58	A Time-Interleaved 2nd-Order Î”Î£ Modulator Achieving 5-MHz Bandwidth and 86.1-dB SNDR Using Digital Feed-Forward Extrapolation. IEEE Journal of Solid-State Circuits, 2021, 56, 2375-2387.	3.5	9
59	A Fully Integrated 10-V Pulse Driver Using Multiband Pulse-Frequency Modulation in 65-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1665-1669.	2.1	0
60	A Single-Stage Dual-Output Regulating Rectifier With Hysteretic Current-Wave Modulation. IEEE Journal of Solid-State Circuits, 2021, 56, 2770-2780.	3.5	12
61	A Hybrid Single-Inductor Bipolar-Output DCâ€“DC Converter With Floating Negative Output for AMOLED Displays. IEEE Journal of Solid-State Circuits, 2021, 56, 2760-2769.	3.5	13
62	An FPGA-Based Energy-Efficient Reconfigurable Convolutional Neural Network Accelerator for Object Recognition Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3143-3147.	2.2	22
63	A 600-Î¼mÂ² Ring-VCO-Based Hybrid PLL Using a 30-Î¼W Charge-Sharing Integrator in 28-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3108-3112.	2.2	6
64	A 0.35-V 5,200-Î¼m² 2.1-MHz Temperature-Resilient Relaxation Oscillator With 667 fJ/Cycle Energy Efficiency Using an Asymmetric Swing-Boosted RC Network and a Dual-Path Comparator. IEEE Journal of Solid-State Circuits, 2021, 56, 2701-2710.	3.5	22
65	A 2.4-GHz CMOS Differential Class-DE Rectifier With Coupled Inductors. IEEE Transactions on Power Electronics, 2021, 36, 9864-9875.	5.4	4
66	A 3.36-GHz Locking-Tuned Type-I Sampling PLL With â¯78.6-dBc Reference Spur Merging Single-Path Reference-Feedthrough-Suppression and Narrow-Pulse-Shielding Techniques. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3093-3097.	2.2	12
67	Adaptive Maximum Power Point Tracking With Model-Based Negative Feedback Control and Improved Vâ€“f Model. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3103-3107.	2.2	3
68	A Two-Phase Three-Level Buck Converter With Cross-Connected Flying Capacitors for Inductor Current Balancing. IEEE Transactions on Power Electronics, 2021, 36, 13855-13866.	5.4	24
69	A 1.7-to-2.7GHz 35â€“38% PAE Multiband CMOS Power Amplifier Employing a Digitally-Assisted Analog Pre-Distorter (DAAPD) Reconfigurable Linearization Technique. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3381-3385.	2.2	7
70	A 12V-to-1V switched-capacitor-assisted hybrid converter with dual-path charge conduction and zero-voltage switching. IEICE Electronics Express, 2021, 18, 20210382-20210382.	0.3	2
71	A Periodically Time-Varying Inductor Applied to The Class-D VCO for Phase Noise Improvement. , 2021, , .		2
72	Recent Advances in High-Resolution Hybrid Discrete-Time Noise-Shaping ADCs. IEEE Open Journal of the Solid-State Circuits Society, 2021, 1, 129-139.	2.0	4

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73	Cancer drug screening with an on-chip multi-drug dispenser in digital microfluidics. Lab on A Chip, 2021, 21, 4749-4759.	3.1	22
74	A 0.01-mm² 1.2-pJ/bit 6.4-to-8Gb/s Reference-less FD-Less BBCDR Using a Deliberately-Clock-Selected Strobe Point Based on a 2Ï€/3-Interval Phase. , 2021, , .		2
75	Background Timing-Skew Mismatch Calibration for Time-Interleaved ADCs. , 2021, , .		1
76	A 15.2-to-18.2GHz Balanced Dual-Core Inverse-Class-F VCO with Q-Enhanced 2nd-Harmonic Resonance Achieving 187-to-188.1dBc/Hz FoM in 28nm CMOS. , 2021, , .		3
77	Design of Diode-Connected and Cross-Connected CMOS Rectifiers with Adaptive Tuning for RF Energy Harvesting. , 2021, , .		0
78	An Arithmetic Progression Switched-Capacitor DC-DC Converter with Soft VCR Transitions Achieving 93.7% Peak Efficiency and 400 mA Output Current. , 2021, , .		3
79	A 95% Peak Efficiency Modified KY (Boost) Converter for IoT with Continuous Flying Capacitor Charging in DCM. , 2021, , .		1
80	A 0.45-V 3.3-ÂµW Resistor-Based Temperature Sensor Achieving 10mK Resolution in 65-nm CMOS. , 2021, , .		1
81	Design Considerations of the Interpolative Digital Transmitter for Quantization Noise and Replicas Rejection. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 37-41.	2.2	4
82	A 1.6-GS/s 12.2-mW Seven-/Eight-Way Split Time-Interleaved SAR ADC Achieving 54.2-dB SNDR With Digital Background Timing Mismatch Calibration. IEEE Journal of Solid-State Circuits, 2020, 55, 693-705.	3.5	41
83	A 76.6-dB-SNDR 50-MHz-BW 29.2-mW Multi-Bit CT Sturdy MASH With DAC Non-Linearity Tolerance. IEEE Journal of Solid-State Circuits, 2020, 55, 344-355.	3.5	38
84	A 2.4-GHz Mid-Field CMOS Wireless Power Receiver Achieving 46% Maximum PCE and 163-mW Output Power. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 360-364.	2.2	11
85	A Temperature-Stabilized Single-Channel 1-GS/s 60-dB SNDR SAR-Assisted Pipelined ADC With Dynamic Gm-R-Based Amplifier. IEEE Journal of Solid-State Circuits, 2020, 55, 322-332.	3.5	43
86	A 12.5-MHz Bandwidth 77-dB SNDR SAR-Assisted Noise Shaping Pipeline ADC. IEEE Journal of Solid-State Circuits, 2020, 55, 312-321.	3.5	16
87	Portable NMR with Parallelism. Analytical Chemistry, 2020, 92, 2112-2120.	3.2	28
88	Cost-Effective Compensation Design for Output Customization and Efficiency Optimization in Series/Series-Parallel Inductive Power Transfer Converter. IEEE Transactions on Industrial Electronics, 2020, 67, 10356-10365.	5.2	10
89	A 0.096-mm$^{2}~1$ â€“20-GHz Triple-Path Noise- Canceling Common-Gate Common-Source LNA With Dual Complementary pMOSâ€“nMOS Configuration. IEEE Transactions on Microwave Theory and Techniques, 2020, 68, 144-159.	2.9	64
90	A 3.15-mW +16.0-dBm IIP3 22-dB CG Inductively Source Degenerated Balun-LNA Mixer With Integrated Transformer-Based Gate Inductor and IM2 Injection Technique. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 700-713.	2.1	19

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91	A 10.6-mW 26.4-GHz Dual-Loop Type-II Phase-Locked Loop Using Dynamic Frequency Detector and Phase Detector. IEEE Access, 2020, 8, 2222-2232.	2.6	16
92	LDO-Free Power Management System: A 10-bit Pipelined ADC Directly Powered by Inductor-Based Boost Converter With Ripple Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4174-4186.	3.5	6
93	An 8-Bit 10-GS/s 16Ã— Interpolation-Based Time-Domain ADC With <1.5-ps Uncalibrated Quantization Steps. IEEE Journal of Solid-State Circuits, 2020, 55, 3225-3235.	3.5	30
94	An NMOS Digital LDO With NAND-Based Analog-Assisted Loop in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4041-4052.	3.5	18
95	Digital Battery Management Unit With Built-In Resistance Compensation, Modulated Frequency Detection and Multi-Mode Protection for Fast, Efficient and Safe Charging. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4063-4074.	3.5	3
96	A 5 GS/s 29 mW Interleaved SAR ADC With 48.5 dB SNDR Using Digital-Mixing Background Timing-Skew Calibration for Direct Sampling Applications. IEEE Access, 2020, 8, 138944-138954.	2.6	17
97	A 0.5-V Supply, 36 nW Bandgap Reference With 42 ppm/Â°C Average Temperature Coefficient Within â^'40 Â°C to 120 Â°C. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3656-3669.	3.5	28
98	Design of a 4.2-to-5.1 GHz Ultralow-Power Complementary Class-B/C Hybrid-Mode VCO in 65-nm CMOS Fully Supported by EDA Tools. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3965-3977.	3.5	22
99	A 3.3-mW 25.2-to-29.4-GHz Current-Reuse VCO Using a Single-Turn Multi-Tap Inductor and Differential-Only Switched-Capacitor Arrays With a 187.6-dBc/Hz FOM. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3704-3717.	3.5	33
100	A Calibration-Free Ring-Oscillator PLL With Gain Tracking Achieving 9% Jitter Variation Over PVT. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3753-3763.	3.5	7
101	A 0.04% BER Strong PUF With Cell-Bias-Based CRPs Filtering and Background Offset Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3853-3865.	3.5	8
102	A Two-Phase Three-Level Buck DCâ€“DC Converter With X-Connected Flying Capacitors for Current Balancing. IEEE Solid-State Circuits Letters, 2020, 3, 442-445.	1.3	14
103	A 0.024-mm² 45.4-GHz-Bandwidth Unity-Gain Output Driver with S_{DD22}<-10dB up to 35 GHz. , 2020, , .		6
104	A Multiband FDD SAW-Less Transmitter for 5G-NR Featuring a BW-Extended <i>N</i>-Path Filter-Modulator, a Switched-BB Input, and a Wideband TIA-Based PA Driver. IEEE Journal of Solid-State Circuits, 2020, 55, 3387-3399.	3.5	3
105	A 65.5-dB SNDR 8.1â€“11.1-nW ECG SAR ADC With Adaptive-Latching OSC-Based Comparator and DAC Calibration. IEEE Solid-State Circuits Letters, 2020, 3, 482-485.	1.3	3
106	Turning on/off satellite droplet ejection for flexible sample delivery on digital microfluidics. Lab on A Chip, 2020, 20, 3709-3719.	3.1	16
107	A 6.4pJ/Bit Strong Physical Unclonable Function Based on Multiple-Stage Amplifier Chain. , 2020, , .		2
108	A Calibration-Free, Reference-Buffer-Free, Type-I Narrow-Pulse-Sampling PLL With â^'78.7-dBc REF Spur, â^'128.1-dBc/Hz Absolute In-Band PN and â^'254-dB FOM. IEEE Solid-State Circuits Letters, 2020, 3, 494-497.	1.3	15

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109	A Single-Pin Antenna Interface RF Front End Using a Single-MOS DCO-PA and a Pushâ€“Pull LNA. IEEE Journal of Solid-State Circuits, 2020, 55, 2055-2068.	3.5	9
110	A Power-Efficient Hybrid Single-Inductor Bipolar-Output DC-DC Converter with Floating Negative Output for AMOLED Displays. , 2020, , .		4
111	Piezoelectric Energy-Harvesting Interface Using Split-Phase Flipping-Capacitor Rectifier With Capacitor Reuse for Input Power Adaptation. IEEE Journal of Solid-State Circuits, 2020, 55, 2106-2117.	3.5	28
112	A 0.0285mm² 0.68pJ/bit Single-Loop Full-Rate Bang-Bang CDR without Reference and Separate Frequency Detector Achieving an 8.2(Gb/s)/Âµs Acquisition Speed of PAM-4 data in 28nm CMOS. , 2020, , .		13
113	A 100-MHz BW 72.6-dB-SNDR CT Î” Î£ Modulator Utilizing Preliminary Sampling and Quantization. IEEE Journal of Solid-State Circuits, 2020, , 1-1.	3.5	5
114	A VHF Wide-Input Range CMOS Passive Rectifier With Active Bias Tuning. IEEE Journal of Solid-State Circuits, 2020, 55, 2629-2638.	3.5	15
115	A 470-nA Quiescent Current and 92.7%/94.7% Efficiency DCT/PWM Control Buck Converter With Seamless Mode Selection for IoT Application. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4085-4098.	3.5	31
116	A SAR-ADC-Assisted DC-DC Buck Converter With Fast Transient Recovery. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1669-1673.	2.2	7
117	A 1-V 4-mW Differential-Folded Mixer With Common-Gate Transconductor Using Multiple Feedback Achieving 18.4-dB Conversion Gain, +12.5-dBm IIP3, and 8.5-dB NF. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1164-1174.	2.1	4
118	A Single-Stage Inductive-Power-Transfer Converter for Constant-Power and Maximum-Efficiency Battery Charging. IEEE Transactions on Power Electronics, 2020, 35, 8973-8984.	5.4	77
119	A digital microfluidic system with 3D microstructures for single-cell culture. Microsystems and Nanoengineering, 2020, 6, 6.	3.4	47
120	An Analog-Proportional Digital-Integral Multiloop Digital LDO With PSR Improvement and LCO Reduction. IEEE Journal of Solid-State Circuits, 2020, , 1-14.	3.5	20
121	10.1 A 1.4-to-2.7GHz FDD SAW-Less Transmitter for 5G-NR Using a BW-Extended N-Path Filter-Modulator, an Isolated-BB Input and a Wideband TIA-Based PA Driver Achieving <â˜’157.5dBc/Hz OB Noise. , 2020, , .		4
122	16.2 A 4Ã— Interleaved 10GS/s 8b Time-Domain ADC with 16Ã— Interpolation-Based Inter-Stage Gain Achieving >37.5dB SNDR at 18GHz Input. , 2020, , .		10
123	17.9 A 9mW 54.9-to-63.5GHz Current-Reuse LO Generator with a 186.7dBc/Hz FoM by Unifying a 20GHz 3rd-Harmonic-Rich Current-Output VCO, a Harmonic-Current Filter and a 60GHz TIA. , 2020, , .		17
124	A 4-Î¼m Diameter SPAD Using Less-Doped N-Well Guard Ring in Baseline 65-nm CMOS. IEEE Transactions on Electron Devices, 2020, 67, 2223-2225.	1.6	14
125	A comparative study of digital low dropout regulators. Journal of Semiconductors, 2020, 41, 111405.	2.0	8
126	11.5 A 2-Phase Soft-Charging Hybrid Boost Converter with Doubled-Switching Pulse Width and Shared Bootstrap Capacitor Achieving 93.5% Efficiency at a Conversion Ratio of 4.5. , 2020, , .		15

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127	A 5.1-to-7.3 mW, 2.4-to-5 GHz Class-C Mode-Switching Single-Ended-Complementary VCO Achieving >190 dBc/Hz FoM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 237-241.	2.2	5
128	A 0.044-mm² 0.5-to-7-GHz Resistor-Plus-Source-Follower-Feedback Noise-Cancelling LNA Achieving a Flat NF of 3.3Â±0.45 dB. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 71-75.	2.2	52
129	A 0.5-V 0.4-to-1.6-GHz 8-Phase Bootstrap Ring-VCO Using Inherent Non-Overlapping Clocks Achieving a 162.2-dBc/Hz FoM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 157-161.	2.2	10
130	A Comparative Study of 8-Phase Feedforward-Coupling Ring VCOs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 527-531.	2.2	13
131	Analysis of Reference Error in High-Speed SAR ADCs With Capacitive DAC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 82-93.	3.5	10
132	A 0.0018-mm² 153% Locking-Range CML-Based Divider-by-2 With Tunable Self-Resonant Frequency Using an Auxiliary Negative-$g_{{m}}$ Cell. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3330-3339.	3.5	11
133	Background Offset Calibration for Comparator Based on Temperature Drift Profile. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1648-1652.	2.2	5
134	A 0.12-mm² 1.2-to-2.4-mW 1.3-to-2.65-GHz Fractional-N Bang-Bang Digital PLL With 8-mu s Settling Time for Multi-ISM-Band ULP Radios. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3307-3316.	3.5	13
135	Design of KY Converter With Constant On-Time Control Under DCM Operation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1753-1757.	2.2	11
136	Analysis and Verification of Jitter in Bang-Bang Clock and Data Recovery Circuit With a Second-Order Loop Filter. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2223-2236.	2.1	18
137	Using EDA Tools to Push the Performance Boundaries of an Ultralow-Power IoT-VCO at 65nm. , 2019, , .		0
138	An Integrated DCâ€“DC Converter With Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery. IEEE Journal of Solid-State Circuits, 2019, 54, 2637-2648.	3.5	6
139	A 4-b 7-mu W Phase Domain ADC With Time Domain Reference Generation for Low-Power FSK/PSK Demodulation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3365-3372.	3.5	2
140	PID Control Considerations for Analog-Digital Hybrid Low-Dropout Regulators (Invited Paper). , 2019, , .		7
141	A Reconfigurable Cross-Connected Wireless-Power Transceiver for Bidirectional Device-to-Device Wireless Charging. IEEE Journal of Solid-State Circuits, 2019, 54, 2579-2589.	3.5	32
142	A 0.0071-mm² 10.8ps_{pp}-Jitter 4 to 10-Gb/s 5-Tap Current-Mode Transmitter Using a Hybrid Delay Line for Sub-1-UI Fractional De-Emphasis. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3991-4004.	3.5	8
143	Fully Integrated High Voltage Pulse Driver Using Switched-Capacitor Voltage Multiplier and Synchronous Charge Compensation in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1768-1772.	2.2	7
144	A $6.5imes7,mu$ m² 0.98-to-1.5 mW Nonself-Oscillation-Mode Frequency Divider-by-2 Achieving a Single-Band Untuned Locking Range of 166.6% (4â€“44 GHz). IEEE Solid-State Circuits Letters, 2019, 2, 37-40.	1.3	20

#	Article	IF	Citations
145	A 0.45-V 70-nW QRS Detector Using Decimated Quadratic Spline Wavelet Transform and Window-based Extrema Difference Techniques. , 2019, , .		0
146	A 40-Gb/s PAM-4 Transmitter Using a 0.16-pJ/bit SST-CML-Hybrid (SCH) Output Driver and a Hybrid-Path 3-Tap FFE Scheme in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4850-4861.	3.5	6
147	Algebraic Series-Parallel-Based Switched-Capacitor DCâ€“DC Boost Converter With Wide Input Voltage Range and Enhanced Power Density. IEEE Journal of Solid-State Circuits, 2019, 54, 3118-3134.	3.5	32
148	A 0.6-V 13-bit 20-MS/s Two-Step TDC-Assisted SAR ADC With PVT Tracking and Speed-Enhanced Techniques. IEEE Journal of Solid-State Circuits, 2019, 54, 3396-3409.	3.5	32
149	CMOS Cross-Coupled Differential-Drive Rectifier in Subthreshold Operation for Ambient RF Energy Harvestingâ€"Model and Analysis. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1942-1946.	2.2	22
150	Cell-based drug screening on microfluidics. TrAC - Trends in Analytical Chemistry, 2019, 117, 231-241.	5.8	48
151	26.2 A 0.08mm2 25.5-to-29.9GHz Multi-Resonant-RLCM-Tank VCO Using a Single-Turn Multi-Tap Inductor and CM-Only Capacitors Achieving 191.6dBc/Hz FoM and 130kHz 1/f3 PN Corner. , 2019, , .		23
152	16.3 A â˜’246dB Jitter-FoM 2.4GHz Calibration-Free Ring-Oscillator PLL Achieving 9% Jitter Variation Over PVT. , 2019, , .		9
153	A coin-battery-powered LDO-Free 2.4-GHz Bluetooth Low Energy/ZigBee receiver consuming 2â€¯mA. The Integration VLSI Journal, 2019, 66, 112-118.	1.3	0
154	Hydrodynamic-flow-enhanced rapid mixer for isothermal DNA hybridization kinetics analysis on digital microfluidics platform. Sensors and Actuators B: Chemical, 2019, 287, 390-397.	4.0	12
155	Micro- and nanofabrication NMR technologies for point-of-care medical applications â€“ A review. Microelectronic Engineering, 2019, 209, 66-74.	1.1	36
156	Multibit Sturdy MASH Î”Î£ Modulator with Error-shaped Segmented DACs for Wideband Low-power Applications. , 2019, , .		0
157	Wideband Variable-Gain Amplifiers Based on a Pseudo-Current-Steering Gain-Tuning Technique. , 2019, , .		5
158	A 200-MHz Wide Input Range CMOS Passive Rectifier with Active Bias Tunning. , 2019, , .		1
159	Digital Battery Management Unit with Built-In Resistance Compensation and Accidental Mutation Protection for Fast and Accurate Charging. , 2019, , .		2
160	A 0.14-to-0.29-pJ/bit 14-GBaud/s Trimodal (NRZ/PAM-4/PAM-8) Half-Rate Bang-Bang Clock and Data Recovery Circuit (BBCDR) in 28-nm CMOS. , 2019, , .		6
161	A Switched-Capacitor DC-DC Converter with Unequal Duty Cycle for Ripple Reduction and Efficiency Improvement. , 2019, , .		2
162	Instantaneous power quality indices detection under frequency deviated environment. IET Science, Measurement and Technology, 2019, 13, 1111-1121.	0.9	12

#	Article	IF	Citations
163	A Reconfigurable Bidirectional Wireless Power Transceiver for Battery-to-Battery Wireless Charging. IEEE Transactions on Power Electronics, 2019, 34, 7745-7753.	5.4	63
164	LampPort: a handheld digital microfluidic device for loop-mediated isothermal amplification (LAMP). Biomedical Microdevices, 2019, 21, 9.	1.4	42
165	A 550-mu W 20-kHz BW 100.8-dB SNDR Linear- Exponential Multi-Bit Incremental $SigmaDelta$ ADC With 256 Clock Cycles in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 1161-1172.	3.5	45
166	A 0.2-V Energy-Harvesting BLE Transmitter With a Micropower Manager Achieving 25% System Efficiency at 0-dBm Output and 5.2-nW Sleep Power in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 1351-1362.	3.5	42
167	Accuracy-Enhanced Variance-Based Time-Skew Calibration Using SAR as Window Detector. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 481-485.	2.1	10
168	Many-Objective Sizing Optimization of a Class-C/D VCO for Ultralow-Power IoT and Ultralow-Phase-Noise Cellular Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 69-82.	2.1	24
169	Design of a High-Speed Time-Interleaved Sub-Ranging SAR ADC With Optimal Code Transfer Technique. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 489-501.	3.5	3
170	A 0.0056-mm² â^'249-dB-FoM All-Digital MDLL Using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring VCOs. IEEE Journal of Solid-State Circuits, 2019, 54, 88-98.	3.5	21
171	A 1.2V 86dB SNDR 500kHz BW Linear-Exponential Multi-Bit Incremental ADC Using Positive Feedback in 65nm CMOS. , 2019, , .		7
172	Quick and cost-efficient A/D converter static characterization using low-precision testing signal. Microelectronics Journal, 2018, 74, 86-93.	1.1	2
173	A 0.18-V 382-<inline-formula> <tex-math notation="LaTeX">mu </tex-math> </inline-formula>W Bluetooth Low-Energy Receiver Front-End With 1.33-nW Sleep Power for Energy-Harvesting Applications in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 1618-1627.	3.5	50
174	Nano-Watt Class Energy-Efficient Capacitive Sensor Interface With On-Chip Temperature Drift Compensation. IEEE Sensors Journal, 2018, 18, 2870-2882.	2.4	15
175	A SAW-Less Tunable RF Front End for FDD and IBFD Combining an Electrical-Balance Duplexer and a Switched-<italic>LC</italic> N-Path LNA. IEEE Journal of Solid-State Circuits, 2018, 53, 1431-1442.	3.5	51
176	Passive Noise Shaping in SAR ADC With Improved Efficiency. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 416-420.	2.1	21
177	A Two-Way Interleaved 7-b 2.4-GS/s 1-Then-2 b/Cycle SAR ADC With Background Offset Calibration. IEEE Journal of Solid-State Circuits, 2018, 53, 850-860.	3.5	55
178	An inverse-class-F CMOS VCO with intrinsic-high-Q 1st- and 2nd-harmonic resonances for 1/f²-to-1/f³ phase-noise suppression achieving 196.2dBc/Hz FOM. , 2018, , .		28
179	A Coin-Battery-Powered LDO-Free 2.4-GHz Bluetooth Low-Energy Transmitter With 34.7% Peak System Efficiency. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1174-1178.	2.2	4
180	A regulation-free sub-0.5V 16/24MHz crystal oscillator for energy-harvesting BLE radios with 14.2nJ startup energy and 31.8pW steady-state power. , 2018, , .		8

#	Article	IF	Citations
181	A reconfigurable cross-connected wireless-power transceiver for bidirectional device-to-device charging with 78.1% total efficiency. , 2018, , .		9
182	A 0.4V 430nA quiescent current NMOS digital LDO with NAND-based analog-assisted loop in 28nm CMOS. , 2018, , .		34
183	A Hardware-Efficient Feedback Polynomial Topology for DPD Linearization of Power Amplifiers: Theory and FPGA Validation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 2889-2902.	3.5	13
184	A 0.032-mm² 0.15-V Three-Stage Charge-Pump Scheme Using a Differential Bootstrapped Ring-VCO for Energy-Harvesting Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 146-150.	2.2	46
185	An Analog-Assisted Tri-Loop Digital Low-Dropout Regulator. IEEE Journal of Solid-State Circuits, 2018, 53, 20-34.	3.5	88
186	Analysis of Common-Mode Interference and Jitter of Clock Receiver Circuits With Improved Topology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1819-1829.	3.5	7
187	Micro-NMR on CMOS for Biomolecular Sensing. , 2018, , 101-132.		4
188	Electronic-Automated Micro-NMR Assay with DMF Device. , 2018, , 41-71.		0
189	A 0.7â€“2.5 GHz, 61% EIRP System Efficiency, Four-Element MIMO TX System Exploiting Integrated Power-Relaxed Power Amplifiers and an Analog Spatial De-Interleaver. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 14-25.	3.5	1
190	Review and Selection Strategy for High-Accuracy Modeling of PWM Converters in DCM. Journal of Electrical and Computer Engineering, 2018, 2018, 1-16.	0.6	6
191	A Power Quality Indexes Measurement System Platform with Remote Alarm Notification. , 2018, , .		4
192	An Inverse-Class-F CMOS Oscillator With Intrinsic-High-Q First Harmonic and Second Harmonic Resonances. IEEE Journal of Solid-State Circuits, 2018, 53, 3528-3539.	3.5	42
193	A 7b 2 GS/s Time-Interleaved SAR ADC with Time Skew Calibration Based on Current Integrating Sampler. , 2018, , .		4
194	An Integrated DC-DC Converter with Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery. , 2018, , .		1
195	A 2.4-GHz Single-Pin Antenna Interface RF Front-End with a Function-Reuse Single-MOS VCO-PA and a Push-Pull LNA. , 2018, , .		3
196	A Digital LDO With Co-SA Logics and TSPC Dynamic Latches for Fast Transient Response. IEEE Solid-State Circuits Letters, 2018, 1, 154-157.	1.3	12
197	Algorithmic Voltage-Feed-In Topology for Fully Integrated Fine-Grained Rational Buckâ€“Boost Switched-Capacitor DCâ€“DC Converters. IEEE Journal of Solid-State Circuits, 2018, 53, 3455-3469.	3.5	24
198	Low-Phase-Noise Wideband Mode-Switching Quad-Core-Coupled mm-wave VCO Using a Single-Center-Tapped Switched Inductor. IEEE Journal of Solid-State Circuits, 2018, 53, 3232-3242.	3.5	51

#	Article	IF	Citations
199	Gain Error Calibrations for Two-Step ADCs: Optimizations Either in Accuracy or Chip Area. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2279-2289.	2.1	3
200	Process compensated bipolar junction transistorâ€based CMOS temperature sensor with a Â±1.5Â°C (3Ïƒ) batchâ€toâ€batch inaccuracy. Electronics Letters, 2018, 54, 1270-1272.	0.5	0
201	Ambient RF energy harvesting system: a review on integrated circuit design. Analog Integrated Circuits and Signal Processing, 2018, 97, 515-531.	0.9	12
202	A 0.19 mm² 10 b 2.3 GS/s 12-Way Time-Interleaved Pipelined-SAR ADC in 65-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3606-3616.	3.5	12
203	A 14-Bit Split-Pipeline ADC With Self-Adjusted Opamp-Sharing Duty-Cycle and Bias Current. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1380-1384.	2.2	5
204	A 10-MHz Bandwidth Two-Path Third-Order <inline-formula> <tex-math notation="LaTeX">$SigmaDelta$ </tex-math> </inline-formula> Modulator With Cross-Coupling Branches. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1410-1414.	2.2	3
205	A 0.083-mm² 25.2-to-29.5 GHz Multi-LC-Tank Class-F₂₃₄ VCO With a 189.6-dBc/Hz FOM. IEEE Solid-State Circuits Letters, 2018, 1, 86-89.	1.3	56
206	A Reconfigurable and Extendable Digital Architecture for Mixed Signal Power Electronics Controller. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1480-1484.	2.2	4
207	A 5.35-mW 10-MHz Single-Opamp Third-Order CT <inline-formula> <tex-math notation="LaTeX">$DeltaSigma$ </tex-math> </inline-formula> Modulator With CTC Amplifier and Adaptive Latch DAC Driver in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 2783-2794.	3.5	13
208	A 36-Gb/s 1.3-mW/Gb/s Duobinary-Signal Transmitter Exploiting Power-Efficient Cross-Quadrature Clocking Multiplexers With Maximized Timing Margin. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3014-3026.	3.5	25
209	A Regulation-Free Sub-0.5-V 16-/24-MHz Crystal Oscillator With 14.2-nJ Startup Energy and 31.8-mu W Steady-State Power. IEEE Journal of Solid-State Circuits, 2018, 53, 2624-2635.	3.5	21
210	A Wideband Inductorless dB-Linear Automatic Gain Control Amplifier Using a Single-Branch Negative Exponential Generator for Wireline Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3196-3206.	3.5	27
211	A Single-Stage Current-Mode Active Rectifier with Accurate Output-Current Regulation for IoT. , 2018, , .		8
212	Nano-Ampere Low-Dropout Regulator Designs for IoT Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 4017-4026.	3.5	46
213	Missing-Code-Occurrence Probability Calibration Technique for DAC Nonlinearity With Supply and Reference Circuit Analysis in a SAR ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3707-3719.	3.5	4
214	A 220-MHz Bondwire-Based Fully-Integrated KY Converter With Fast Transient Response Under DCM Operation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, , 1-12.	3.5	11
215	0.45â€V 5.4â€nW switchedâ€capacitor bandgap reference with intermittent operation and improved supply immunity. Electronics Letters, 2018, 54, 1154-1156.	0.5	7
216	A 6.78 MHz active voltage doubler with near-optimal on/off delay compensation for wireless power transfer systems. , 2018, , .		4

#	Article	IF	Citations
217	Handheld Total Chemical and Biological Analysis Systems. , 2018, , .		3
218	One-Chip Micro-NMR Platform with B0-Field Stabilization. , 2018, , 73-90.		0
219	Metastablility in SAR ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 111-115.	2.2	15
220	A Wide Input Range Dual-Path CMOS Rectifier for RF Energy Harvesting. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 166-170.	2.2	111
221	A 10-bit 500-MS/s Partial-Interleaving Pipelined SAR ADC With Offset and Reference Mismatch Calibrations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 354-363.	2.1	13
222	Activeâ€“Passive $Delta Sigma $ Modulator for High-Resolution and Low-Power Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 364-374.	2.1	20
223	A 0.45 V 147â€“375 nW ECG Compression Processor With Wavelet Shrinkage and Adaptive Temporal Decimation Architectures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1307-1319.	2.1	27
224	A 73.9%-Efficiency CMOS Rectifier Using a Lower DC Feeding (LDCF) Self-Body-Biasing Technique for Far-Field RF Energy-Harvesting Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 992-1002.	3.5	76
225	A 0.35-V 520- $mu ext{W}$ 2.4-GHz Current-Bleeding Mixer With Inductive-Gate and Forward-Body Bias, Achieving >13-dB Conversion Gain and >55-dB Port-to-Port Isolation. IEEE Transactions on Microwave Theory and Techniques, 2017, 65, 1284-1293.	2.9	20
226	22.4 A reconfigurable bidirectional wireless power transceiver with maximum-current charging mode and 58.6% battery-to-battery efficiency. , 2017, , .		21
227	A sub-1V 78-nA bandgap reference with curvature compensation. Microelectronics Journal, 2017, 63, 35-40.	1.1	14
228	DCM operation analysis of 3â€level boost converters. Electronics Letters, 2017, 53, 270-272.	0.5	5
229	A 3D microblade structure for precise and parallel droplet splitting on digital microfluidic chips. Lab on A Chip, 2017, 17, 896-904.	3.1	33
230	20.4 An output-capacitor-free analog-assisted digital low-dropout regulator with tri-loop control. , 2017, , .		55
231	16.4 A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with background offset calibration. , 2017, , .		21
232	A 7.8-mW 5-b 5-GS/s Dual-Edges-Triggered Time-Based Flash ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1966-1976.	3.5	21
233	A 4.2-mW 77.1-dB SNDR 5-MHz BW DT 2-1 MASH $Delta Sigma $ Modulator With Multirate Opamp Sharing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2641-2654.	3.5	39
234	A 0.038-mm2 SAW-Less Multiband Transceiver Using an N-Path SC Gain Loop. IEEE Journal of Solid-State Circuits, 2017, 52, 2055-2070.	3.5	12

#	Article	IF	Citations
235	A High-Voltage-Enabled Class-D Polar PA Using Interactive AM-AM Modulation, Dynamic Matching, and Power-Gating for Average PAE Enhancement. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2844-2857.	3.5	5
236	A 12b 180MS/s 0.068mm² With Full-Calibration-Integrated Pipelined-SAR ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1684-1695.	3.5	24
237	LC-VCOs using spiral inductors with single- and dual-layer patterned floating shields: a comparative study. Analog Integrated Circuits and Signal Processing, 2017, 91, 497-502.	0.9	1
238	Reconfigurable mismatchâ€free timeâ€interleaved bandpass sigmaâ€“delta modulator for wireless communications. Electronics Letters, 2017, 53, 506-508.	0.5	3
239	A 2.4-GHz ZigBee Transmitter Using a Function-Reuse Class-F DCO-PA and an ADPLL Achieving 22.6% (14.5%) System Efficiency at 6-dBm (0-dBm) $P_{mathrm {out}}$. IEEE Journal of Solid-State Circuits, 2017, 52, 1495-1508.	3.5	22
240	Fully Integrated Inductor-Less Flipping-Capacitor Rectifier for Piezoelectric Energy Harvesting. IEEE Journal of Solid-State Circuits, 2017, 52, 3168-3180.	3.5	77
241	A 27-Gb/s Time-Interleaved Duobinary Transmitter Achieving 1.44-mW/Gb/s FOM in 65-nm CMOS. IEEE Microwave and Wireless Components Letters, 2017, 27, 839-841.	2.0	15
242	Drug screening of cancer cell lines and human primary tumors using droplet microfluidics. Scientific Reports, 2017, 7, 9109.	1.6	69
243	An Area-Efficient and Tunable Bandwidth- Extension Technique for a Wideband CMOS Amplifier Handling 50+ Gb/s Signaling. IEEE Transactions on Microwave Theory and Techniques, 2017, 65, 4960-4975.	2.9	24
244	Split-based time-interleaved ADC with digital background timing-skew calibration. , 2017, , .		5
245	A digital PWM controlled KY step-up converter based on passive sigma-delta modulator. , 2017, , .		2
246	60-dB SNDR 100-MS/s SAR ADCs With Threshold Reconfigurable Reference Error Calibration. IEEE Journal of Solid-State Circuits, 2017, 52, 2576-2588.	3.5	40
247	A digital PWM controlled KY step-up converter based on frequency domain Î£Î” ADC. , 2017, , .		1
248	Piecewise BJT process spread compensation exploiting base recombination current. , 2017, , .		2
249	A digital microfluidic system for loop-mediated isothermal amplification and sequence specific pathogen detection. Scientific Reports, 2017, 7, 14586.	1.6	56
250	Seven-bit 700-MS/s Four-Way Time-Interleaved SAR ADC With Partial $V_{mathrm {cm}}$ -Based Switching. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1168-1172.	2.1	12
251	A Handheld High-Sensitivity Micro-NMR CMOS Platform With B-Field Stabilization for Multi-Type Biological/Chemical Assays. IEEE Journal of Solid-State Circuits, 2017, 52, 284-297.	3.5	50
252	A Single-Chip Solar Energy Harvesting IC Using Integrated Photodiodes for Biomedical Implant Applications. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 44-53.	2.7	83

#	Article	IF	Citations
253	A Dual-Output Wireless Power Transfer System With Active Rectifier and Three-Level Operation. IEEE Transactions on Power Electronics, 2017, 32, 927-930.	5.4	35
254	A 5-bit 2 GS/s binary-search ADC with charge-steering comparators. , 2017, , .		1
255	A 310 nW 14.2-bit iterative-incremental ADC for wearable sensing systems. , 2017, , .		1
256	A 5.35 mW 10 MHz bandwidth CT third-order Î”Î£ modulator with single Opamp achieving 79.6/84.5 dB SNDR/DR in 65 nm CMOS. , 2017, , .		0
257	A 0.4V 4.8Î¼W 16MHz CMOS crystal oscillator achieving 74-fold startup-time reduction using momentary detuning. , 2017, , .		2
258	A missing-code-detection gain error calibration achieving 63dB SNR for an 11-bit ADC. , 2017, , .		2
259	Circuit Techniques for IoT-Enabling Short-Range ULP Radios. , 2017, , 385-408.		0
260	A high DR multi-channel stage-shared hybrid front-end for integrated power electronics controller. , 2016, , .		7
261	A 0.011mm² 60dB SNDR 100MS/s reference error calibrated SAR ADC with 3pF decoupling capacitance for reference voltages. , 2016, , .		3
262	A high-Q spiral inductor with dual-layer patterned floating shield in a class-B VCO achieving a 190.5-dBc/Hz FoM. , 2016, , .		7
263	A high resolution multi-bit incremental converter insensitive to DAC mismatch error. , 2016, , .		6
264	A digital LDO with transient enhancement and limit cycle oscillation reduction. , 2016, , .		5
265	Joint-digital-predistortion for wireless transmitterâ€™s I/Q imbalance and PA nonlinearities using an asymmetrical complexity-reduced Volterra series model. Analog Integrated Circuits and Signal Processing, 2016, 87, 35-47.	0.9	4
266	A Time-Interleaved Ring-VCO with Reduced 1/ $ext {f}^{3}$ Phase Noise Corner, Extended Tuning Range and Inherent Divided Output. IEEE Journal of Solid-State Circuits, 2016, 51, 2979-2991.	3.5	23
267	A 312 ps responseâ€time LDO with enhanced super source follower in 28Ânm CMOS. Electronics Letters, 2016, 52, 1368-1370.	0.5	30
268	A <inline-formula> <tex-math notation="LaTeX">$mu $ </tex-math> </inline-formula>NMR CMOS Transceiver Using a Butterfly-Coil Input for Integration With a Digital Microfluidic Device Inside a Portable Magnet. IEEE Journal of Solid-State Circuits, 2016, 51, 2274-2286.	3.5	22
269	A 1.1 Î¼W CMOS Smart Temperature Sensor with an Inaccuracy of Â±0.2Â°C (3Ïƒ) for Clinical Temperature Monitoring. IEEE Sensors Journal, 2016, , 1-1.	2.4	13
270	Sub-7-second genotyping of single-nucleotide polymorphism by high-resolution melting curve analysis on a thermal digital microfluidic device. Lab on A Chip, 2016, 16, 743-752.	3.1	23

#	Article	IF	Citations
271	Wide Input Range Supply Voltage Tolerant Capacitive Sensor Readout Using On-Chip Solar Cell. Journal of Circuits, Systems and Computers, 2016, 25, 1640006.	1.0	0
272	Limit Cycle Oscillation Reduction for Digital Low Dropout Regulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 903-907.	2.2	49
273	Time-domain I/Q-LOFT compensator using a simple envelope detector for a sub-GHz IEEE 802.11af WLAN transmitter. , 2016, , .		0
274	Sub-ÂµW QRS detection processor using quadratic spline wavelet transform and maxima modulus pair recognition for power-efficient wireless arrhythmia monitoring. , 2016, , .		0
275	A Fully Integrated Digital LDO With Coarseâ€“Fine-Tuning and Burst-Mode Operation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 683-687.	2.2	116
276	A 6 b 5 GS/s 4 Interleaved 3 b/Cycle SAR ADC. IEEE Journal of Solid-State Circuits, 2016, 51, 365-377.	3.5	32
277	A 2- 45-nV/âˆšHz Readout Front End With Multiple-Chopping Active-High-Pass Ripple Reduction Loop and Pseudofeedback DC Servo Loop. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 351-355.	2.2	36
278	Sub-threshold VLSI logic family exploiting unbalanced pull-up/down network, logical effort and inverse-narrow-width techniques. , 2016, , .		3
279	An 11b 450 MS/s Three-Way Time-Interleaved Subranging Pipelined-SAR ADC in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2016, 51, 1223-1234.	3.5	30
280	Uniform Quantization Theory-Based Linearity Calibration for Split Capacitive DAC in an SAR ADC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2603-2607.	2.1	14
281	The dispersal analysis on basis construction of digital predistortion techniques for power amplifiers. Analog Integrated Circuits and Signal Processing, 2016, 86, 77-86.	0.9	3
282	A 2-<formula formulatype="inline"><tex Notation="TeX">$mu{hbox{m}}$</tex></formula> InGaP/GaAs Class-J Power Amplifier for Multi-Band LTE Achieving 35.8-dB Gain, 40.5% to 55.8% PAE and 28-dBm Linear Output Power. IEEE Transactions on Microwave Theory and Techniques, 2016, 64, 200-209.	2.9	27
283	A 2.4-GHz ZigBee Receiver Exploiting an RF-to-BB-Current-Reuse BlixerÂ+ÂHybrid Filter Topology in 65-nm CMOS. Analog Circuits and Signal Processing Series, 2016, , 33-55.	0.3	1
284	Histogram-Based Ratio Mismatch Calibration for Bridge-DAC in 12-bit 120 MS/s SAR ADC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1203-1207.	2.1	24
285	Analysis and Modeling of a Gain-Boosted N-Path Switched-Capacitor Bandpass Filter. Analog Circuits and Signal Processing Series, 2016, , 57-80.	0.3	3
286	A Sub-GHz Multi-ISM-Band ZigBee Receiver Using Function-Reuse and Gain-Boosted N-Path Techniques for IoT Applications. Analog Circuits and Signal Processing Series, 2016, , 81-103.	0.3	25
287	A palm-size Î¼NMR relaxometer using a digital microfluidic device and a semiconductor transceiver for chemical/biological diagnosis. Analyst, The, 2015, 140, 5129-5137.	1.7	37
288	A Sub-GHz Wireless Transmitter Utilizing a Multi-Class-Linearized PA and Time-Domain Wideband-Auto I/Q-LOFT Calibration for IEEE 802.11af WLAN. IEEE Transactions on Microwave Theory and Techniques, 2015, 63, 3228-3241.	2.9	9

#	Article	IF	Citations
289	Polyphase Decomposition for Tunable Band-Pass Sigma-Delta A/D Converters. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 537-547.	2.7	8
290	Corrections to â€œA $hbox{0.02 mm}^{2}$ 59.2 dB SFDR 4th-Order SC LPF With 0.5-to-10 MHz Bandwidth Scalability Exploiting a Recycling SC-Buffer Biquadâ€•[Sep 15 1988-2001]. IEEE Journal of Solid-State Circuits, 2015, 50, 2464-2464.	3.5	0
291	20.4 A 123-phase DC-DC converter-ring with fast-DVS for microprocessors. , 2015, , .		35
292	DCM operation analysis of KY converter. Electronics Letters, 2015, 51, 2037-2039.	0.5	9
293	A 89fJ-FOM 6-bit 3.4GS/s flash ADC with 4x time-domain interpolation. , 2015, , .		14
294	Self-Reconfiguration Property of a Mixed Signal Controller for Improving Power Quality Compensation During Light Loading. IEEE Transactions on Power Electronics, 2015, 30, 5938-5951.	5.4	11
295	On the droplet velocity and electrode lifetime of digital microfluidics: voltage actuation techniques and comparison. Microfluidics and Nanofluidics, 2015, 18, 673-683.	1.0	33
296	Energy Optimized Subthreshold VLSI Logic Family With Unbalanced Pull-Up/Down Network and Inverse Narrow-Width Techniques. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 3119-3123.	2.1	22
297	Improving the Linearity and Power Efficiency of Active Switched-Capacitor Filters in a Compact Die Area. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 3104-3108.	2.1	1
298	A 0.0045- <inline-formula> <tex-math notation="TeX">$hbox{mm}^{2}$</tex-math></inline-formula> 32.4- <inline-formula> <tex-math notation="TeX">$muhbox{W} $</tex-math></inline-formula> Two-Stage Amplifier for pF-to-nF Load Using CM Frequency Compensation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 246-250.	2.2	21
299	A review and design of the on-chip rectifiers for RF energy harvesting. , 2015, , .		28
300	0.0045Âmm ² 15.8 ÂµW threeâ€stage amplifier driving 10Ã—â€wide (0.15â€“1.5ÂnF) capacitive loads with >50Â° phase margin. Electronics Letters, 2015, 51, 454-456.	0.5	5
301	A 0.02 mm<formula formulatype="inline"><tex Notation="TeX">^{2}</tex></formula> 59.2 dB SFDR 4th-Order SC LPF With 0.5-to-10 MHz Bandwidth Scalability Exploiting a Recycling SC-Buffer Biquad. IEEE Journal of Solid-State Circuits, 2015, 50, 1988-2001.	3.5	8
302	A 0.07 mm<formula formulatype="inline"><tex Notation="TeX">^{2}</tex></formula> 2.2 mW 10 GHz Current-Reuse Class-B/C Hybrid VCO Achieving 196-dBc/Hz FoM<formula formulatype="inline"><tex Notation="TeX">$_{{m A}}$</tex> </formula>. IEEE Microwave and Wireless Components Letters, 2015, 25, 457-459.	2.0	21
303	Adhesion promoter for a multi-dielectric-layer on a digital microfluidic chip. RSC Advances, 2015, 5, 48626-48630.	1.7	16
304	2.4 A 0.028mm² 11mW single-mixing blocker-tolerant receiver with double-RF N-path filtering, S<inf>11</inf> centering, +13dBm OB-IIP3 and 1.5-to-2.9dB NF. , 2015, , .		13
305	Wideband Receivers: Design Challenges, Tradeoffs and State-of-the-Art. IEEE Circuits and Systems Magazine, 2015, 15, 12-24.	2.6	36
306	A Combinatorial Impairment-Compensation Digital Predistorter for a Sub-GHz IEEE 802.11af-WLAN CMOS Transmitter Covering a 10x-Wide RF Bandwidth. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1025-1032.	3.5	13

#	Article	IF	Citations
307	Nested-Current-Mirror Rail-to-Rail-Output Single-Stage Amplifier With Enhancements of DC Gain, GBW and Slew Rate. IEEE Journal of Solid-State Circuits, 2015, 50, 2353-2366.	3.5	63
308	Resolutionâ€enhanced sturdy MASH deltaâ€“sigma modulator for wideband lowâ€voltage applications. Electronics Letters, 2015, 51, 1061-1063.	0.5	9
309	Thermal and Reference Noise Analysis of Time-Interleaving SAR and Partial-Interleaving Pipelined-SAR ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2196-2206.	3.5	21
310	A 3.6â€mW 6â€GHz currentâ€reuse VCOâ€buffer with improved load drivability in 65â€nm CMOS. International Journal of Circuit Theory and Applications, 2015, 43, 133-138.	1.3	6
311	A 0.137 mm$^{{2}}$ 9 GHz Hybrid Class-B/C QVCO With Output Buffering in 65 nm CMOS. IEEE Microwave and Wireless Components Letters, 2014, 24, 716-718.	2.0	5
312	Jitter-resistant Capacitor Based Sine-Shaped DAC for Continuous-Time Sigma-Delta modulators. , 2014, , .		1
313	Natural discharge after pulse and cooperative electrodes to enhance droplet velocity in digital microfluidics. AIP Advances, 2014, 4, 047129.	0.6	9
314	A 104μW EMI-resisting bandgap voltage reference achieving −20dB PSRR, and 5% DC shift under a 4dBm EMI level. , 2014, , .		4
315	Split-SAR ADCs: Improved Linearity With Power and Speed Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 372-383.	2.1	53
316	Analysis and Modeling of a Gain-Boosted N-Path Switched-Capacitor Bandpass Filter. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2560-2568.	3.5	50
317	3.9 An RF-to-BB current-reuse wideband receiver with parallel N-path active/passive mixers and a single-MOS pole-zero LPF. , 2014, , .		5
318	Micropower two-stage amplifier employing recycling current-buffer Miller compensation. , 2014, , .		5
319	A Sub-GHz Multi-ISM-Band ZigBee Receiver Using Function-Reuse and Gain-Boosted N-Path Techniques for IoT Applications. IEEE Journal of Solid-State Circuits, 2014, 49, 2990-3004.	3.5	48
320	Enhancing the performances of recycling folded cascode OpAmp in nanoscale CMOS through voltage supply doubling and design for reliability. International Journal of Circuit Theory and Applications, 2014, 42, 605-619.	1.3	5
321	An RF-to-BB-Current-Reuse Wideband Receiver With Parallel N-Path Active/Passive Mixers and a Single-MOS Pole-Zero LPF. IEEE Journal of Solid-State Circuits, 2014, 49, 2547-2559.	3.5	41
322	NMRâ€“DMF: a modular nuclear magnetic resonanceâ€“digital microfluidics system for biological assays. Analyst, The, 2014, 139, 6204-6213.	1.7	17
323	A sine-LO square-law harmonic-rejection mixerâ€”theory, implementation, and application. IEEE Transactions on Microwave Theory and Techniques, 2014, 62, 313-322.	2.9	8
324	9.4 A 0.5V 1.15mW 0.2mm² Sub-GHz ZigBee receiver supporting 433/860/915/960MHz ISM bands with zero external components. , 2014, , .		12

#	Article	IF	Citations
325	A 2.4 GHz ZigBee Receiver Exploiting an RF-to-BB-Current-Reuse Blixer + Hybrid Filter Topology in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2014, 49, 1333-1344.	3.5	51
326	A 0.14-${hbox {mm}}^{2}$ 1.4-mW 59.4-dB-SFDR 2.4-GHz ZigBee/WPAN Receiver Exploiting a â€œSplit-LNTA + 50% LOâ€•Topology in 65-nm CMOS. IEEE Transactions on Microwave Theory and Techniques, 2014, 62, 1525-1534.	2.9	29
327	A 0.6V 8b 100MS/s SAR ADC with minimized DAC capacitance and switching energy in 65nm CMOS. , 2013, , .		4
328	A 53-to-75-mW, 59.3-dB HRR, TV-Band White-Space Transmitter Using a Low-Frequency Reference LO in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 2078-2089.	3.5	13
329	A 1.7mW 0.22mm² 2.4GHz ZigBee RX exploiting a current-reuse blixer + hybrid filter topology in 65nm CMOS. , 2013, , .		3
330	Excess-loop-delay compensation technique for CT Î”Î£ modulator with hybrid activeâ€“passive loop-filters. Analog Integrated Circuits and Signal Processing, 2013, 76, 35-46.	0.9	0
331	A Nonrecursive Digital Calibration Technique for Joint Elimination of Transmitter and Receiver I/Q Imbalances With Minimized Add-On Hardware. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 462-466.	2.2	12
332	Correction to "A 0.016 mmÂ² 144-ÂµW Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load With >0.95-MHz GBW". IEEE Journal of Solid-State Circuits, 2013, 48, 1539-1539.	3.5	0
333	A 10.4-ENOB 120MS/s SAR ADC with DAC linearity calibration in 90nm CMOS. , 2013, , .		5
334	Construction of a microfluidic chip, using dried-down reagents, for LATE-PCR amplification and detection of single-stranded DNA. Lab on A Chip, 2013, 13, 4635.	3.1	14
335	Systematic analysis and cancellation of kickback noise in a dynamic latched comparator. Analog Integrated Circuits and Signal Processing, 2013, 77, 277-284.	0.9	22
336	A 5-Bit 1.25-GS/s 4x-Capacitive-Folding Flash ADC in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 2154-2169.	3.5	18
337	A 2.93μW 8-bit capacitance-to-RF converter for movable laboratory mice blood pressure monitoring. , 2013, , .		0
338	Optimization of microwatt on-chip charge pump for single-chip solar energy harvesting. , 2013, , .		1
339	An intelligent digital microfluidic system with fuzzy-enhanced feedback for multi-droplet manipulation. Lab on A Chip, 2013, 13, 443-451.	3.1	54
340	A 0.127-mm², 5.6-mW, 5th-order SC LPF with +23.5-dBm IIP3 and 1.5-to-15-MHz clock-defined bandwidth in 65-nm CMOS. , 2013, , .		1
341	A 0.016-mm^{2} 144-muW Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load With $> $0.95-MHz GBW. IEEE Journal of Solid-State Circuits, 2013, 48, 527-540.	3.5	126
342	A wideband multi-stage inverter-based driver amplifier for IEEE 802.22 WRAN transmitters. , 2013, , .		2

#	Article	IF	Citations
343	A 13-bit 60MS/s split pipelined ADC with background gain and mismatch error calibration. , 2013, , .		1
344	A 0.5V 10GHz 8-phase LC-VCO Combining current-reuse and back-gate-coupling techniques consuming 2mW. , 2013, , .		4
345	15-nW Biopotential LPFs in 0.35-<formula formulatype="inline"> <tex Notation="TeX">$mu{m m}$</tex></formula> CMOS Using Subthreshold-Source-Follower Biquads With and Without Gain Compensation. IEEE Transactions on Biomedical Circuits and Systems, 2013, 7, 690-702.	2.7	63
346	Sub-threshold standard cell library design for ultra-low power biomedical applications. , 2013, 2013, 1454-7.		15
347	A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC. IEEE Journal of Solid-State Circuits, 2013, 48, 1783-1794.	3.5	34
348	Low-complexity, full-resolution, mirror- switching digital predistortion scheme for polar-modulated power amplifiers. Electronics Letters, 2012, 48, 1551-1553.	0.5	1
349	Enhanced RFICs in Nanoscale CMOS. IEEE Microwave Magazine, 2012, 13, 80-89.	0.7	0
350	A 50-fJ 10-b 160-MS/s Pipelined-SAR ADC Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation. IEEE Journal of Solid-State Circuits, 2012, 47, 2614-2626.	3.5	27
351	A 2.3mW 10-bit 170MS/s two-step binary-search assisted time-interleaved SAR ADC. , 2012, , .		8
352	A 0.8 µW 8-bit 1.5∼20-pF-input-range capacitance-to-digital converter for lab-on-chip digital microfluidics systems. , 2012, , .		4
353	Inter-Stage Gain Error self-calibration of a 31.5fJ 10b 470MS/S Pipelined-SAR ADC. , 2012, , .		5
354	A 0.024 mm² 4.9 fJ 10-bit 2 MS/s SAR ADC in 65 nm CMOS. , 2012, , .		2
355	An 8-b 400-MS/s 2-b-Per-Cycle SAR ADC With Resistive DAC. IEEE Journal of Solid-State Circuits, 2012, 47, 2763-2772.	3.5	78
356	A dynamic-range-improved 2.4GHz WLAN class-E PA combining PWPM and cascode modulation. , 2012, , .		1
357	A 22.4 μW 80dB SNDR ΣΔ modulator with passive analog adder and SAR quantizer for EMG application. , 2012, , .		8
358	A 0.83-<formula formulatype="inline"><tex Notation="TeX">$mu {m W}$</tex></formula> QRS Detection Processor Using Quadratic Spline Wavelet Transform for Wireless ECG Acquisition in 0.35-<formula formulatype="inline"> <tex Notation="TeX">$mu{m m}$</tex></formula> CMOS. IEEE Transactions on Biomedical Circuits and Systems, 2012, 6, 586-595.	2.7	112
359	A 12-bit 110MS/s 4-stage single-opamp pipelined SAR ADC with ratio-based GEC technique. , 2012, , .		6
360	A frequency-translation technique for low-noise ultra-low-cutoff lowpass filtering. Analog Integrated Circuits and Signal Processing, 2012, 72, 265-269.	0.9	3

#	Article	IF	Citations
361	Double recycling technique for folded-cascode OTA. Analog Integrated Circuits and Signal Processing, 2012, 71, 137-141.	0.9	59
362	General Considerations of High-/Mixed-VDD Analog and RF Circuits and Systems. , 2012, , 9-34.		1
363	A Mixed-Voltage Unified Receiver Front-End for Full-Band Mobile TV in 65-nm CMOS. , 2012, , 81-119.		0
364	A Full-Band Mobile-TV LNA with Mixed-Voltage ESD Protection in 90-nm CMOS. , 2012, , 35-54.		0
365	A nonlinearity digital background calibration algorithm for 2.5bit/stage pipelined ADCs with opamp sharing architecture. , 2011, , .		0
366	Design techniques for nanometer wideband power-efficient CMOS ADCs. , 2011, , .		0
367	A 0.46mm² 4dB-NF unified receiver front-end for full-band mobile TV in 65nm CMOS. , 2011, , .		4
368	A FPGA-based power electronics controller for hybrid active power filters. , 2011, , .		5
369	A single-to-differential LNA topology with robust output gain-phase balancing against balun imbalance. , 2011, , .		10
370	Multi-merged-switched redundant capacitive DACs for 2b/cycle SAR ADC. , 2011, , .		0
371	A 35 fJ 10b 160 MS/s pipelined-SAR ADC with decoupled flip-around MDAC and self-embedded offset cancellation. , 2011, , .		12
372	A high-voltage-enabled recycling folded cascode OpAmp for nanoscale CMOS technologies. , 2011, , .		4
373	Noise shaping implementation in two-step/SAR ADC architectures based on delayed quantization error. , 2011, , .		5
374	A time-efficient dither-injection scheme for pipelined SAR ADC. , 2011, , .		1
375	Two Stage Operational Amplifiers: Power and Area Efficient Frequency Compensation for Driving a Wide Range of Capacitive Load. IEEE Circuits and Systems Magazine, 2011, 11, 26-42.	2.6	29
376	A 0.46-mm$ ^{2}$ 4-dB NF Unified Receiver Front-End for Full-Band Mobile TV in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2011, 46, 1970-1984.	3.5	50
377	A charge pump based timing-skew calibration for time-interleaved ADC. , 2011, , .		0
378	A dual-VCO-based quantizer with highly improved linearity and enlarged dynamic range. , 2011, , .		3

#	Article	IF	Citations
379	A reconfigurable low-noise dynamic comparator with offset calibration in 90nm CMOS. , 2011, , .		40
380	A passive Excess-Loop-Delay compensation technique for Gm-C based continuous-time ΣΔ modulators. , 2011, , .		4
381	An ultra-low-power filtering technique for biomedical applications. , 2011, 2011, 1859-62.		2
382	FPGA-based decoupled double synchronous reference frame PLL for active power filters. , 2011, , .		9
383	High-/Mixed-Voltage RF and Analog CMOS Circuits Come of Age. IEEE Circuits and Systems Magazine, 2010, 10, 27-39.	2.6	29
384	A threshold-embedded offset calibration technique for inverter-based flash ADCs. , 2010, , .		6
385	A power effective 5-bit 600 MS/s binary-search ADC with simplified switching. , 2010, , .		7
386	Analysis and Design of Open-Loop Multiphase Local-Oscillator Generator for Wireless Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 970-981.	3.5	15
387	Parasitics nonlinearity cancellation technique for split DAC architecture by using capacitive charge-pump. , 2010, , .		5
388	Design and Experimental Verification of a Power Effective Flash-SAR Subranging ADC. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 607-611.	2.2	28
389	A Rapid Power-Switchable Track-and-Hold Amplifier in 90-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 16-20.	2.2	17
390	A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 1111-1121.	3.5	571
391	A $2imes V_{m DD}$-Enabled Mobile-TV RF Front-End With TV-GSM Interoperability in 1-V 90-nm CMOS. IEEE Transactions on Microwave Theory and Techniques, 2010, 58, 1664-1676.	2.9	16
392	An efficient DAC and interstage gain error calibration technique for multi-bit pipelined ADCs. , 2010, , .		2
393	A background amplifier offset calibration technique for high-resolution pipelined ADCs. , 2010, , .		4
394	A digital background nonlinearity calibration algorithm for pipelined ADCs. , 2010, , .		1
395	Advanced Low Voltage Circuit Techniques. , 2010, , 27-54.		0
396	Design of a 1.2 V, 10-bit, 60â€“360 MHz Time-Interleaved Pipelined ADC. , 2010, , 75-95.		0

#	Article	IF	Citations
397	Challenges in Low-Voltage Circuit Designs. , 2010, , 11-26.		0
398	Experimental Results. , 2010, , 97-112.		0
399	Conclusions and Prospective for Future Work. , 2010, , 113-116.		0
400	High-speed robust level converter for ultra-low power 0.6-V LSIs to 3.3-V I/O. , 2009, , .		0
401	A 2.4 Hz-to-10 kHz-tunable biopotential filter using a novel capacitor multiplier. , 2009, , .		12
402	A 90nm CMOS bio-potential signal readout front-end with improved powerline interference rejection. , 2009, , .		18
403	Parasitic calibration by two-step ratio approaching technique for split capacitor array SAR ADCs. , 2009, , .		4
404	An active-balun LNA with forestage-poststage gain controls for VHF/UHF mobile-TV tuners. , 2009, , .		1
405	An open-loop octave-phase local-oscillator generator with high-precision correlated phases for VHF/UHF mobile-TV tuners. , 2009, , .		1
406	On-chip small capacitor mismatches measurement technique using beta-multiplier-biased ring oscillator. , 2009, , .		7
407	Design of an ESD-Protected Ultra-Wideband LNA in Nanoscale CMOS for Full-Band Mobile TV Tuners. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 933-942.	3.5	29
408	Comparator-based successive folding ADC. , 2009, , .		1
409	On the Design of a Programmable-Gain Amplifier With Built-In Compact DC-Offset Cancellers for Very Low-Voltage WLAN Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 496-509.	3.5	48
410	An open-source-input, ultra-wideband LNA with mixed-voltage ESD protection for full-band (170-to-1700 MHz) mobile TV tuners. , 2008, , .		2
411	A power scalable 6-bit 1.2GS/s flash ADC with power on/off Track-and-Hold and preamplifier. , 2008, , .		8
412	A pseudo-differential comparator-based pipelined ADC with common mode feedforward technique. , 2008, , .		1
413	A novel CMOS switched-current mode sequential shift forward inference circuit for fuzzy logic controller. , 2008, , .		0
414	Generalized Circuit Techniques for Low-Voltage High-Speed Reset- and Switched-Opamps. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 2188-2201.	3.5	5

#	Article	IF	Citations
415	Linearity analysis on a series-split capacitor array for high-speed SAR ADCs. , 2008, , .		6
416	A process- and temperature- insensitive current-controlled delay generator for sampled-data systems. , 2008, , .		1
417	Statistical Spectra and Distortion Analysis of Time-Interleaved Sampling Bandwidth Mismatch. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 648-652.	2.2	24
418	A 1-V 90dB DR audio stereo DAC with embedding headphone driver. , 2008, , .		4
419	A DC-offset-compensated, CT/DT hybrid filter with process-insensitive cutoff and low in-band group-delay variation for WLAN receivers. , 2008, , .		0
420	INTERACTIVE IIR SC MULTIRATE COMPILER APPLIED TO MULTISTAGE DECIMATOR DESIGN. Journal of Circuits, Systems and Computers, 2007, 16, 517-525.	1.0	1
421	Transceiver architecture selection: Review, state-of-the-art survey and case study. IEEE Circuits and Systems Magazine, 2007, 7, 6-25.	2.6	121
422	A 100MS/s recycling 2-step ADC embedding programmable gain amplification for DVB satellite. Midwest Symposium on Circuits and Systems, 2007, , .	1.0	1
423	Novel defected ground structure element with triple transmission zeros and its application for multispurious suppression of microstrip parallel-coupled-line bandpass filter. Microwave and Optical Technology Letters, 2007, 49, 1409-1412.	0.9	8
424	Experimental 1-V flexible-IF CMOS analogue-baseband chain for IEEE 802.11a/b/g WLAN receivers. IET Circuits, Devices and Systems, 2007, 1, 415.	0.9	4
425	A 1-V 2.5-mW Transient-Improved Current-Steering DAC using Charge-Removal-Replacement Technique. , 2006, , .		3
426	Design of microwave lumped and transversal bandpass filter with noise reduction. Microwave and Optical Technology Letters, 2006, 48, 1161-1164.	0.9	3
427	Compact Microstrip Quasi-Elliptic Bandpass Filter Using Open-Loop Dumbbell Shaped Defected Ground Structure. , 2006, , .		17
428	Multistandard-compliant receiver architecture with low-voltage implementation. , 2005, , .		0
429	Exact Spectra Analysis of Sampled Signals With Jitter-Induced Nonuniformly Holding Effects. IEEE Transactions on Instrumentation and Measurement, 2004, 53, 1279-1288.	2.4	17
430	Two-step channel selection technique by programmable digital-double quadrature sampling for complex low-IF receivers. Electronics Letters, 2003, 39, 825.	0.5	5
431	Impulse sampled FIR interpolation with SC active-delayed block polyphase structures. Electronics Letters, 1998, 34, 443.	0.5	4
432	MMIC active filter with tuned transversal element. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1998, 45, 632-634.	2.3	20

#	Article	IF	Citations
433	An optimum CMOS switched-capacitor antialiasing decimating filter. IEEE Journal of Solid-State Circuits, 1993, 28, 962-970.	3.5	26
434	Novel second-order switched-capacitor interpolator. Electronics Letters, 1992, 28, 348.	0.5	11
435	Optimum multistage multirate switched capacitor architectures for highly selective interface filtering. Electronics Letters, 1992, 28, 72-75.	0.5	0
436	IIR switched-capacitor decimator building blocks with optimum implementation. IEEE Transactions on Circuits and Systems, 1990, 37, 81-90.	0.9	43
437	A modular approach for high Q microwave CMOS active inductor design. , 0, , .		1
438	N-path multirate sigma-delta modulator for high-frequency applications. , 0, , .		1
439	Frequency-downconversion and IF channel selection A-DQS sample-and-hold pair for two-step-channel-select low-IF receiver. , 0, , .		3
440	A Novel Microstrip Transversal Bandpass Filter with Simultaneous Size Reduction and Spurious Responses Suppression. , 0, , .		6
441	A Novel Low-Voltage Cross-Coupled Passive Sampling Branch for Reset- and Switched-Opamp Circuits. , 0, , .		5
442	A Novel Very Low-Voltage SC-CMFB Technique for Fully-Differential Reset-Opamp Circuits. , 0, , .		2
443	A Novel Microstrip Bandpass Filter Design using Asymmetric Parallel Coupled-Line. , 0, , .		3
444	A switchedâ€capacitorâ€assisted wireless power transfer system with regulating TX power and fast global loop. Electronics Letters, 0, , .	0.5	2