# Hans Reisinger

List of Publications by Year
in descending order

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| 27 | 1,263 | 933447 | 1199594 |
|---|---|---|---|
| papers | citations | 10 h-index | 12 g-index |

| 27 | 27 | 27 | 563 |
|---|---|---|---|
| all docs | docs citations | times ranked | citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability. , 2010, , . | | 226 |
| 2 | Analysis of NBTI Degradation- and Recovery-Behavior Based on Ultra Fast VT-Measurements. , 2006, , . | | 188 |
| 3 | The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress. , 2010, , . | | 167 |
| 4 | Analytic modeling of the bias temperature instability using capture/emission time maps. , 2011, , . | | 136 |
| 5 | Review on SiC MOSFETs High-Voltage Device Reliability Focusing on Threshold Voltage Instability. IEEE Transactions on Electron Devices, 2019, 66, 4604-4616. | 3.0 | 101 |
| 6 | Understanding and modeling AC BTI. , 2011, , . | | 76 |
| 7 | Understanding BTI in SiC MOSFETs and Its Impact on Circuit Operation. IEEE Transactions on Device and Materials Reliability, 2018, 18, 144-153. | 2.0 | 70 |
| 8 | NBTI in Nanoscale MOSFETsâ€"The Ultimate Modeling Benchmark. IEEE Transactions on Electron Devices, 2014, 61, 3586-3593. | 3.0 | 49 |
| 9 | Understanding and modeling transient threshold voltage instabilities in SiC MOSFETs. , 2018, , . | | 36 |
| 10 | Threshold voltage hysteresis in SiC MOSFETs and its impact on circuit operation. , 2017, , . | | 23 |
| 11 | Impact of Mixed Negative Bias Temperature Instability and Hot Carrier Stress on MOSFET Characteristicsâ€"Part I: Experimental. IEEE Transactions on Electron Devices, 2019, 66, 232-240. | 3.0 | 22 |
| 12 | Physical Modeling of Charge Trapping in 4H-SiC DMOSFET Technologies. IEEE Transactions on Electron Devices, 2021, 68, 4016-4021. | 3.0 | 22 |
| 13 | Mixed Hot-Carrier/Bias Temperature Instability Degradation Regimes in Full {V <sub>G</sub>, V <sub>D</sub>} Bias Space: Implications and Peculiarities. IEEE Transactions on Electron Devices, 2020, 67, 3315-3322. | 3.0 | 20 |
| 14 | NBTI Degradation and Recovery in Analog Circuits: Accurate and Efficient Circuit-Level Modeling. IEEE Transactions on Electron Devices, 2019, 66, 1662-1668. | 3.0 | 18 |
| 15 | A Study of NBTI and Short-Term Threshold Hysteresis of Thin Nitrided and Thick Non-Nitrided Oxides. IEEE Transactions on Device and Materials Reliability, 2009, 9, 106-114. | 2.0 | 15 |
| 16 | Physical modeling of NBTI: From individual defects to devices. , 2014, , . | | 15 |
| 17 | On the influence of BTI and HCI on parameter variability. , 2017, , . | | 12 |
| 18 | Voltage-Dependent Activation Energy Maps for Analytic Lifetime Modeling of NBTI Without Time Extrapolation. IEEE Transactions on Electron Devices, 2018, 65, 4764-4771. | 3.0 | 12 |

| # | Article | IF | Citations |
|---|---|---|---|
| 19 | Circuit relevant HCS lifetime assessments at single transistors with emulated variable loads. , 2017, , . | | 11 |
| 20 | An Efficient Analog Compact NBTI Model for Stress and Recovery Based on Activation Energy Maps. IEEE Transactions on Electron Devices, 2019, 66, 4623-4630. | 3.0 | 10 |
| 21 | On the Physical Meaning of Single-Value Activation Energies for BTI in Si and SiC MOSFET Devices. IEEE Transactions on Electron Devices, 2021, 68, 236-243. | 3.0 | 10 |
| 22 | Analog-circuit NBTI degradation and time-dependent NBTI variability: An efficient physics-based compact model. , 2016, , . | | 6 |
| 23 | The Impact of Interfacial Charge Trapping on the Reproducibility of Measurements of Silicon Carbide MOSFET Device Parameters. Crystals, 2020, 10, 1143. | 2.2 | 6 |
| 24 | Optical Emission Correlated to Bias Temperature Instability in SiC MOSFETs. , 2022, , . | | 6 |
| 25 | Fast acquisition of activation energy maps using temperature ramps for lifetime modeling of BTI. , 2018, , . | | 4 |
| 26 | Efficient Evaluation of the Time-Dependent Threshold Voltage Distribution Due to NBTI Stress Using Transistor Arrays. , 2022, , . | | 2 |
| 27 | Performance Analysis of 4H-SiC Pseudo-D CMOS Inverter Circuits Employing Physical Charge Trapping Models. Materials Science Forum, 0, 1062, 688-695. | 0.3 | 0 |