# Yasuhiro Ogasahara

List of Publications by Year
in descending order



| 39 | 204 | 1478505 6 | 1199594 12 |
|---|---|---|---|
| papers | citations | h-index | g-index |

| 39 | 39 | 39 | 121 |
|---|---|---|---|
| all docs | docs citations | times ranked | citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | Yield and leakage current of organic thin-film transistor logic gates toward reliable and low-power operation of large-scale logic circuits for IoT nodes. Japanese Journal of Applied Physics, 2022, 61, SC1044. | 1.5 | 3 |
| 2 | Implementation of pseudo-linear feedback shift register-based physical unclonable functions on silicon and sufficient Challengeâ€“Response pair acquisition using Built-In Self-Test before shipping. The Integration VLSI Journal, 2020, 71, 144-153. | 2.1 | 6 |
| 3 | Measurement and Modeling of Ambient-Air-Induced Degradation in Organic Thin-Film Transistor. IEEE Transactions on Semiconductor Manufacturing, 2020, 33, 216-223. | 1.7 | 4 |
| 4 | Recovery-aware bias-stress degradation model for organic thin-film transistors considering drain and gate bias voltages. Japanese Journal of Applied Physics, 2020, 59, SGGG08. | 1.5 | 6 |
| 5 | Organic Current Mirror PUF for Improved Stability Against Device Aging. IEEE Sensors Journal, 2020, 20, 7569-7578. | 4.7 | 9 |
| 6 | OCM-PUF: organic current mirror PUF with enhanced resilience to device degradation. , 2019, , . | | 5 |
| 7 | Feasibility of a low-power, low-voltage complementary organic thin film transistor buskeeper physical unclonable function. Japanese Journal of Applied Physics, 2019, 58, SBBG03. | 1.5 | 7 |
| 8 | Mechanically and electrically robust metal-mask design for organic CMOS circuits. Japanese Journal of Applied Physics, 2018, 57, 04FL05. | 1.5 | 6 |
| 9 | An Experimental Design of Robust Current-mode Arbiter PUF using Organic Thin Film Transistors. , 2018, , . | | 0 |
| 10 | Measurement and Modeling of Frequency Degradation of an oTFT Ring Oscillator. , 2018, , . | | 3 |
| 11 | Prototype of USB stick-sized PUF module for authentication and key generation. , 2017, , . | | 1 |
| 12 | A 65-nm SOTB implementation of a physically unclonable function and its performance improvement by body bias control. , 2017, , . | | 2 |
| 13 | Implementation of pseudo linear feedback shift register physical unclonable function on silicon. , 2016, , . | | 5 |
| 14 | Impacts of flexible V<sub>th</sub> control, low process variability, and steep SS with low on-current of new structure transistors to ultra-low voltage designs. IEICE Electronics Express, 2015, 12, 20150460-20150460. | 0.8 | 2 |
| 15 | Low-power embedded read-only memory using atom switch and silicon-on-thin-buried-oxide transistor. Applied Physics Express, 2015, 8, 045201. | 2.4 | 2 |
| 16 | Standard cell implementation of buskeeper PUF with symmetric inverters and neighboring cells for passing randomness tests. , 2015, , . | | 3 |
| 17 | A Silicon-on-Thin-Buried-Oxide CMOS Microcontroller with Embedded Atom-Switch ROM. IEEE Micro, 2015, 35, 13-23. | 1.8 | 5 |
| 18 | Measurement of V<inf>th</inf> variation due to STI stress and inverse narrow channel effect at ultra-low voltage in a variability-suppressed process. , 2015, , . | | 0 |

| # | Article | IF | Citations |
|---|---|---|---|
| 19 | Reduction of overhead in adaptive body bias technology due to triple-well structure based on measurement and simulation. , 2015, , . | | 2 |
| 20 | SOTB Implementation of a Field Programmable Gate Array with Fine-Grained Vt Programmability. Journal of Low Power Electronics and Applications, 2014, 4, 188-200. | 2.0 | 8 |
| 21 | Near-0.1V ultra-low voltage operation of SOTB 1M logic gates. , 2014, , . | | 1 |
| 22 | More than an order of magnitude energy improvement of FPGA by combining 0.4V operation and Multi-Vt optimization of 20k body bias domains. , 2014, , . | | 4 |
| 23 | Utility of high on-off ratio, high off resistance rewritable device to EEPROM for ultra-low voltage operation of steep subthreshold slope FETs. , 2014, , . | | 4 |
| 24 | Resistivity-based modeling of substrate non-uniformity for low-resistivity substrate. IEICE Electronics Express, 2014, 11, 20130813-20130813. | 0.8 | 0 |
| 25 | The first SOTB implementation of Flex Power FPGA. , 2013, , . | | 5 |
| 26 | Supply Noise Suppression by Triple-Well Structure. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 781-785. | 3.1 | 12 |
| 27 | Measurement of on-chip I/O power supply noise and correlation verification between noise magnitude and delay increase due to SSO. , 2010, , . | | 0 |
| 28 | All-Digital Ring-Oscillator-Based Macro for Sensing Dynamic Supply Noise Waveform. IEEE Journal of Solid-State Circuits, 2009, 44, 1745-1755. | 5.4 | 33 |
| 29 | Measurement and Analysis of Inductive Coupling Noise in 90 nm Global Interconnects. IEEE Journal of Solid-State Circuits, 2008, 43, 718-728. | 5.4 | 7 |
| 30 | Measurement of supply noise suppression by substrate and deep N-well in 90nm process. , 2008, , . | | 11 |
| 31 | Dynamic supply noise measurement circuit composed of standard cells suitable for in-site SoC power integrity verification. , 2008, , . | | 2 |
| 32 | Dynamic Supply Noise Measurement with All Digital Gated Oscillator for Evaluating Decoupling Capacitance Effect. , 2007, , . | | 5 |
| 33 | Validation of a Full-Chip Simulation Model for Supply Noise and Delay Dependence on Average Voltage Drop With On-Chip Delay Measurement. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 868-872. | 2.2 | 31 |
| 34 | Impact of well edge proximity effect on timing. , 2007, , . | | 0 |
| 35 | Quantitative Prediction of On-Chip Capacitive and Inductive Crosstalk Noise and Tradeoff between Wire Cross-Sectional Area and Inductive Crosstalk Effect. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2007, E90-A, 724-731. | 0.3 | 2 |
| 36 | Quantitative Prediction of On-chip Capacitive and Inductive Crosstalk Noise and Discussion on Wire Cross-Sectional Area Toward Inductive Crosstalk Free Interconnects. Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors, 2006, , . | 0.0 | 2 |

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|---|---|---|---|
| 37 | W-CDMA Channel Codec by Configurable Processors. Intelligent Automation and Soft Computing, 2006, 12, 317-329. | 2.1 | 0 |
| 38 | Measurement of Inductive Coupling Effect on Timing in 90nm Global Interconnects. , 2006, , . | | 4 |
| 39 | Measurement results of delay degradation due to power supply noise well correlated with full-chip simulation. , 2006, , . | | 2 |