Stephen A Edwards

List of Publications by Year
in descending order

50	913	1040056 9	713466 21
papers	citations	h-index	g-index

53	53	53	363
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	The Sparse Synchronous Model. , 2020, , .		3
2	Master of none acceleration. , 2019, , .		8
3	Compositional Dataflow Circuits. Transactions on Embedded Computing Systems, 2019, 18, 1-27.	2.9	7
4	Further Experiences Teaching an FPGA-Based Embedded Systems Class. Lecture Notes in Computer Science, 2019, , 222-230.	1.3	1
5	On Determinism. Lecture Notes in Computer Science, 2018, , 240-253.	1.3	1
6	From functional programs to pipelined dataflow circuits. , 2017, , .		22
7	Network Synthesis for Database Processing Units. , 2017, , .		0
8	Deadlock-free joins in DB-mesh, an asynchronous systolic array accelerator. , 2017, , .		1
9	Compositional dataflow circuits. , 2017, , .		14
10	Hardware synthesis from a recursive functional language. , 2015, , .		4
11	Implementing latency-insensitive dataflow blocks. , 2015, , .		8
12	MEMOCODE 2014 software design contest: Space Invaders emulator. , 2014, , .		0
13	Welcome message from the chairs. , 2014, , .		0
14	MEMOCODE 2012 hardware/software codesign contest: DNA sequence aligner. , 2012, , .		7
15	Cache Impacts of Datatype Acceleration. IEEE Computer Architecture Letters, 2012, 11, 21-24.	1.5	4
16	Computation vs. Memory Systems: Pinning Down Accelerator Bottlenecks. Lecture Notes in Computer Science, 2011, , 86-98.	1.3	2
17	A novel analysis space for pointer analysis and its application for bug finding. Science of Computer Programming, 2010, 75, 921-942.	1.9	5
18	Ensuring deterministic concurrency through compilation. , 2010, , .		0

#	Article	IF	Citations
19	Simple and fast biased locks. , 2010, , .		23
20	Buffer Sharing in Rendezvous Programs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1471-1480.	2.7	0
21	Compiling SHIM. , 2010, , 121-146.		0
22	Compositional deadlock detection for rendezvous communication. , 2009, , .		3
23	Celling SHIM. , 2009, , .		9
24	A disruptive computer design idea: Architectures with repeatable timing. , 2009, , .		27
25	Buffer sharing in CSP-like programs. , 2009, , .		4
26	Compile-Time Analysis and Specialization of Clocks in Concurrent Programs. Lecture Notes in Computer Science, 2009, , 48-62.	1.3	11
27	Concurrency and Communication: Lessons from the SHIM Project. Lecture Notes in Computer Science, 2009, , 276-287.	1.3	1
28	Instantaneous Transitions in Esterel. Electronic Notes in Theoretical Computer Science, 2008, 203, 49-64.	0.9	0
29	Static Deadlock Detection for the SHIM Concurrent Language. , 2008, , .		11
30	Static elaboration of recursion for concurrent software. , 2008, , .		5
31	Predictable programming on a precision timed architecture. , 2008, , .		102
32	Programming shared memory multiprocessors with deterministic message-passing concurrency. , 2008, , .		17
33	Flexible pointer analysis using assign-fetch graphs. , 2008, , .		2
34	Programming Shared Memory Multiprocessors with Deterministic Message-Passing Concurrency: Compiling SHIM to Pthreads. , 2008, , .		3
35	A deterministic multi-way rendezvous library for haskell. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	5
36	Code Generation in the Columbia Esterel Compiler. Eurasip Journal on Embedded Systems, 2007, 2007, 1-31.	1.2	23

#	Article	IF	Citations
37	Optimizing Sequential Cycles Through Shannon Decomposition and Retiming. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 456-467.	2.7	11
38	Efficient code generation from SHIM models. ACM SIGPLAN Notices, 2006, 41, 125-134.	0.2	2
39	Compiling Esterel into Static Discrete-Event Code. Electronic Notes in Theoretical Computer Science, 2006, 153, 117-131.	0.9	11
40	A Domain-Specific Language for Generating Dataflow Analyzers. Electronic Notes in Theoretical Computer Science, 2006, 164, 103-119.	0.9	5
41	Scheduling-independent threads and exceptions in SHIM. , 2006, , .		30
42	A Processor Extension for Cycle-Accurate Real-Time Software. Lecture Notes in Computer Science, 2006, , 449-458.	1.3	17
43	Efficient code generation from SHIM models. , 2006, , .		8
44	SHIM. , 2005, , .		43
45	Experiences teaching an FPGA-based embedded systems class. ACM SIGBED Review, 2005, 2, 56-62.	1.8	20
46	Separate Compilation for Synchronous Modules. Lecture Notes in Computer Science, 2005, , 129-140.	1.3	13
47	Approximate Reachability for Dead Code Elimination in Esterelâ€‰â€†. Lecture Notes in Computer Science, 2005, , 323-337.	1.3	1
48	Generating fast code from concurrent program dependence graphs. ACM SIGPLAN Notices, 2004, 39, 175-181.	0.2	0
49	VIS. Lecture Notes in Computer Science, 1996, , 248-256.	1.3	17
50	VIS: A system for verification and synthesis. Lecture Notes in Computer Science, 1996, , 428-432.	1.3	351