Dennis Sylvester

List of Publications by Citations

96 papers	2,758 citations	26 h-index	50 g-index
104 ext. papers	3,502 ext. citations	4.1 avg, IF	5.21 L-index

#	Paper	IF	Citations
96	Near-Threshold Computing: Reclaiming Moore's Law Through Energy Efficient Integrated Circuits. *Proceedings of the IEEE*, **2010**, 98, 253-266	14.3	490
95	. *IEEE Journal of Solid-State Circuits*, **2012**, 47, 2534-2545	5.5	199
94	A Modular 1 mm^{3} Die-Stacked Sensing Platform With Low Power I^{2}C Inter-Die Communication and Multi-Modal Energy Harvesting. *IEEE Journal of Solid-State Circuits*, **2013**, 48, 229-243	5.5	127
93	Millimeter-scale nearly perpetual sensor system with stacked battery and solar cells **2010**,		115
92	A Low-Voltage Processor for Sensing Applications With Picowatt Standby Mode. *IEEE Journal of Solid-State Circuits*, **2009**, 44, 1145-1155	5.5	112
91	A highly resilient routing algorithm for fault-tolerant NoCs **2009**,		111
90	An Ultra-Low Power Fully Integrated Energy Harvester Based on Self-Oscillating Switched-Capacitor Voltage Doubler. *IEEE Journal of Solid-State Circuits*, **2014**, 49, 2800-2811	5.5	100
89	A Subthreshold Voltage Reference With Scalable Output Voltage for Low-Power IoT Systems. *IEEE Journal of Solid-State Circuits*, **2017**, 52, 1443-1449	5.5	94
88	A Variation-Tolerant Sub-200 mV 6-T Subthreshold SRAM. *IEEE Journal of Solid-State Circuits*, **2008**, 43, 2338-2348	5.5	91
87	A2: Analog Malicious Hardware **2016**,		89
86	**2017**,		58
85	Yield-Driven Near-Threshold SRAM Design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1590-1598	2.6	58
84	. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 995-1005	5.5	50
83	Low-Power High-Throughput LDPC Decoder Using Non-Refresh Embedded DRAM. *IEEE Journal of Solid-State Circuits*, **2014**, 49, 783-794	5.5	50
82	Swizzle-Switch Networks for Many-Core Systems. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2012**, 2, 278-294	5.2	50
81	SRAM for Error-Tolerant Applications With Dynamic Energy-Quality Management in 28 nm CMOS. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 1310-1323	5.5	46
80	Low-Power Circuit Analysis and Design Based on Heterojunction Tunneling Transistors (HETTs). *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 1632-1643	2.6	39

79	. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 1006-1015	5.5	36
78	A 28-nm Compute SRAM With Bit-Serial Logic/Arithmetic Operations for Programmable In-Memory Vector Computing. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 76-86	5.5	33
77	A 5.8 nW CMOS Wake-Up Timer for Ultra-Low-Power Wireless Applications. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 1754-1763	5.5	32
76	. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 261-274	5.5	32
75	CAS-FEST 2010: Mitigating Variability in Near-Threshold Computing. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2011**, 1, 42-49	5.2	31
74	A Constant Energy-Per-Cycle Ring Oscillator Over a Wide Frequency Range for Wireless Sensor Nodes. *IEEE Journal of Solid-State Circuits*, **2016**, 51, 697-711	5.5	30
73	A Resonant Current-Mode Wireless Power Receiver and Battery Charger With −32 dBm Sensitivity for Implantable Systems. *IEEE Journal of Solid-State Circuits*, **2016**, 51, 2880-2892	5.5	30
72	A Sub-nW Multi-stage Temperature Compensated Timer for Ultra-Low-Power Sensor Nodes. *IEEE Journal of Solid-State Circuits*, **2013**, 48, 2511-2521	5.5	28
71	Approximate SRAMs With Dynamic Energy-Quality Management. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 2128-2141	2.6	27
70	SLC: Split-control Level Converter for dense and stable wide-range voltage conversion **2012**,		24
69	. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 231-239	5.5	22
68	A 346 μm 2 VCO-Based, Reference-Free, Self-Timed Sensor Interface for Cubic-Millimeter Sensor Nodes in 28 nm CMOS. *IEEE Journal of Solid-State Circuits*, **2014**, 49, 2462-2473	5.5	21
67	A Low Ripple Switched-Capacitor Voltage Regulator Using Flying Capacitance Dithering. *IEEE Journal of Solid-State Circuits*, **2016**, 51, 919-929	5.5	19
66	An Acoustic Signal Processing Chip With 142-nW Voice Activity Detection Using Mixer-Based Sequential Frequency Scanning and Neural Network Classification. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 3005-3016	5.5	19
65	Fast Statistical Static Timing Analysis Using Smart Monte Carlo Techniques. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 852-865	2.5	19
64	Design Methodology for Voltage-Overscaled Ultra-Low-Power Systems. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2012**, 59, 952-956	3.5	18
63	Low-Power-Design Space Exploration Considering Process Variation Using Robust Optimization. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 67-79	2.5	18
62	5.2 Energy-Efficient Low-Noise CMOS Image Sensor with Capacitor Array-Assisted Charge-Injection SAR ADC for Motion-Triggered Low-Power IoT Applications **2019**,		17

61	A 5.58 nW Crystal Oscillator Using Pulsed Driver for Real-Time Clocks. *IEEE Journal of Solid-State Circuits*, **2016**, 51, 509-522	5.5	17
60	A 23pW, 780ppm/□C resistor-less current reference using subthreshold MOSFETs **2014**,		16
59	Process Variation and Temperature-Aware Full Chip Oxide Breakdown Reliability Analysis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 1321-1334	2.5	16
58	A statistical approach for full-chip gate-oxide reliability analysis **2008**,		16
57	A Self-Tuning IoT Processor Using Leakage-Ratio Measurement for Energy-Optimal Operation. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 87-97	5.5	16
56	Circuit and System Designs of Ultra-Low Power Sensor Nodes With Illustration in a Miniaturized GNSS Logger for Position Tracking: Part I□Analog Circuit Techniques. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2017**, 64, 2237-2249	3.9	15
55	System-On-Mud: Ultra-Low Power Oceanic Sensing Platform Powered by Small-Scale Benthic Microbial Fuel Cells. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2015**, 1-10	3.9	15
54	A 5.58nW 32.768kHz DLL-assisted XO for real-time clocks in wireless sensing applications **2012**,		15
53	A 1.85fW/bit ultra low leakage 10T SRAM with speed compensation scheme **2011**,		15
52	An Area-Efficient 128-Channel Spike Sorting Processor for Real-Time Neural Recording With $0.175~mu$ W/Channel in 65-nm CMOS. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 126-137	2.6	15
51	Energy-Efficient Motion-Triggered IoT CMOS Image Sensor With Capacitor Array-Assisted Charge-Injection SAR ADC. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 2921-2931	5.5	14
50	A 1920 $times$ 1080 25-Frames/s 2.4-TOPS/W Low-Power 6-D Vision Processor for Unified Optical Flow and Stereo Depth With Semi-Global Matching. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 1048-1058	5.5	14
49	A 0.3V VDDmin 4+2T SRAM for searching and in-memory computing using 55nm DDC technology **2017**,		14
48	Battery Voltage Supervisors for Miniature IoT Systems. *IEEE Journal of Solid-State Circuits*, **2016**, 51, 2743-2756	5.5	13
47	An Efficient Piezoelectric Energy Harvesting Interface Circuit Using a Sense-and-Set Rectifier. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 3348-3361	5.5	12
46	Robust Clock Network Design Methodology for Ultra-Low Voltage Operations. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2011**, 1, 120-130	5.2	12
45	Variation-aware static and dynamic writability analysis for voltage-scaled bit-interleaved 8-T SRAMs **2011**,		11
44	Robust ultra-low voltage ROM design **2008**,		11

43	Parametric Yield Analysis and Optimization in Leakage Dominated Technologies. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2007**, 15, 613-623	2.6	10
42	A 1.7nW PLL-assisted current injected 32KHz crystal oscillator for IoT **2017**,		9
41	**2019**,		8
40	NSF expedition on variability-aware software: Recent results and contributions. *IT - Information Technology*, **2015**, 57, 181-198	0.4	8
39	Dual-slope capacitance to digital converter integrated in an implantable pressure sensing system **2014**,		8
38	A 1.02nW PMOS-only, trim-free current reference with 282ppm/□C from □40□C to 120□C and 1.6% within-wafer inaccuracy **2017**,		7
37	A 1.6-mm2 38-mW 1.5-Gb/s LDPC decoder enabled by refresh-free embedded DRAM **2012**,		7
36	A Dual-Stage, Ultra-Low-Power Acoustic Event Detection System **2016**,		7
35	Subthreshold voltage reference with nwell/psub diode leakage compensation for low-power high-temperature systems **2017**,		6
34	Energy-optimized high performance FFT processor **2011**,		6
33	IoT2 □the Internet of Tiny Things: Realizing mm-Scale Sensors through 3D Die Stacking **2019**,		5
32	Circuit and System Design Guidelines for Ultra-low Power Sensor Nodes. *IPSJ Transactions on System LSI Design Methodology*, **2013**, 6, 17-26	0.2	5
31	A 67-fsrms Jitter, □130 dBc/Hz In-Band Phase Noise, □256-dB FoM Reference Oversampling Digital PLL With Proportional Path Timing Control. *IEEE Solid-State Circuits Letters*, **2020**, 3, 430-433	2	5
30	A Reference Oversampling Digital Phase-Locked Loop with -240 dB FOM and -80 dBc Reference Spur **2019**,		5
29	A Noise-Efficient Neural Recording Amplifier Using Discrete-Time Parametric Amplification. *IEEE Solid-State Circuits Letters*, **2018**, 1, 203-206	2	5
28	Reference Oversampling PLL Achieving □256-dB FoM and □78-dBc Reference Spur. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 2993-3007	5.5	5
27	Millimeter-scale computing platform for next generation of Internet of Things **2016**,		4
26	STEEL: A technique for stress-enhanced standard cell library design **2008**,		4

25	A 0.3-V to 1.8□3.3-V Leakage-Biased Synchronous Level Converter for ULP SoCs. *IEEE Solid-State Circuits Letters*, **2020**, 3, 130-133	2	4
24	RRAM-DNN: An RRAM and Model-Compression Empowered All-Weights-On-Chip DNN Accelerator. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 1105-1115	5.5	4
23	A 40-nm Ultra-Low Leakage Voltage-Stacked SRAM for Intelligent IoT Sensors. *IEEE Solid-State Circuits Letters*, **2021**, 4, 14-17	2	4
22	Victim Alignment in Crosstalk-Aware Timing Analysis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 261-274	2.5	3
21	Self-Timed Regenerators for High-Speed and Low-Power On-Chip Global Interconnect. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2008**, 16, 673-677	2.6	3
20	A Light Tolerant Neural Recording IC for Near-Infrared-Powered Free Floating Motes. **2021**, 2021,		3
19	A 42 nJ/Conversion On-Demand State-of-Charge Indicator for Miniature IoT Li-Ion Batteries. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 524-537	5.5	3
18	Achieving Ultralow Standby Power With an Efficient SCCMOS Bias Generator. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2013**, 60, 842-846	3.5	2
17	A Statistical Framework for Post-Fabrication Oxide Breakdown Reliability Prediction and Management. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 630-643	2.5	2
16	A 128kb high density portless SRAM using hierarchical bitlines and thyristor sense amplifiers **2011**,		2
15	Synchronization of ultra-low power wireless sensor nodes **2011**,		2
14	Standby power reduction techniques for ultra-low power processors **2008**,		2
13	A Light-Tolerant Wireless Neural Recording IC for Motor Prediction With Near-Infrared-Based Power and Data Telemetry. *IEEE Journal of Solid-State Circuits*, **2022**, 1-1	5.5	2
12	Sample and Average Common-Mode Feedback in a 101 nW Acoustic Amplifier **2020**,		2
11	An Ultra-Low-Power Image Signal Processor for Hierarchical Image Recognition With Deep Neural Networks. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 1071-1081	5.5	2
10	FOCUS: Key building blocks and integration strategy of a miniaturized wireless sensor node **2015**,		1
9	Circuits for ultra-low power millimeter-scale sensor nodes **2012**,		1
8	Demo: Ultra-constrained sensor platform interfacing **2012**,		1

List of Publications

7	A Delta Sigma-Modulated Sample and Average Common-Mode Feedback Technique for Capacitively Coupled Amplifiers in a 192-nW Acoustic Analog Front-End. *IEEE Journal of Solid-State Circuits*, **2022**, 1-1	5.5	1
6	Ultra-Low Power 32kHz Crystal Oscillators: Fundamentals and Design Techniques. *IEEE Open Journal of the Solid-State Circuits Society*, **2021**, 1, 79-93		1
5	AA-ResNet: Energy Efficient All-Analog ResNet Accelerator **2020**,		1
4	A 510-pW 32-kHz Crystal Oscillator With High Energy-to-Noise-Ratio Pulse Injection. *IEEE Journal of Solid-State Circuits*, **2021**, 1-1	5.5	1
3	An Analog-Assisted Digital LDO With Single Subthreshold Output pMOS Achieving 1.44-fs FOM. *IEEE Solid-State Circuits Letters*, **2021**, 4, 154-157	2	0
2	Introduction to the Special Section on Circuits and Systems for Energy-Autonomous Microsystems. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2013**, 60, 825-826	3.5	
1	A 43 nW, 32 kHz, ±4.2 ppm Piecewise Linear Temperature-Compensated Crystal Oscillator With ΔΣ-Modulated Load Capacitance. *IEEE Journal of Solid-State Circuits*, **2022**, 1-1	5.5	