Xing Zhou

List of Publications by Year in descending order

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623188 676716 48 551 14 22 citations g-index h-index papers 48 48 48 415 all docs docs citations times ranked citing authors

#	Article	IF	CITATIONS
1	Enabling Monolithic Heterogeneously Integrated Si/III-V Technology Platform. , 2021, , .		O
2	High-Frequency Characteristics of InGaP/GaAs Double Heterojunction Bipolar Transistor Epitaxially Grown on 200 mm Ge/Si Wafers. IEEE Journal of the Electron Devices Society, 2020, 8, 122-125.	1.2	2
3	Hybrid III–V/Si-CMOS PDK for Monolithic Heterogeneously-Integrated III–V/Si Technology Platforms. , 2020, , .		1
4	Monolithic Co-integration of III-V Materials into Foundry Si-CMOS in a Single Chip for Novel Integrated Circuits. , 2019, , .		0
5	Reduction of Current Collapse in GaN (MIS)-HEMTs Using Dual Material Gate. , 2019, , .		1
6	Monolithic III-V/CMOS Co-integrated Technology, Scalable Compact Modeling, and Hybrid Circuit Design. , 2018, , .		2
7	In0.49Ga0.51P/GaAs heterojunction bipolar transistors (HBTs) on 200 mm Si substrates: Effects of base thickness, base and sub-collector doping concentrations. AIP Advances, 2018, 8, 115132.	0.6	10
8	Impact of Subthreshold Carrier Statistics on the Low-Frequency Noise in MOSFETs. IEEE Transactions on Electron Devices, 2017, 64, 1702-1707.	1.6	2
9	A New Interpretation for the Anomalous Channel-Length Dependence of Low-Frequency Noise in Quasi-Ballistic Transistors. IEEE Electron Device Letters, 2017, 38, 1113-1116.	2.2	O
10	Analytical models for channel potential and drain current in AlGaN/GaN HEMT devices., 2017,,.		1
11	Effect of metal work function on the DC characteristics of an asymmetric MOSFET with Schottky-based source. , 2016, , .		1
12	An on-chip integrated III–V / CMOS 125MSps 6-bit SAR ADC. , 2016, , .		0
13	A Comprehensive Compact Model for GaN HEMTs, Including Quasi-Steady-State and Transient Trap-Charge Effects. IEEE Transactions on Electron Devices, 2016, 63, 1478-1485.	1.6	30
14	Unified regional fermi-potential-based compact model for double heterostructure HEMTs. , 2016, , .		1
15	Unified HEMT/CMOS compact models for future heterogeneous III–V/Si co-integrated technology. , 2016, , .		O
16	Quasi-2D Surface-Potential-Based Critical Length for Drift-Diffusion. IEEE Electron Device Letters, 2016, 37, 1051-1054.	2.2	2
17	GaN HEMT compact model for circuit simulation. , 2015, , .		3
18	Compact electrical/optical model for InGaN/GaN quantum-well based LEDs., 2015, , .		0

#	Article	IF	Citations
19	Compact modeling of III–V/Si FETs. , 2014, , .		О
20	Floating-Body Effect in Partially/Dynamically/Fully Depleted DG/SOI MOSFETs Based on Unified Regional Modeling of Surface and Body Potentials. IEEE Transactions on Electron Devices, 2014, 61, 333-341.	1.6	4
21	Compact Fermi potential model for heterostructure HEMTs with rectangular quantum well. , 2014, , .		4
22	Compact Zero-Temperature Coefficient Modeling Approach for MOSFETs Based on Unified Regional Modeling of Surface Potential. IEEE Transactions on Electron Devices, 2013, 60, 2164-2170.	1.6	4
23	The temperature dependent TCAD and SPICE modeling of AlGaN/GaN HEMTs. , 2013, , .		0
24	Quasi-Ballistic Transport Model for Graphene Field-Effect Transistor. IEEE Transactions on Electron Devices, 2013, 60, 2410-2414.	1.6	11
25	Unified regional modeling of GaN HEMTs with the 2DEG and DD formalism. , 2012, , .		2
26	Unification of MOS compact models with the unified regional modeling approach. Journal of Computational Electronics, 2011, 10, 121-135.	1.3	13
27	Subcircuit Compact Model for Dopant-Segregated Schottky Gate-All-Around Si-Nanowire MOSFETs. IEEE Transactions on Electron Devices, 2010, 57, 772-781.	1.6	25
28	Test Structure for Characterization of Low-Frequency Noise in CMOS Technologies. IEEE Transactions on Instrumentation and Measurement, 2010, 59, 1860-1865.	2.4	12
29	A Compact Model for Undoped Silicon-Nanowire MOSFETs With Schottky-Barrier Source/Drain. IEEE Transactions on Electron Devices, 2009, 56, 1100-1109.	1.6	40
30	Investigation of Low-Frequency Noise in N-Channel FinFETs From Weak to Strong Inversion. IEEE Transactions on Electron Devices, 2009, 56, 2800-2810.	1.6	22
31	Investigation of Low-Frequency Noise in Silicon Nanowire MOSFETs in the Subthreshold Region. IEEE Electron Device Letters, 2009, 30, 668-671.	2.2	43
32	Impact of Gate Electrodes on $\frac{1}{f}$ Noise of Gate-All-Around Silicon Nanowire Transistors. IEEE Electron Device Letters, 2009, 30, 1081-1083.	2.2	24
33	Atomistic modeling of the electrostatic and transport properties ofÂaÂsimplified nanoscale field effect transistor. Journal of Computational Electronics, 2008, 7, 500-508.	1.3	3
34	A Compact Model Satisfying Gummel Symmetry in Higher Order Derivatives and Applicable to Asymmetric MOSFETs. IEEE Transactions on Electron Devices, 2008, 55, 624-631.	1.6	24
35	Rigorous Surface-Potential Solution for Undoped Symmetric Double-Gate MOSFETs Considering Both Electrons and Holes at Quasi NonEquilibrium. IEEE Transactions on Electron Devices, 2008, 55, 616-623.	1.6	31
36	Unified Compact Modeling of Emerging Multiple-Gate MOSFETs., 2007,,.		0

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37	Surface-Potential Solution for Generic Undoped MOSFETs With Two Gates. IEEE Transactions on Electron Devices, 2007, 54, 169-172.	1.6	32
38	Effect of substrate doping on the capacitance-Voltage characteristics of strained-silicon pMOSFETs. IEEE Electron Device Letters, 2006, 27, 62-64.	2.2	17
39	Implicit Analytical Surface/Interface Potential Solutions for Modeling Strained-Si MOSFETs. IEEE Transactions on Electron Devices, 2006, 53, 3110-3117.	1.6	4
40	Physics-Based Single-Piece Charge Model for Strained-Si MOSFETs. IEEE Transactions on Electron Devices, 2005, 52, 1555-1562.	1.6	16
41	Source–Drain Symmetry in Unified Regional MOSFET Model. IEEE Electron Device Letters, 2004, 25, 311-313.	2.2	7
42	The missing link to seamless simulation. IEEE Circuits and Devices: the Magazine of Electronic and Photonic Systems, 2003, 19, 9-17.	0.8	4
43	Unified MOSFET compact I-V model formulation through physics-based effective transformation. IEEE Transactions on Electron Devices, 2001, 48, 887-896.	1.6	22
44	Exploring the novel characteristics of hetero-material gate field-effect transistors (HMGFETs) with gate-material engineering. IEEE Transactions on Electron Devices, 2000, 47, 113-120.	1.6	89
45	A general approach to compact threshold voltage formulation based on 2D numerical simulation and experimental correlation for deep-submicron ULSI technology development [CMOS]. IEEE Transactions on Electron Devices, 2000, 47, 214-221.	1.6	27
46	Numerical investigation of subpicosecond electrical pulse generation by edge illumination of silicon transmission-line gaps. IEEE Journal of Quantum Electronics, 1998, 34, 171-178.	1.0	2
47	Numerical physics of subpicosecond electrical pulse generation by nonuniform gap illumination. IEEE Journal of Quantum Electronics, 1996, 32, 1672-1679.	1.0	8
48	Extraction of physical parameters of strainedsilicon MOSFETs from C-V measurement. , 0, , .		5