Eric A M Klumperink

List of Publications by Year
in descending order

48	2,359	279798	276875
papers	citations	23 h-index	41 g-index

48	48	48	1345
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Low-Power High-Linearity Mixer-First Receiver Using Implicit Capacitive Stacking With 3Ã— Voltage Gain. IEEE Journal of Solid-State Circuits, 2022, 57, 245-259.	5.4	17
2	Figures of Merit for CMOS Low-Noise Amplifiers and Estimates for Their Theoretical Limits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 734-738.	3.0	10
3	2.4-GHz Highly Selective IoT Receiver Front End With Power Optimized LNTA, Frequency Divider, and Baseband Analog FIR Filter. IEEE Journal of Solid-State Circuits, 2021, 56, 2007-2017.	5.4	26
4	Power Efficiency Model for MIMO Transmitters Including Memory Polynomial Digital Predistortion. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1183-1187.	3.0	8
5	Multi-Receiver Cross-Correlation Technique for (B)FSK Radios. IEEE Access, 2021, 9, 96791-96798.	4.2	1
6	A Predistortion-Less Digital Transmitter With â^'50-dB ACLR Exploiting Output Conductance Linearization. IEEE Solid-State Circuits Letters, 2021, 4, 162-165.	2.0	3
7	A 0.7â€“5.7 GHz Reconfigurable MIMO Receiver Architecture for Analog Spatial Notch Filtering Using Orthogonal Beamforming. IEEE Journal of Solid-State Circuits, 2021, 56, 1527-1540.	5.4	12
8	Simplified Harmonic Rejection Mixer Analysis and Design Based on a Filtered Periodic Impulse Model. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2292-2296.	3.0	1
9	Interference Mitigation by Adaptive Analog Spatial Filtering for MIMO Receivers. IEEE Transactions on Microwave Theory and Techniques, 2021, 69, 4169-4179.	4.6	5
10	A Fully Passive RF Front End With 13-dB Gain Exploiting Implicit Capacitive Stacking in a Bottom-Plate N-Path Filter/Mixer. IEEE Journal of Solid-State Circuits, 2020, 55, 1139-1150.	5.4	34
11	Low-Power Highly Selective Channel Filtering Using a Transconductorâ€“Capacitor Analog FIR. IEEE Journal of Solid-State Circuits, 2020, 55, 1785-1795.	5.4	13
12	Analysis of Switched Capacitor Losses in Polar and Quadrature Switched Capacitor PAs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1904-1908.	3.0	5
13	A 0.06â€“3.4-MHz 92-mu W Analog FIR Channel Selection Filter With Very Sharp Transition Band for IoT Receivers. IEEE Solid-State Circuits Letters, 2019, 2, 171-174.	2.0	5
14	A 1-4 GHz 4Ã—4 MIMO Receiver with 4 Reconfigurable Orthogonal Beams for Analog Interference Rejection. , 2019, , .		7
15	Digital-to-Frequency Converters With a DTC: Theoretical Analysis of the Output SFDR. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3761-3774.	5.4	3
16	A Switched Capacitor Digital Sinewave Mixer for Software-Defined Radio. IEEE Solid-State Circuits Letters, 2019, 2, 13-16.	2.0	1
17	High-Linearity Bottom-Plate Mixing Technique With Switch Sharing for <inline-formula> <tex-math notation="LaTeX">N </tex-math> </inline-formula>-path Filters/Mixers. IEEE Journal of Solid-State Circuits, 2019, 54, 323-335.	5.4	38
18	Improving Receiver Close-In Blocker Tolerance by Baseband <inline-formula> <tex-math notation="LaTeX">G_m-C </tex-math> </inline-formula> Notch Filtering. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 885-896.	5.4	10

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19	Feedforward Phase Noise Cancellation Exploiting a Sub-Sampling Phase Detector. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1574-1578.	3.0	9
20	A 2.4-GHz 16-Phase Sub-Sampling Fractional-N PLL With Robust Soft Loop Switching. IEEE Journal of Solid-State Circuits, 2018, 53, 715-727.	5.4	39
21	Enhanced-Selectivity High-Linearity Low-Noise Mixer-First Receiver With Complex Pole Pair Due to Capacitive Positive Feedback. IEEE Journal of Solid-State Circuits, 2018, 53, 1348-1360.	5.4	80
22	Generalized Analysis of High-Order Switch-RC <inline-formula> <tex-math notation="LaTeX">N </tex-math> </inline-formula>-Path Mixers/Filters Using the Adjoint Network. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3267-3278.	5.4	16
23	Analysis of the Effect of Source Capacitance and Inductance on N -Path Mixers and Filters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1469-1480.	5.4	34
24	Beamformer With Constant-Gm Vector Modulators and Its Spatial Intermodulation Distortion. IEEE Journal of Solid-State Circuits, 2017, 52, 735-746.	5.4	28
25	Simplified Unified Analysis of Switched-RC Passive Mixers, Samplers, and N -Path Filters Using the Adjoint Network. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2714-2725.	5.4	31
26	A digital sine-weighted switched-Gm mixer for single-clock power-scalable parallel receivers. , 2017, , .		6
27	Multi-phase sub-sampling fractional-N PLL with soft loop switching for fast robust locking. , 2017, , .		7
28	Compact Cascadable g m -C All-Pass True Time Delay Cell With Reduced Delay Variation Over Frequency. IEEE Journal of Solid-State Circuits, 2015, 50, 693-703.	5.4	100
29	A High-Linearity Digital-to-Time Converter Technique: Constant-Slope Charging. IEEE Journal of Solid-State Circuits, 2015, 50, 1412-1423.	5.4	78
30	RF Transconductor Linearization Robust to Process, Voltage and Temperature Variations. IEEE Journal of Solid-State Circuits, 2015, 50, 2591-2602.	5.4	24
31	Sub-sampling PLL techniques. , 2015, , .		33
32	Analysis of the Signal Transfer and Folding in N-Path Filters With a Series Inductance. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 263-272.	5.4	37
33	Tunable N-Path Notch Filters for Blocker Suppression: Modeling and Verification. IEEE Journal of Solid-State Circuits, 2013, 48, 1370-1382.	5.4	106
34	Using Crosscorrelation to Mitigate Analog/RF Impairments for Integrated Spectrum Analyzers. IEEE Transactions on Microwave Theory and Techniques, 2013, 61, 1327-1337.	4.6	19
35	Widely Tunable 4th Order Switched G$_m$-C Band-Pass Filter Based on N-Path Filters. IEEE Journal of Solid-State Circuits, 2012, 47, 3105-3119.	5.4	114
36	A CMOS spectrum analyzer frontend for cognitive radio achieving +25dBm IIP3 and â^'169 dBm/Hz DANL. , 2012, , .		2

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37	A CMOS-Compatible Spectrum Analyzer for Cognitive Radio Exploiting Crosscorrelation to Improve Linearity and Noise Performance. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 479-492.	5.4	24
38	Improving harmonic rejection for spectrum sensing using crosscorrelation. , 2012, , .		4
39	Tunable High-Q N-Path Band-Pass Filters: Modeling and Verification. IEEE Journal of Solid-State Circuits, 2011, 46, 998-1010.	5.4	368
40	Lowering the SNR Wall for Energy Detection Using Cross-Correlation. IEEE Transactions on Vehicular Technology, 2011, 60, 3748-3757.	6.3	48
41	Spur Reduction Techniques for Phase-Locked Loops Exploiting A Sub-Sampling Phase Detector. IEEE Journal of Solid-State Circuits, 2010, 45, 1809-1821.	5.4	183
42	Unified Frequency-Domain Analysis of Switched-Series-RC Passive Mixers and Samplers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2618-2631.	5.4	122
43	A 300â€“800 MHz Tunable Filter and Linearized LNA Applied in a Low-Noise Harmonic-Rejection RF-Sampling Receiver. IEEE Journal of Solid-State Circuits, 2010, 45, 967-978.	5.4	31
44	Discrete-Time Mixing Receiver Architecture for RF-Sampling Software-Defined Radio. IEEE Journal of Solid-State Circuits, 2010, 45, 1732-1745.	5.4	58
45	A 50Mhz-To-1.5Ghz Cross-Correlation CMOS Spectrum Analyzer for Cognitive Radio with 89dB SFDR in 1Mhz RBW. , 2010, , .		19
46	Jitter Analysis and a Benchmarking Figure-of-Merit for Phase-Locked Loops. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 117-121.	3.0	224
47	A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is Not Multiplied by $N ^{2}$. IEEE Journal of Solid-State Circuits, 2009, 44, 3253-3263.	5.4	282
48	Advantages of Shift Registers Over DLLs for Flexible Low Jitter Multiphase Clock Generation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 244-248.	3.0	34