

Woogeun Rhee

List of Publications by Year in descending order

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170
papers

1,596
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430874

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171
docs citations

171
times ranked

971
citing authors

#	ARTICLE	IF	CITATIONS
1	A 1.1-GHz CMOS fractional-N frequency synthesizer with a 3-b third-order $\Delta\Sigma$ modulator. IEEE Journal of Solid-State Circuits, 2000, 35, 1453-1460.	5.4	187
2	A 10-Gb/s 5-Tap DFE/4-Tap FFE Transceiver in 90-nm CMOS Technology. IEEE Journal of Solid-State Circuits, 2006, 41, 2885-2900.	5.4	182
3	A 6.4-Gb/s CMOS SerDes core with feed-forward and decision-feedback equalization. IEEE Journal of Solid-State Circuits, 2005, 40, 2633-2645.	5.4	136
4	A single-chip quad-band (850/900/1800/1900 MHz) direct conversion GSM/GPRS RF transceiver with integrated VCOs and fractional-n synthesizer. IEEE Journal of Solid-State Circuits, 2002, 37, 1710-1720.	5.4	127
5	An Ultra-Compact Differentially Tuned 6-GHz CMOS LC-VCO With Dynamic Common-Mode Feedback. IEEE Journal of Solid-State Circuits, 2007, 42, 1635-1641.	5.4	58
6	A 13.3 mW 500 Mb/s IR-UWB Transceiver With Link Margin Enhancement Technique for Meter-Range Communications. IEEE Journal of Solid-State Circuits, 2015, 50, 669-678.	5.4	51
7	A Dual-Channel Compass/GPS/GLONASS/Galileo Reconfigurable GNSS Receiver in 65 nm CMOS With On-Chip I/Q Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1720-1732.	5.4	47
8	An FIR-Embedded Noise Filtering Method for $\Delta\Sigma$ Fractional- N PLL Clock Generators. IEEE Journal of Solid-State Circuits, 2009, 44, 2426-2436.	5.4	42
9	Low power sensor design for IoT and mobile healthcare applications. China Communications, 2015, 12, 42-54.	3.2	32
10	A Hybrid Loop Two-Point Modulator Without DCO Nonlinearity Calibration by Utilizing 1 Bit High-Pass Modulation. IEEE Journal of Solid-State Circuits, 2014, 49, 2172-2186.	5.4	30
11	A $\Delta\Sigma$ Fractional-N Synthesizer With Customized Noise Shaping for WCDMA/HSDPA Applications. IEEE Journal of Solid-State Circuits, 2009, 44, 2193-2201.	5.4	26
12	A Gated FM-UWB System With Data-Driven Front-End Power Control. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1348-1358.	5.4	26
13	A Capacitor-Less Ripple-Less Hybrid LDO With Exponential Ratio Array and 4000x Load Current Range. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 36-40.	3.0	26
14	A 3.8-mW 3.5-4-GHz Regenerative FM-UWB Receiver With Enhanced Linearity by Utilizing a Wideband LNA and Dual Bandpass Filters. IEEE Transactions on Microwave Theory and Techniques, 2013, 61, 3350-3359.	4.6	24
15	A 0.42-mW 1-Mb/s 3- to 4-GHz Transceiver in 0.18- μm CMOS With Flexible Efficiency, Bandwidth, and Distance Control for IoT Applications. IEEE Journal of Solid-State Circuits, 2017, 52, 1479-1494.	5.4	24
16	An 18-mW 2.5-GHz/900-MHz BiCMOS dual frequency synthesizer with >10 -Hz RF carrier resolution. IEEE Journal of Solid-State Circuits, 2002, 37, 515-520.	5.4	23
17	Experimental Analysis of Substrate Noise Effect on PLL Performance. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 638-642.	3.0	23
18	A 0.35-0.5-V 18-152 MHz Digitally Controlled Relaxation Oscillator With Adaptive Threshold Calibration in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 736-740.	3.0	23

#	ARTICLE	IF	CITATIONS
37	A Δ Sigma-Based Beamforming Method for Vital Sign Detection Radar Systems. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 932-936.	3.0	8
38	A PSRR Enhancing Method for GRO TDC Based Clock Generation Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 680-688.	5.4	8
39	A 19.2mW 1Gb/s secure proximity transceiver with ISI pre-correction and hysteresis energy detection. , 2016, , .		8
40	Digital LDO with Δ modulation for low-voltage clock generation systems. Electronics Letters, 2016, 52, 2034-2036.	1.0	8
41	A Δ fractional-N synthesizer with customized noise shaping for WCDMA/HSDPA applications. , 2008, , .		7
42	Low power, non invasive UWB systems for WBAN and biomedical applications. , 2010, , .		7
43	9.2 A 13.3mW 500Mb/s IR-UWB transceiver with link-margin enhancement technique for meter-range communications. , 2014, , .		7
44	A 17 mW 3-to-5 GHz Duty-Cycled Vital Sign Detection Radar Transceiver With Frequency Hopping and Time-Domain Oversampling. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 969-980.	5.4	7
45	A 6.5-8.1-GHz Communication/Ranging VWB Transceiver for Secure Wireless Connectivity With Enhanced Bandwidth Efficiency and Δ Energy Detection. IEEE Journal of Solid-State Circuits, 2020, 55, 219-232.	5.4	7
46	A low-cost, leakage-insensitive semi-digital PLL with linear phase detection and FIR-embedded digital frequency acquisition. , 2010, , .		6
47	A Reconfigurable FM-UWB Transceiver for Short-Range Wireless Communications. IEEE Microwave and Wireless Components Letters, 2013, 23, 371-373.	3.2	6
48	A 2 GHz 2 Mb/s Semi-Digital Δ -Point Modulator With Separate FIR-Embedded 1-Bit DCO Modulation in 0.18 μ m CMOS. IEEE Microwave and Wireless Components Letters, 2015, 25, 253-255.	3.2	6
49	Flash ADC-based digital LDO with non-linear decoder and exponential ratio array. Electronics Letters, 2019, 55, 585-587.	1.0	6
50	A Bias-Current-Free Fractional-N Hybrid PLL for Low-Voltage Clock Generation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3611-3620.	5.4	6
51	All-Digital Dynamic Self-Detection and Self-Compensation of Static Phase Offsets in Charge-Pump PLLs. , 2007, , .		5
52	A 2.4 GHz 6.6 mA fully differential CMOS PLL frequency synthesiser. International Journal of Electronics, 2009, 96, 1039-1056.	1.4	5
53	A low data rate FM-UWB transmitter with-based sub-carrier modulation and quasi-continuous frequency-locked loop. , 2010, , .		5
54	A 1Mb/s 3.2-4.4GHz reconfigurable FM-UWB transmitter in 0.18 μ m CMOS. , 2011, , .		5

#	ARTICLE	IF	CITATIONS
55	A power-efficient all-digital IR-UWB transmitter with configurable pulse shaping by utilizing a digital amplitude modulation technique. , 2012, , .		5
56	A 5GHz 200kHz/5000ppm Spread-Spectrum Clock Generator with Calibration-Free Two-Point Modulation Using a Nested-Loop BBPLL. , 2019, , .		5
57	A 3.7-mW 2.4-GHz Phase-Tracking GFSK Receiver With BBPLL-Based Demodulation. IEEE Journal of Solid-State Circuits, 2019, 54, 336-345.	5.4	5
58	A Fractional-N PLL for Digital Clock Generation With an FIR-Embedded Frequency Divider. , 2007, , .		4
59	A relaxation oscillator with multi-phase triangular waveform generation. , 2011, , .		4
60	A 0.65V 1.2mW 2.4GHz/400MHz dual-mode phase modulator for mobile healthcare applications. , 2014, , .		4
61	A 0.6V 50-to-145MHz PVT tolerant digital PLL with DCO-dedicated $\hat{\nu}$ LDO and temperature compensation circuits in 65nm CMOS. , 2017, , .		4
62	Energy-efficient proprietary transceivers for IoT and smartphone-based WPAN. , 2017, , .		4
63	A 5-mW 750-kb/s Noninvasive Transceiver for Around-the-Head Audio Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 196-200.	3.0	4
64	A Secure TOF-Based Transceiver with Low Latency and sub-cm Ranging for Mobile Authentication Applications. , 2018, , .		4
65	A VCO-dedicated digital LDO with multi-comparator coarse loop and 1-bit $\hat{\nu}$ fine loop for robust frequency generation. , 2018, , .		4
66	A Noise and Spur Reduction Technique for $\hat{\nu}$ Fractional-N Bang-Bang PLLs with Embedded Phase Domain Filtering. , 2019, , .		4
67	A Low-Spur Current-Biasing-Free Fractional-N Hybrid PLL for Low-Voltage Clock Generation. , 2020, , .		4
68	Low-noise fractional-N PLL design with mixed-mode triple-input LC VCO in 65nm CMOS. , 2010, , .		3
69	Reconfigurable, spectrally efficient, high data rate IR-UWB transmitter design using a Δ PLL driven ILO and a 7-tap FIR filter. , 2011, , .		3
70	A 2.74–5.37GHz boosted-gain type-I PLL with &#60;15% loop filter area. , 2012, , .		3
71	Design and analysis of a robust all-digital clock generation system with a DLL-based TDC. , 2012, , .		3
72	A high efficiency robust IR-UWB receiver design for high data rate CM-range communications. , 2014, , .		3

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73	A 7.6mW 2Gb/s proximity transmitter for smartphone-mirrored display applications. , 2015, , .		3
74	A 0.55V 100MHz ADPLL with $\hat{\Gamma}$ LDO and Relaxation DCO in 65nm CMOS. , 2015, , .		3
75	A 6.5mW, wide band dual-path LC VCO design with mode switching technique in 130nm CMOS. , 2015, , .		3
76	A 1.9mW 750kb/s 2.4GHz F-OOK transmitter with symmetric FM template and high-point modulation PLL. , 2016, , .		3
77	10Mbps 0.3nJ/bit OQPSK transceiver IC for 400-450MHz medical telemetry. Electronics Letters, 2016, 52, 1830-1832.	1.0	3
78	Design and Analysis of DTC-Free $\hat{\Gamma}$ Bang-Bang Phase-Locked Loops. , 2021, , .		3
79	Experimental analysis of the effect of substrate noise on PLL performance. , 0, , .		2
80	A hybrid spur compensation technique for finite-modulo fractional-N phase-locked loops. , 2008, , .		2
81	A semi-digital cascaded CDR with fast phase acquisition and adaptive resolution control. , 2010, , .		2
82	A latency-proof quantization noise reduction method for digitally-controlled ring oscillators. , 2010, , .		2
83	A digitally reconfigurable auto amplitude calibration method for wide tuning range VCO design. , 2010, , .		2
84	Reconfigurable FM-UWB transmitter design for robust short range communications. Telecommunication Systems, 2013, 52, 1133.	2.5	2
85	A wide-tuning quasi-type-I PLL with voltage-mode frequency acquisition aid. , 2011, , .		2
86	A 9.6Gb/s 5+1-lane source synchronous transmitter in 65nm CMOS technology. , 2012, , .		2
87	A pulse-shaped power amplifier with dynamic bias switching for IR-UWB transmitters. , 2012, , .		2
88	A 3.8mW, 3.5-4GHz regenerative FM-UWB receiver with enhanced linearity by utilizing a wideband LNA and dual bandpass filters. , 2012, , .		2
89	Algorithm-Based Countermeasures against Power Analysis Attacks for Public-Key Cryptography SM2. , 2014, , .		2
90	A 3.5-4GHz FMCW radar transceiver design with phase-domain oversampled ranging by utilizing a 1-bit $\hat{\Gamma}$ TDC. , 2014, , .		2

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91	A 1.5GHz all-digital frequency-locked loop with 1-bit ΔΣ frequency detection in 0.18μm CMOS. , 2014, , .		2
92	A 4.8-mW/Gb/s 9.6-Gb/s 5 – – – notation="TeX"⟩⟩⟩ 1-Lane Source-Synchronous Transmitter in 65-nm Bulk CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 209-213.	3.0	2
93	A digital-intensive F/PLL-based two-point modulator with a constant-gain DCO for linear FMCW generation. , 2015, , .		2
94	A delta-sigma-based transmitter utilizing FIR-embedded digital power amplifiers. , 2015, , .		2
95	A 10 Mb/s hybrid two-point modulator with front-end phase selection and dual-path DCO modulation. , 2015, , .		2
96	A multi-bit FIR filtering technique for two-point modulators with dedicated digital high-pass modulation path. , 2015, , .		2
97	A 0.5mW 1Mb/s multi-channel chirp-UWB transmitter with burst-mode transmission and optimized digital gradient. , 2016, , .		2
98	A 10.3mW 13.6GHz phase-locked loop with boosted Gm two-stage ring VCO. , 2016, , .		2
99	20-Mb/s GFSK Modulator Based on 3.6-GHz Hybrid PLL With 3-b DCO Nonlinearity Calibration and Independent Delay Mismatch Control. IEEE Transactions on Microwave Theory and Techniques, 2017, 65, 2387-2398.	4.6	2
100	A 6.1mW 5Mb/s 2.4GHz transceiver with F-OOK modulation for high bandwidth and energy efficiencies. , 2017, , .		2
101	A 77-GHz mixed-mode FMCW signal generator based on bang-bang phase detector. , 2017, , .		2
102	A 6-8GHZ 200MHz Bandwidth 9-Channel VWB Transceiver with 8 Frequency-Hopping Subbands. , 2018, , .		2
103	A $\hat{\mu}$ DPLL with 1b TDC, 4b DTC and 8-tap FIR filter for low-voltage clock generation/modulation systems. , 2018, , .		2
104	A Gaussian-Filtered Fully-Balanced FSK Modulator with Integer-N PLL Based 1+-Point Modulation. , 2019, , .		2
105	Frequency-Domain Modeling and Analysis of Injection-Locked Oscillators. IEEE Journal of Solid-State Circuits, 2019, , 1-14.	5.4	2
106	A 1Mb/s 2.86% EVM GFSK Modulator Based on $\hat{\mu}$ BB-DPLL without Background Digital Calibration. , 2020, , .		2
107	A 3.5-GHz 0.24-nj/b 100-Mb/s Fully Balanced FSK Receiver With Sideband Energy Detection. IEEE Solid-State Circuits Letters, 2021, 4, 26-29.	2.0	2
108	Customized zero frequency control for hybrid FIR noise filtering in ΣΔ fractional-N PLL. , 2009, , .		1

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109	Continuously auto-tuned and self-ranged dual-path PLL design with hybrid AFC. , 2011, , .		1
110	A ΔΣ IR-UWB radar with sub-mm ranging capability for human body monitoring systems. , 2012, , .		1
111	A PVT-insensitive self-dithered TDC design by utilizing a ΔΣ DLL. , 2012, , .		1
112	A 5.2–1.8MHz octa-phase relaxation oscillator for 8-PSK FM-UWB transceiver systems. , 2013, , .		1
113	A PLL/DLL based CDR with ΔΣ frequency tracking and low algorithmic jitter generation. , 2013, , .		1
114	A 1.6Mb/s 3.75–4.25GHz chirp-UWB transceiver with enhanced spectral efficiency in 0.18μm CMOS. , 2014, , .		1
115	A chirp-UWB transceiver with embedded bulk PPM for energy efficient data transmission. , 2014, , .		1
116	A 3.1–4.8-GHz delay-line-based frequency-hopping IR-UWB transmitter in 65-NM CMOS technology. , 2014, , .		1
117	Phase-locked frequency synthesis and modulation for modern wireless transceivers. , 2015, , .		1
118	A 2.4 GHz two-point $\hat{\Gamma}$ - $\hat{\Gamma}$ modulator with gain calibration and AFC for WPAN/BAN applications. , 2015, , .		1
119	A high-PSRR ADPLL with self-regulated GRO TDC and DCO-dedicated voltage regulator. , 2015, , .		1
120	A digital power amplifier with FIR-embedded 1-Bit high-order ΔΣ modulation for WBAN polar transmitters. , 2015, , .		1
121	2.4GHz 20Mb/s FSK receiver front-end and transmitter modulation PLL design for energy-efficient short-range communicaiton. , 2016, , .		1
122	A 13.5mW 4Gb/s Filter-less UWB Transmitter for High Data Rate Mobile Applications. , 2018, , .		1
123	A 26.6mW 1Gb/s dual-antenna wideband receiver with auto beam steering for secure proximity communications. , 2018, , .		1
124	Design and Analysis of Data-Pattern-Insensitive Phase-Tracking Receivers with Fully-Balanced FSK Modulation. , 2019, , .		1
125	A Sub-10fs FOM, 5000x Load Driving Capacity and 5mV Output Ripple Digital LDO with Dual-Mode Nonlinear Voltage Detector and Dead-Zone Charge Pump Loop. , 2020, , .		1
126	A 5.4GHz $\hat{\Gamma}$ - $\hat{\Gamma}$ Bang-Bang PLL with 19dB In-Band Noise Reduction by Using a Nested PLL Filter. , 2020, , .		1

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127	A 13-bit 312.5-MS/s Pipelined SAR ADC with Integrator-type Residue Amplifier and Inter-stage Gain Stabilization Technique. , 2020, , .		1
128	A Correlation-based Timing Skew Calibration Strategy Using a Time-Interleaved Reference ADC. , 2020, , .		1
129	A Quantization Noise Reduction Method for Delta-Sigma Fractional-N PLLs Using Cascaded Injection-Locked Oscillators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2448-2452.	3.0	1
130	A 7.25-7.75GHz 5.9mW UWB Transceiver with -23.8dBm NBI Tolerance and 1.5cm Ranging Accuracy Using Uncertain IF and Pulse-Triggered Envelope/Energy Detection. , 2022, , .		1
131	A low-cost, multi-standard Δ∑ fractional-N synthesizer design for WiMAX/WLAN applications. , 2009, , .		0
132	A 0.4-to-1.6GHz low-OSR ΔΣ DLL with self-referenced multiphase generation. , 2009, , .		0
133	Transient analysis of nonlinear settling behavior in charge-pump phase-locked loop design. , 2009, , .		0
134	A 65nm CMOS 3.6GHz fractional-N PLL with 5th-order ΔΣ modulation and weighted FIR filtering. , 2009, , .		0
135	Power and jitter optimized VCO design using an on-chip supply noise monitoring circuit. , 2010, , .		0
136	A — 131dBc@1M PhaseNoise, 74% spectral efficiency, GA optimized FIR impulse radio UWB transmitter. , 2010, , .		0
137	Reconfigurable, fast AFC technique using code estimation and binary search algorithm for 0.2–6GHz software-defined radio frequency synthesis. , 2010, , .		0
138	Technology-friendly phase-locked loops. , 2011, , .		0
139	Fractional-N frequency synthesis: Overview and design perspectives. , 2011, , .		0
140	Semidigital PLL Design for Low-Cost Low-Power Clock Generation. Journal of Electrical and Computer Engineering, 2011, 2011, 1-9.	0.9	0
141	Clock/Frequency Generation Circuits and Systems. Journal of Electrical and Computer Engineering, 2012, 2012, 1-2.	0.9	0
142	Introduction to the Special Section on the 2011 Asian Solid-State Circuits Conference (A-SSCC). IEEE Journal of Solid-State Circuits, 2012, 47, 2551-2553.	5.4	0
143	A C<inf>int</inf>-less type-II PLL with ΔΣ DAC based frequency acquisition and reduced quantization noise. , 2012, , .		0
144	An 11.7–17.2GHz digitally-controlled oscillator in 65nm CMOS for high-band UWB applications. , 2012, , .		0

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145	An FM-UWB transceiver with M-PSK subcarrier modulation and regenerative FM demodulation. , 2013, , .		0
146	Introduction to the Special Section on the 2012 Asian Solid-State Circuits Conference (A-SSCC). IEEE Journal of Solid-State Circuits, 2013, 48, 2579-2581.	5.4	0
147	A 2.5–4.5 GHz CMOS fast settling PLL for IR-UWB radar applications. , 2014, , .		0
148	A 2.5GHz ADPLL with PVT-insensitive ΔΣ dithered time-to-digital conversion by utilizing an ADDLL. , 2014, , .		0
149	A Mixed Voltage Bidirectional I/O IP corewith low power modification for automotive BCM SoC. , 2014, , .		0
150	A second-order multi-bit ΔΣ TDC for high resolution IR-UWB radar systems. , 2014, , .		0
151	An overview of digital-intensive $\Sigma\Delta$ phase-locked loops utilizing 1-bit conversion and modulation. , 2016, , .		0
152	A 0.3mW 1Mb/s high security proximity UWB transmitter with frequency/time-domain scrambling. , 2016, , .		0
153	A 1.8mW 2Mb/s chirp-UWB transceiver with burst-mode transmission and slope-based detection. , 2016, , .		0
154	A hybrid frequency/phase-locked loop for versatile clock generation with wide reference frequency range. , 2016, , .		0
155	Session 15 "Energy-efficient wireless for 5G and IoT. , 2017, , .		0
156	An energy/bandwidth/area efficient frequency-domain OOK transmitter with phase rotated modulation. , 2017, , .		0
157	A fractional-NBB-DPLL with auto-tuned DTC and FIR filter for noise and spur reduction. , 2017, , .		0
158	A 1-GHz 1.6-mW Auto-Calibrated Bit Slicer for Energy/Envelope Detection Receivers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 587-591.	3.0	0
159	A 120 pJ/bit $\Delta\Sigma$ -Based 2.4-GHz Transmitter Using FIR-Embedded Digital Power Amplifier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1854-1858.	3.0	0
160	A 9mW 6-9GHz 2.5Gb/s Proximity Transmitter with Combined OOK/BPSK Modulation for Low Power Mobile Connectivity. , 2019, , .		0
161	A BBPLL-Based Demodulator with Multiphase and Feedforward Linearization Methods for Phase-Tracking Receivers. , 2019, , .		0
162	A 100Mb/s 3.5GHz Fully-Balanced BFOOK Modulator Based on Integer-N Hybrid PLL. , 2019, , .		0

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163	Enhanced FIR-embedded noise reduction method with hybrid phase detection for semidigital fractional-N phase-locked loops. , 2019, , .		0
164	A 6-8GHz Multichannel Reconfigurable Pulse-Based Transceiver with 3.5ns Processing Latency and 1cm Ranging Accuracy for Secure Wireless Connectivity. , 2020, , .		0
165	A 2.4-GHz Crystal-Less GFSK Receiver Using an Auxiliary Multiphase BBPLL for Digital Output Demodulation With Enhanced Frequency Scaling. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1143-1147.	3.0	0
166	A Two-Point Modulation Spread-Spectrum Clock Generator With FIR-Embedded Binary Phase Detection and 1-Bit High-Order $\hat{\mu}$ Modulation. Journal of Semiconductor Technology and Science, 2016, 16, 425-435.	0.4	0
167	A 7.6 mW 2 Gb/s Proximity Transmitter for Smartphone-Mirrored Display Applications. Journal of Semiconductor Technology and Science, 2016, 16, 415-424.	0.4	0
168	A Nonlinearity-Calibration-Free Reconfigurable ADPLL for General Purpose Frequency Modulation. , 2020, , .		0
169	A 0.0048mm ² 0.43-to-1.0V 0.54-to-1.76GHz Bias-Current-Free PLL in 14nm FinFET CMOS. , 2021, , .		0
170	A 0.14nJ/b 200Mb/s Quasi-Balanced FSK Transceiver with Closed-Loop Modulation and Sideband Energy Detection. , 2022, , .		0