

Yung-Yueh Chiu

List of Publications by Year in descending order

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19
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citing authors

#	ARTICLE	IF	CITATIONS
1	A unified 3D device simulation of random dopant, interface trap and work function fluctuations on high- κ /metal gate device. , 2011, , .		19
2	New Method to Analyze the Shift of Floating Gate Charge and Generated Tunnel Oxide Trapped Charge Profile in NAND Flash Memory by Program/Erase Endurance. IEEE Transactions on Electron Devices, 2015, 62, 114-120.	3.0	16
3	Transconductance Distribution in Program/Erase Cycling of NAND Flash Memory Devices: a Statistical Investigation. IEEE Transactions on Electron Devices, 2019, 66, 1255-1261.	3.0	8
4	Interface traps and random dopants induced characteristic fluctuations in emerging MOSFETs. Microelectronic Engineering, 2011, 88, 1269-1271.	2.4	7
5	Evaluation of the Role of Deep Trap State Using Analytical Model in the Program/Erase Cycling of NAND Flash Memory and Its Process Dependence. IEEE Transactions on Electron Devices, 2018, 65, 499-506.	3.0	6
6	Impact of Program/Erase Cycling Interval on the Transconductance Distribution of NAND Flash Memory Devices. IEEE Transactions on Electron Devices, 2020, 67, 4897-4903.	3.0	4
7	Technique for Profiling the Cycling-Induced Oxide Trapped Charge in NAND Flash Memories. Electronics (Switzerland), 2021, 10, 2492.	3.1	4
8	Dual-Material Gate Approach to Suppression of Random-Dopant-Induced Characteristic Fluctuation in 16 nm Metal- ϵ -Oxide- ϵ -Semiconductor Field-Effect-Transistor Devices. Japanese Journal of Applied Physics, 2011, 50, 04DC07.	1.5	3
9	Impact of String Pattern on the Threshold-Voltage Spread of Program-Inhibited Cell in NAND Flash. IEEE Journal of the Electron Devices Society, 2016, 4, 174-178.	2.1	3
10	Simulation Study of the Instability Induced by the Variation of Grain Boundary Width and Trap Density in Gate-All-Around Polysilicon Transistor. IEEE Transactions on Electron Devices, 2021, 68, 1969-1974.	3.0	3
11	The origin of oxide degradation during time interval between program/erase cycles in NAND Flash memory devices. Japanese Journal of Applied Physics, 0, , .	1.5	3
12	Correlation between interface traps and random dopants in emerging MOSFETs. , 2011, , .		2
13	3D simulation of electrical characteristic fluctuation induced by interface traps at Si/high- κ /oxide interface and random dopants in 16-nm-Gate CMOS devices. , 2011, , .		2
14	Random interface-traps-induced characteristic fluctuation in 16-nm high- κ /metal gate CMOS device and SRAM circuit. , 2011, , .		2
15	Electrical characteristic fluctuation of 16 nm MOSFETs induced by random dopants and interface traps. , 2011, , .		2
16	Characterization of the charge trapping properties in p-channel silicon- ϵ -oxide- ϵ -nitride- ϵ -oxide- ϵ -silicon memory devices including SiO ₂ /Si ₃ N ₄ interfacial transition layer. Japanese Journal of Applied Physics, 2015, 54, 104201.	1.5	2
17	DC/AC characteristic fluctuations induced by interface traps and random dopants of high- κ /metal-gate devices. , 2011, , .		0
18	Study Trapped Charge Distribution in P-Channel Silicon- ϵ -Oxide- ϵ -Nitride- ϵ -Oxide- ϵ -Silicon Memory Device Using Dynamic Programming Scheme. Japanese Journal of Applied Physics, 2013, 52, 04CD01.	1.5	0

#	ARTICLE	IF	CITATIONS
19	The effect of hydrogen on programmed threshold-voltage distribution in NAND flash memories. Japanese Journal of Applied Physics, 2019, 58, 081002.	1.5	0