Huazhong Yang

List of Publications by Citations

248 papers	3,165 citations	25 h-index	49 g-index
329 ext. papers	4,378 ext. citations	2.6 avg, IF	5.5 L-index

#	Paper	IF	Citations
248	Going Deeper with Embedded FPGA Platform for Convolutional Neural Network **2016**,		550
247	Angel-Eye: A Complete Design Flow for Mapping CNN Onto Embedded FPGA. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 35-47	2.5	216
246	Accurate Temperature-Dependent Integrated Circuit Leakage Power Estimation is Easy **2007**,		111
245	**2017**,		84
244	Technological Exploration of RRAM Crossbar Array for Matrix-Vector Multiplication. *Journal of Computer Science and Technology*, **2016**, 31, 3-19	1.7	78
243	Thermal vs Energy Optimization for DVFS-Enabled Processors in Embedded Systems **2007**,		73
242	RRAM-Based Analog Approximate Computing. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 1905-1917	2.5	69
241	Region ensemble network: Improving convolutional network for hand pose estimation **2017**,		65
240	Storage-Less and Converter-Less Photovoltaic Energy Harvesting With Maximum Power Point Tracking for Internet of Things. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 173-186	2.5	58
239	**2018**,		57
238	FPGP **2016**,		53
237	ForeGraph **2017**,		50
236	Stuck-at Fault Tolerance in RRAM Computing Systems. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2018**, 8, 102-115	5.2	46
235	**2016**,		43
234	A global and updatable ECG beat classification system based on recurrent neural networks and active learning. *Information Sciences*, **2019**, 501, 523-542	7.7	42
233	Storage-less and converter-less maximum power point tracking of photovoltaic cells for a nonvolatile microprocessor **2014**,		40
232	A Deep Learning Approach for Blind Drift Calibration of Sensor Networks. *IEEE Sensors Journal*, **2017**, 17, 4158-4171	4	38

231	NICSLU: An Adaptive Sparse Matrix Solver for Parallel Circuit Simulation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 261-274	2.5	37
230	GPU-Accelerated Sparse LU Factorization for Circuit Simulation with Performance Modeling. *IEEE Transactions on Parallel and Distributed Systems*, **2015**, 26, 786-795	3.7	34
229	PaCC: A Parallel Compare and Compress Codec for Area Reduction in Nonvolatile Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 1491-1505	2.6	33
228	GraphH: A Processing-in-Memory Architecture for Large-Scale Graph Processing. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 640-653	2.5	33
227	TIME: A Training-in-Memory Architecture for RRAM-Based Deep Neural Networks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 834-847	2.5	32
226	Angel-Eye: A Complete Design Flow for Mapping CNN onto Customized Hardware **2016**,		27
225	. *IEEE Journal of Solid-State Circuits*, **2017**, 52, 2194-2207	5.5	26
224	A Configurable Multi-Precision CNN Computing Framework Based on Single Bit RRAM **2019**,		25
223	Solar Power Prediction Assisted Intra-task Scheduling for Nonvolatile Sensor Nodes. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 724-737	2.5	24
222	An EScheduler-Based Data Dependence Analysis and Task Scheduling for Parallel Circuit Simulation. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2011**, 58, 702-706	3.5	24
221	A Ferroelectric Nonvolatile Processor with 46 $mu $ s System-Level Wake-up Time and 14 $mu $ s Sleep Time for Energy Harvesting Applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2017**, 64, 596-607	3.9	23
220	MSP-MFCC: Energy-Efficient MFCC Feature Extraction Method With Mixed-Signal Processing Architecture for Wearable Speech Recognition Applications. *IEEE Access*, **2020**, 8, 48720-48730	3.5	20
219	Hardware Trojan Detection in Third-Party Digital Intellectual Property Cores by Multilevel Feature Analysis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1370-1383	2.5	20
218	Spread spectrum audio watermarking based on perceptual characteristic aware extraction. *IET Signal Processing*, **2016**, 10, 266-273	1.7	20
217	An Investigation on Ground Electrodes of Capacitive Coupling Human Body Communication. *IEEE Transactions on Biomedical Circuits and Systems*, **2017**, 11, 910-919	5.1	19
216	FPGA and GPU implementation of large scale SpMV **2010**,		19
215	Computation-oriented fault-tolerance schemes for RRAM computing systems **2017**,		17
214	A Tissue-Channel Transcutaneous Power Transfer Technique for Implantable Devices. *IEEE Transactions on Power Electronics*, **2018**, 33, 9753-9761	7.2	17

213	Modeling Random Telegraph Noise as a Randomness Source and its Application in True Random Number Generation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1435-1448	2.5	17
212	Hu-Fu: Hardware and Software Collaborative Attack Framework Against Neural Networks **2018**,		17
211	A 14 Bit 500 MS/s CMOS DAC Using Complementary Switched Current Sources and Time-Relaxed Interleaving DRRZ. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 2337-2347	3.9	17
210	A 12-bit self-calibrating SAR ADC achieving a Nyquist 90.4-dB SFDR. *Analog Integrated Circuits and Signal Processing*, **2013**, 74, 239-254	1.2	17
209	Modeling the Impact of Process Variation on Critical Charge Distribution **2006**,		17
208	Blind Drift Calibration of Sensor Networks Using Sparse Bayesian Learning. *IEEE Sensors Journal*, **2016**, 1-1	4	17
207	Long live TIME **2018**,		17
206	An energy efficient backup scheme with low inrush current for nonvolatile SRAM in energy harvesting sensor nodes **2015**,		16
205	A General Framework for Hardware Trojan Detection in Digital Circuits by Statistical Learning Algorithms. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1633-1646	2.5	15
204	Design of 2T/Cell and 3T/Cell Nonvolatile Memories with Emerging Ferroelectric FETs. *IEEE Design and Test*, **2019**, 36, 39-45	1.4	15
203	A Five-Tissue-Layer Human Body Communication Circuit Model Tunable to Individual Characteristics. *IEEE Transactions on Biomedical Circuits and Systems*, **2018**, 12, 303-312	5.1	15
202	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 1414-1427	2.5	15
201	NS-CIM: A Current-Mode Computation-in-Memory Architecture Enabling Near-Sensor Processing for Intelligent IoT Vision Nodes. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 2909-2922	3.9	14
200	Instruction driven cross-layer CNN accelerator with winograd transformation on FPGA **2017**,		14
199	Large depth-of-field 3D shape measurement using an electrically tunable lens. *Optics Express*, **2019**, 27, 29697-29709	3.3	14
198	STICKER: An Energy-Efficient Multi-Sparsity Compatible Accelerator for Convolutional Neural Networks in 65-nm CMOS. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 465-477	5.5	14
197	Exploring the Precision Limitation for RRAM-Based Analog Approximate Computing. *IEEE Design and Test*, **2016**, 33, 51-58	1.4	13
196	A Self-Adaptive Capacitive Compensation Technique for Body Channel Communication. *IEEE Transactions on Biomedical Circuits and Systems*, **2017**, 11, 1001-1012	5.1	13

195	An analytical phase noise model of charge pump mismatch in sigma-delta frequency synthesizer. *Analog Integrated Circuits and Signal Processing*, **2006**, 48, 223-229	1.2	13
194	MNSIM: Simulation Platform for Memristor-Based Neuromorphic Computing System. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 1-1	2.5	12
193	Performance analysis of data hiding in MPEG-4 AAC audio. *Tsinghua Science and Technology*, **2009**, 14, 55-61	3.4	12
192	High Speed Soft-Error-Tolerant Latch and Flip-Flop Design for Multiple VDD Circuit **2007**,		12
191	Processing Near Sensor Architecture in Mixed-Signal Domain With CMOS Image Sensor of Convolutional-Kernel-Readout Method. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 389-400	3.9	12
190	Lowering Area Overheads for FeFET-Based Energy-Efficient Nonvolatile Flip-Flops. *IEEE Transactions on Electron Devices*, **2018**, 65, 2670-2674	2.9	11
189	Intra-task scheduling for storage-less and converter-less solar-powered nonvolatile sensor nodes **2014**,		11
188	A Generic Graph-Based Neural Architecture Encoding Scheme for Predictor-Based NAS. *Lecture Notes in Computer Science*, **2020**, 189-204	0.9	11
187	Demystifying and Mitigating Code-Dependent Switching Distortions in Current-Steering DACs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 68-81	3.9	11
186	The Role and Challenges of Body Channel Communication in Wearable Flexible Electronics. *IEEE Transactions on Biomedical Circuits and Systems*, **2020**, 14, 283-296	5.1	10
185	Design exploration of inrush current aware controller for nonvolatile processor **2015**,		10
184	Application of DAPSK in HF communications. *IEEE Communications Letters*, **2005**, 9, 613-615	3.8	10
183	FTT-NAS: Discovering Fault-Tolerant Neural Architecture **2020**,		9
182	A 3.77TOPS/W Convolutional Neural Network Processor With Priority-Driven Kernel Optimization. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 277-281	3.5	9
181	FPGA based memory efficient high resolution stereo vision system for video tolling **2012**,		9
180	Design methodology of variable latency adders with multistage function speculation **2010**,		9
179	A New Family of Sequential Elements With Built-in Soft Error Tolerance for Dual-VDD Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2008**, 16, 1372-1384	2.6	9
178	Autofocusing method for high-resolution three-dimensional profilometry. *Optics Letters*, **2020**, 45, 375	3	9

177	DSA: More Efficient Budgeted Pruning via Differentiable Sparsity Allocation. *Lecture Notes in Computer Science*, **2020**, 592-607	0.9	9
176	A Multi-accuracy-Level Approximate Memory Architecture Based on Data Significance Analysis **2016**,		9
175	A 130-nm Ferroelectric Nonvolatile System-on-Chip With Direct Peripheral Restore Architecture for Transient Computing System. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 885-895	5.5	9
174	PAGANI Toolkit: Parallel graph-theoretical analysis package for brain network big data. *Human Brain Mapping*, **2018**, 39, 1869-1885	5.9	8
173	A blind audio watermarking algorithm by logarithmic quantization index modulation. *Multimedia Tools and Applications*, **2014**, 71, 1157-1177	2.5	8
172	Design of Signal Constellations in the Presence of Phase Noise **2008**,		8
171	Guided, Fusion-Based, Large Depth-of-field 3D Imaging Using a Focal Stack. *Sensors*, **2019**, 19,	3.8	8
170	Approximate Computing in Chrominance Cache for Image/Video Processing **2015**,		7
169	**2014**,		7
168	A 65-nm ReRAM-Enabled Nonvolatile Processor With Time-Space Domain Adaption and Self-Write-Termination Achieving $> 4times $ Faster Clock Frequency and $> 6times $ Higher Restore Speed. *IEEE Journal of Solid-State Circuits*, **2017**, 52, 2769-2785	5.5	7
167	Drift detection and calibration of sensor networks **2015**,		7
166	Exploration of Electrical and Novel Optical Chip-to-Chip Interconnects. *IEEE Design and Test*, **2014**, 31, 28-35	1.4	7
165	An adaptive LU factorization algorithm for parallel circuit simulation **2012**,		7
164	A Sparse-Adaptive CNN Processor with Area/Performance balanced N-Way Set-Associate PE Arrays Assisted by a Collision-Aware Scheduler **2019**,		7
163	**2018**,		7
162	NS-FDN: Near-Sensor Processing Architecture of Feature-Configurable Distributed Network for Beyond-Real-Time Always-on Keyword Spotting. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 1-14	3.9	7
161	All-Digital Galvanically-Coupled BCC Receiver Resilient to Frequency Misalignment. *IEEE Transactions on Biomedical Circuits and Systems*, **2017**, 11, 714-726	5.1	6
160	A 14-bit 1.0-GS/s dynamic element matching DAC with >80 dB SFDR up to the Nyquist **2015**,		6

159	Soft Error Mitigation for Deep Convolution Neural Network on FPGA Accelerators **2020**,		6
158	CNN-based Feature-point Extraction for Real-time Visual SLAM on Embedded FPGA **2020**,		6
157	Long Live TIME: Improving Lifetime and Security for NVM-Based Training-in-Memory Systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 4707-4720	2.5	6
156	Lightweight Precision-Adaptive Time Synchronization in Wireless Sensor Networks. *IEICE Transactions on Communications*, **2010**, E93-B, 2299-2308	0.5	6
155	Low Voltage Low Power Class-AB OTA with Negative Resistance Load **2006**,		6
154	Noise Margin Modeling for Zero- $V_{text {GS}}$ Load TFT Circuits and Yield Estimation. *IEEE Transactions on Electron Devices*, **2016**, 63, 684-690	2.9	6
153	MACSen: A Processing-In-Sensor Architecture Integrating MAC Operations Into Image Sensor for Ultra-Low-Power BNN-Based Intelligent Visual Perception. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 627-631	3.5	6
152	Noise Margin, Delay, and Power Model for Pseudo-CMOS TFT Logic Circuits. *IEEE Transactions on Electron Devices*, **2017**, 64, 2635-2642	2.9	5
151	Dynamic Channel Modeling and OFDM System Analysis for Capacitive Coupling Body Channel Communication. *IEEE Transactions on Biomedical Circuits and Systems*, **2019**, 13, 735-745	5.1	5
150	Efficient region-aware P/G TSV planning for 3D ICs **2014**,		5
149	MDCT Sinusoidal Analysis for Audio Signals Analysis and Processing. *IEEE Transactions on Audio Speech and Language Processing*, **2013**, 21, 1403-1414		5
148	CORAL: Coarse-grained reconfigurable architecture for Convolutional Neural Networks **2017**,		5
147	AICNN: Implementing Typical CNN Algorithms with Analog-to-Information Conversion Architecture **2017**,		5
146	Robust and transparent audio watermarking based on improved spread spectrum and psychoacoustic masking **2012**,		5
145	An energy efficient fully integrated OOK transceiver SoC for wireless body area networks **2013**,		5
144	Making Human Connectome Faster: GPU Acceleration of Brain Network Analysis **2010**,		5
143	A 250KS/s, 0.8V ultra low power successive approximation register ADC using a Dynamic rail-to-rail comparator. *IEICE Electronics Express*, **2010**, 7, 261-267	0.5	5
142	A precision adaptive average time synchronization protocol in wireless sensor networks **2008**,		5

141	FeFET-based low-power bitwise logic-in-memory with direct write-back and data-adaptive dynamic sensing interface **2020**,		5
140	Temperature-Aware NBTI Modeling Techniques in Digital Circuits. *IEICE Transactions on Electronics*, **2009**, E92-C, 875-886	0.4	5
139	Enabling Efficient and Flexible FPGA Virtualization for Deep Learning in the Cloud **2020**,		5
138	CMOS Image Sensor Data-Readout Method for Convolutional Operations with Processing Near Sensor Architecture **2018**,		5
137	HyVE: Hybrid Vertex-Edge Memory Hierarchy for Energy-Efficient Graph Processing. *IEEE Transactions on Computers*, **2019**, 68, 1131-1146	2.5	4
136	A 5-tissue-layer lumped-element based HBC circuit model compatible to IEEE802.15.6 **2015**,		4
135	An Energy-Efficient Quantized and Regularized Training Framework For Processing-In-Memory Accelerators **2020**,		4
134	HyVE: Hybrid vertex-edge memory hierarchy for energy-efficient graph processing **2018**,		4
133	An Auto Loss Compensation System for Capacitive-Coupled Body Channel Communication. *IEEE Transactions on Biomedical Circuits and Systems*, **2019**, 13, 756-765	5.1	4
132	GoHop: Personal VPN to defend from censorship **2014**,		4
131	DVFS-Based Long-Term Task Scheduling for Dual-Channel Solar-Powered Sensor Nodes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2981-2994	2.6	4
130	Statistical analysis of random telegraph noise in digital circuits **2014**,		4
129	Hardware computing for brain network analysis **2010**,		4
128	A novel low power time-mode comparator for successive approximation register ADC. *IEICE Electronics Express*, **2009**, 6, 1155-1160	0.5	4
127	Design of Circular Signal Constellations in the Presence of Phase Noise **2008**,		4
126	Lifetime-Aware Battery Allocation for Wireless Sensor Network under Cost Constraints. *IEICE Transactions on Communications*, **2012**, E95.B, 1651-1660	0.5	4
125	Selective Host-Interference Cancellation: A New Informed Embedding Strategy for Spread Spectrum Watermarking. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2012**, E95.A, 1065-1073	0.4	4
124	Unsupervised Domain Adaptation for ECG Arrhythmia Classification. *Annual International Conference of the IEEE Engineering in Medicine and Biology Society IEEE Engineering in Medicine and Biology Society Annual International Conference*, **2020**, 2020, 304-307	0.9	4

123	Senputing: An Ultra-Low-Power Always-On Vision Perception Chip Featuring the Deep Fusion of Sensing and Computing. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 1-12	3.9	4
122	Enabling Lower-Power Charge-Domain Nonvolatile In-Memory Computing With Ferroelectric FETs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 1-1	3.5	4
121	Scene-Adaptive Image Acquisition for Focus Stacking **2018**,		4
120	Low-overhead implementation of logic encryption using gate replacement techniques **2017**,		3
119	A 3T/Cell Practical Embedded Nonvolatile Memory Supporting Symmetric Read and Write Access Based on Ferroelectric FETs **2019**,		3
118	Nonvolatile memory allocation and hierarchy optimization for high-level synthesis **2015**,		3
117	Design of FPGA-Based Accelerator for Convolutional Neural Network under Heterogeneous Computing Framework with OpenCL. *International Journal of Reconfigurable Computing*, **2018**, 2018, 1-10	2.1	3
116	Blind drift calibration of sensor networks using signal space projection and Kalman filter **2015**,		3
115	An FPGA-based real-time simultaneous localization and mapping system **2015**,		3
114	A low-power robust GFSK demodulation technique for WBAN applications **2013**,		3
113	Design of variable latency adder based on present and transitional states prediction **2013**,		3
112	A hybrid cache architecture with 2D-based prefetching scheme for image and video processing **2013**,		3
111	MDCT spectrum separation: Catching the fine spectral structures for stereo coding **2010**,		3
110	A highly linear low-voltage source-degeneration transconductor based on unity-gain buffer. *Tsinghua Science and Technology*, **2009**, 14, 698-702	3.4	3
109	A power efficient digitally programmable delay element for low power VLSI applications **2009**,		3
108	An Ultra Low Output Resistance and Wide Swing Voltage Follower **2007**,		3
107	NS-KWS **2020**,		3
106	Enabling Secure NVM-Based in-Memory Neural Network Computing by Sparse Fast Gradient Encryption. *IEEE Transactions on Computers*, **2020**, 69, 1596-1610	2.5	3

105	Almost-Nonvolatile IGZO-TFT-Based Near-Sensor In-Memory Computing **2021**,		3
104	STICKER-T: An Energy-Efficient Neural Network Processor Using Block-Circulant Algorithm and Unified Frequency-Domain Acceleration. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 1936-1948	5.5	3
103	**2019**,		3
102	. *IEEE Sensors Journal*, **2021**, 21, 1799-1808	4	3
101	Mixup Asymmetric Tri-Training for Heartbeat Classification Under Domain Shift. *IEEE Signal Processing Letters*, **2021**, 28, 718-722	3.2	3
100	A Bi-directional Integrated Equalizer Based on the Sepic-Zeta Converter for Hybrid Energy Storage System. *IEEE Transactions on Power Electronics*, **2022**, 1-1	7.2	3
99	STICKER-IM: A 65 nm Computing-in-Memory NN Processor Using Block-Wise Sparsity Optimization and Inter/Intra-Macro Data Reuse. *IEEE Journal of Solid-State Circuits*, **2022**, 1-14	5.5	3
98	Design Methodology for Thin-Film Transistor Based Pseudo-CMOS Logic Array with Multi-Layer Interconnect Architecture **2017**,		2
97	Supply-Noise Interactions Among Submodules Inside a Charge-Pump PLL. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 771-775	2.6	2
96	On-Chip Instruction Generation for Cross-Layer CNN Accelerator on FPGA **2019**,		2
95	Design of RF transceivers for wireless sensor networks in hazardous applications. *Analog Integrated Circuits and Signal Processing*, **2014**, 79, 319-329	1.2	2
94	Hardware acceleration with pipelined adder for Support Vector Machine classifier **2014**,		2
93	Design considerations for low power time-mode SAR ADC. *International Journal of Circuit Theory and Applications*, **2014**, 42, 707-730	2	2
92	A High-Linearity Energy-Efficient CMOS PA for Wireless Environment Monitoring **2013**,		2
91	A 1.9 GHz ADPLL with 130 reference cycles settling time in 0.18 μm CMOS technology. *Analog Integrated Circuits and Signal Processing*, **2013**, 76, 81-89	1.2	2
90	Multistage Latency Adders Architecture Employing Approximate Computing. *Journal of Circuits, Systems and Computers*, **2017**, 26, 1750039	0.9	2
89	Probabilistic Brain Fiber Tractography on GPUs **2012**,		2
88	A novel redundant pipelined successive approximation register ADC. *IEICE Electronics Express*, **2013**, 10, 20130047-20130047	0.5	2

87	A PLL based WSN transmitter and I/Q LO signal generator at 430435 MHz. *Analog Integrated Circuits and Signal Processing*, **2011**, 67, 293-308	1.2	2
86	SERSim: a soft error rate simulator and a case study for a 32-bit OpenRisc 1200 microprocessor. *International Journal of Electronics*, **2010**, 97, 441-455	1.2	2
85	A voltage-controlled oscillator with an ultra-low supply voltage and its application to a fractional-N phase-locked loop. *International Journal of Electronics*, **2009**, 96, 1011-1022	1.2	2
84	A low power error detection in the syndrome calculator block for reed-solomon codes: RS(204,188). *Tsinghua Science and Technology*, **2009**, 14, 474-477	3.4	2
83	A heterogeneous accelerator platform for multi-subject voxel-based brain network analysis **2011**,		2
82	A fast-locking all-digital phase-locked loop with a novel counter-based mode switching controller **2009**,		2
81	Implementation of low-swing differential interface circuits for high-speed on-chip asynchronous interconnection. *Science in China Series F: Information Sciences*, **2008**, 51, 975-984		2
80	Leakage Power Modeling Method for SRAM Considering Temperature, Supply Voltage and Bias Voltage **2006**,		2
79	MOS CURRENT MODE LOGIC CIRCUITS: DESIGN CONSIDERATION IN HIGH-SPEED LOW-POWER APPLICATIONS AND ITS FUTURE TREND, A TUTORIAL. *International Journal of High Speed Electronics and Systems*, **2005**, 15, 599-614	0.5	2
78	Improved multiuser detector for fast FH/MFSK systems with soft-limiter		2
77	Multi-channel precision-sparsity-adapted inter-frame differential data codec for video neural network processor **2020**,		2
76	Balanced Switching Schemes for Gradient-Error Compensation in Current-Steering DACs. *IEICE Transactions on Electronics*, **2012**, E95.C, 1790-1798	0.4	2
75	CNN-based Monocular Decentralized SLAM on embedded FPGA **2020**,		2
74	Optimization and Evaluation of Energy-Efficient Mixed-Signal MFCC Feature Extraction Architecture **2020**,		2
73	A priority-based selective bit dropping strategy to reduce DRAM and SRAM power in image processing. *IEICE Electronics Express*, **2016**, 13, 20160990-20160990	0.5	2
72	A 2.2-GHz Configurable Direct Digital Frequency Synthesizer Based on LUT and Rotation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 1970-1980	3.9	2
71	Epipolar Geometry Guided Highly Robust Structured Light 3D Imaging. *IEEE Signal Processing Letters*, **2021**, 28, 887-891	3.2	2
70	CP-FPGA: Energy-Efficient Nonvolatile FPGA With Offline/Online Checkpointing Optimization. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2153-2163	2.6	1

69	AERIS **2019**,		1
68	HS3-DPG: Hierarchical Simulation for 3-D P/G Network. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 2307-2311	2.6	1
67	One-Shot Refresh: A Low-Power Low-Congestion Approach for Dynamic Memories. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 3402-3406	3.5	1
66	GAAS: An Efficient Group Associated Architecture and Scheduler Module for Sparse CNN Accelerators. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 5170-5182	2.5	1
65	Two-stream binocular network: Accurate near field finger detection based on binocular images **2017**,		1
64	Mechanical strain and temperature aware design methodology for thin-film transistor based pseudo-CMOS logic array **2018**,		1
63	Accurate personal ultraviolet dose estimation with multiple wearable sensors **2016**,		1
62	NVPsim: A simulator for architecture explorations of nonvolatile processors **2016**,		1
61	Using nonvolatile processors to reduce leakage in power management approaches **2014**,		1
60	Design and implementation of motion compensator in memory reduced HDTV decoder with embedded compression engine. *Multimedia Tools and Applications*, **2012**, 56, 597-614	2.5	1
59	HS3DPG: Hierarchical simulation for 3D P/G network **2013**,		1
58	A 6-bit 320-MS/s 2-bit/cycle SAR ADC with tri-level charge redistribution **2015**,		1
57	Simultaneous accelerator parallelization and point-to-point interconnect insertion for bus-based embedded SoCs. *Tsinghua Science and Technology*, **2015**, 20, 644-660	3.4	1
56	Increasing compression ratio of low complexity compressive sensing video encoder with application-aware configurable mechanism **2014**,		1
55	A 12-bit 400-MS/s SHA-less pipelined ADC **2014**,		1
54	A low power time-to-digital converter for all-digital phase-locked loop. *Journal of Electronics*, **2011**, 28, 402-408		1
53	Cooperative blind receiving scheme for space-time coding systems **2010**,		1
52	Transmission line inspires a new distributed algorithm to solve the nonlinear dynamical system of physical circuit **2010**,		1

51	Low-Power Off-Chip Memory Design for Video Decoder Using Embedded Bus-Invert Coding **2011**,		1
50	System-Level Evaluation of Video Processing System Using SimpleScalar-Based Multi-core Processor Simulator **2011**,		1
49	Design methodology of multistage time-domain logic speculation circuits **2011**,		1
48	A Functional Model of SystemC-Based MPEG-2 Decoder with Heterogeneous Multi-IP-Cores and Hybrid-Interconnections Architecture **2009**,		1
47	Comparison of Sigma-Delta Modulator for fractional-N PLL frequency synthesizer. *Journal of Electronics*, **2007**, 24, 374-379		1
46	More Practical Intermodulation Distortion in Envelope Elimination and Restoration RF Power Amplifiers. *Midwest Symposium on Circuits and Systems*, **2006**,	1	1
45	Accurate and Fast Estimation of Junction Band-to-Band Leakage in Nanometer-Scale MOSFET **2006** ,		1
44	A 10-Bit, 40 MSamples/s Low Power Pipeline ADC for System-on-a-Chip Digital TV Application **2006**,		1
43	Sensitivity of carrier offset and MAI in DAPSK-MC-CDMA systems **2007**,		1
42	A highly linear low voltage CMOS triode transconductor **2007**,		1
41	MODIFIED CONDITIONAL-PRECHARGE SENSE-AMPLIFIER-BASED FLIP-FLOP WITH IMPROVED SPEED. *Journal of Circuits, Systems and Computers*, **2007**, 16, 199-210	0.9	1
40	A low power ROM-less direct digital frequency synthesizer with preset value pipelined accumulator **2006**,		1
39	A Novel Low-Power and High-Speed Master-Slave D Flip-Flop **2006**,		1
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