Huazhong Yang

List of Publications by Year
in descending order

328	5,394	218381	223531
papers	citations	26 h-index	46 g-index

329	329	329	4025
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Going Deeper with Embedded FPGA Platform for Convolutional Neural Network. , 2016, , .		836
2	Angel-Eye: A Complete Design Flow for Mapping CNN Onto Embedded FPGA. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 35-47.	1.9	382
3	Accurate Temperature-Dependent Integrated Circuit Leakage Power Estimation is Easy. , 2007, , .		135
4	Binary convolutional neural network on RRAM. , 2017, , .		119
5	Technological Exploration of RRAM Crossbar Array for Matrix-Vector Multiplication. Journal of Computer Science and Technology, 2016, 31, 3-19.	0.9	117
6	RRAM-Based Analog Approximate Computing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1905-1917.	1.9	100
7	ForeGraph. , 2017, , .		100
8	Thermal vs Energy Optimization for DVFS-Enabled Processors in Embedded Systems. , 2007, , .		94
9	Region ensemble network: Improving convolutional network for hand pose estimation. , 2017, , .		92
10	FPGP. , 2016, , .		91
11	Stuck-at Fault Tolerance in RRAM Computing Systems. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 102-115.	2.7	88
12	Storage-Less and Converter-Less Photovoltaic Energy Harvesting With Maximum Power Point Tracking for Internet of Things. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 173-186.	1.9	87
13	Sticker: A 0.41-62.1 TOPS/W 8Bit Neural Network Processor with Multi-Sparsity Compatible Convolution Arrays and Online Tuning Acceleration for Fully Connected Layers. , 2018, , .		86
14	A global and updatable ECG beat classification system based on recurrent neural networks and active learning. Information Sciences, 2019, 501, 523-542.	4.0	79
15	GraphH: A Processing-in-Memory Architecture for Large-Scale Graph Processing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 640-653.	1.9	75
16	NXgraph: An efficient graph processing system on a single machine. , 2016, , .		63
17	A Deep Learning Approach for Blind Drift Calibration of Sensor Networks. IEEE Sensors Journal, 2017, 17, 4158-4171.	2.4	59
18	NICSLU: An Adaptive Sparse Matrix Solver for Parallel Circuit Simulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 261-274.	1.9	57

#	Article	IF	Citations
19	GPU-Accelerated Sparse LU Factorization for Circuit Simulation with Performance Modeling. IEEE Transactions on Parallel and Distributed Systems, 2015, 26, 786-795.	4.0	52
20	Angel-Eye: A Complete Design Flow for Mapping CNN onto Customized Hardware. , 2016, , .		52
21	STICKER: An Energy-Efficient Multi-Sparsity Compatible Accelerator for Convolutional Neural Networks in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2020, 55, 465-477.	3.5	51
22	A Configurable Multi-Precision CNN Computing Framework Based on Single Bit RRAM. , 2019, , .		50
23	Storage-less and converter-less maximum power point tracking of photovoltaic cells for a nonvolatile microprocessor. , 2014, , .		49
24	TIME: A Training-in-Memory Architecture for RRAM-Based Deep Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 834-847.	1.9	44
25	MNSIM: Simulation Platform for Memristor-based Neuromorphic Computing System. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, , 1-1.	1.9	42
26	Hardware Trojan Detection in Third-Party Digital Intellectual Property Cores by Multilevel Feature Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1370-1383.	1.9	42
27	PaCC: A Parallel Compare and Compress Codec for Area Reduction in Nonvolatile Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1491-1505.	2.1	41
28	A ReRAM-Based Nonvolatile Flip-Flop With Self-Write-Termination Scheme for Frequent-OFF Fast-Wake-Up Nonvolatile Processors. IEEE Journal of Solid-State Circuits, 2017, 52, 2194-2207.	3.5	41
29	Low Bit-Width Convolutional Neural Network on RRAM. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1414-1427.	1.9	37
30	MSP-MFCC: Energy-Efficient MFCC Feature Extraction Method With Mixed-Signal Processing Architecture for Wearable Speech Recognition Applications. IEEE Access, 2020, 8, 48720-48730.	2.6	37
31	DSA: More Efficient Budgeted Pruning via Differentiable Sparsity Allocation. Lecture Notes in Computer Science, 2020, , 592-607.	1.0	36
32	An EScheduler-Based Data Dependence Analysis and Task Scheduling for Parallel Circuit Simulation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 702-706.	2.2	35
33	A Ferroelectric Nonvolatile Processor with 46 $mu $ s System-Level Wake-up Time and 14 $mu $ s Sleep Time for Energy Harvesting Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 596-607.	3.5	35
34	A Tissue-Channel Transcutaneous Power Transfer Technique for Implantable Devices. IEEE Transactions on Power Electronics, 2018, 33, 9753-9761.	5.4	34
35	Computation-oriented fault-tolerance schemes for RRAM computing systems. , 2017, , .		31
36	Long live TIME. , 2018, , .		30

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37	Hu-Fu: Hardware and Software Collaborative Attack Framework Against Neural Networks. , 2018, , .		29
38	A Generic Graph-Based Neural Architecture Encoding Scheme for Predictor-Based NAS. Lecture Notes in Computer Science, 2020, , 189-204.	1.0	29
39	A 14 Bit 500 MS/s CMOS DAC Using Complementary Switched Current Sources and Time-Relaxed Interleaving DRRZ. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2337-2347.	3.5	28
40	Demystifying and Mitigating Code-Dependent Switching Distortions in Current-Steering DACs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 68-81.	3.5	28
41	Processing Near Sensor Architecture in Mixed-Signal Domain With CMOS Image Sensor of Convolutional-Kernel-Readout Method. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 389-400.	3.5	28
42	The Role and Challenges of Body Channel Communication in Wearable Flexible Electronics. IEEE Transactions on Biomedical Circuits and Systems, 2020, 14, 283-296.	2.7	28
43	Senputing: An Ultra-Low-Power Always-On Vision Perception Chip Featuring the Deep Fusion of Sensing and Computing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 232-243.	3.5	28
44	Spread spectrum audio watermarking based on perceptual characteristic aware extraction. IET Signal Processing, 2016, 10, 266-273.	0.9	27
45	Instruction driven cross-layer CNN accelerator with winograd transformation on FPGA. , 2017, , .		27
46	Solar Power Prediction Assisted Intra-task Scheduling for Nonvolatile Sensor Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 724-737.	1.9	26
47	An Investigation on Ground Electrodes of Capacitive Coupling Human Body Communication. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 910-919.	2.7	26
48	Design of 2T/Cell and 3T/Cell Nonvolatile Memories with Emerging Ferroelectric FETs. IEEE Design and Test, 2019, 36, 39-45.	1.1	26
49	CNN-based Feature-point Extraction for Real-time Visual SLAM on Embedded FPGA. , 2020, , .		26
50	Large depth-of-field 3D shape measurement using an electrically tunable lens. Optics Express, 2019, 27, 29697.	1.7	26
51	NS-CIM: A Current-Mode Computation-in-Memory Architecture Enabling Near-Sensor Processing for Intelligent IoT Vision Nodes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2909-2922.	3.5	25
52	FPGA and GPU implementation of large scale SpMV. , 2010, , .		23
53	Modeling Random Telegraph Noise as a Randomness Source and its Application in True Random Number Generation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1435-1448.	1.9	23
54	A General Framework for Hardware Trojan Detection in Digital Circuits by Statistical Learning Algorithms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1633-1646.	1.9	23

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55	Blind Drift Calibration of Sensor Networks using Sparse Bayesian Learning. IEEE Sensors Journal, 2016, , 1-1.	2.4	22
56	A Five-Tissue-Layer Human Body Communication Circuit Model Tunable to Individual Characteristics. IEEE Transactions on Biomedical Circuits and Systems, 2018, 12, 303-312.	2.7	22
57	Modeling the Impact of Process Variation on Critical Charge Distribution. , 2006, , .		21
58	A 14-bit 1.0-GS/s dynamic element matching DAC with >80 dB SFDR up to the Nyquist. , 2015, , .		21
59	A Self-Adaptive Capacitive Compensation Technique for Body Channel Communication. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 1001-1012.	2.7	21
60	Lowering Area Overheads for FeFET-Based Energy-Efficient Nonvolatile Flip-Flops. IEEE Transactions on Electron Devices, 2018, 65, 2670-2674.	1.6	21
61	A 3.77TOPS/W Convolutional Neural Network Processor With Priority-Driven Kernel Optimization. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 277-281.	2.2	21
62	A 12-bit self-calibrating SAR ADC achieving a Nyquist 90.4-dB SFDR. Analog Integrated Circuits and Signal Processing, 2013, 74, 239-254.	0.9	20
63	FTT-NAS: Discovering Fault-Tolerant Neural Architecture. , 2020, , .		20
64	An application of DAPSK in HF communications. IEEE Communications Letters, 2005, 9, 613-615.	2.5	19
65	NS-FDN: Near-Sensor Processing Architecture of Feature-Configurable Distributed Network for Beyond-Real-Time Always-on Keyword Spotting. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1892-1905.	3.5	19
66	An Energy Efficient Backup Scheme with Low Inrush Current for Nonvolatile SRAM in Energy Harvesting Sensor Nodes. , 2015, , .		19
67	An Energy-Efficient Quantized and Regularized Training Framework For Processing-In-Memory Accelerators. , 2020, , .		18
68	Enabling Lower-Power Charge-Domain Nonvolatile In-Memory Computing With Ferroelectric FETs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2262-2266.	2.2	18
69	Autofocusing method for high-resolution three-dimensional profilometry. Optics Letters, 2020, 45, 375.	1.7	18
70	An adaptive LU factorization algorithm for parallel circuit simulation. , 2012, , .		17
71	STICKER-IM: A 65 nm Computing-in-Memory NN Processor Using Block-Wise Sparsity Optimization and Inter/Intra-Macro Data Reuse. IEEE Journal of Solid-State Circuits, 2022, 57, 2560-2573.	3.5	17
72	A Bidirectional Integrated Equalizer Based on the Sepicâ€“Zeta Converter for Hybrid Energy Storage System. IEEE Transactions on Power Electronics, 2022, 37, 12659-12668.	5.4	16

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73	High Speed Soft-Error-Tolerant Latch and Flip-Flop Design for Multiple VDD Circuit. , 2007, , .		15
74	MDCT Sinusoidal Analysis for Audio Signals Analysis and Processing. IEEE Transactions on Audio Speech and Language Processing, 2013, 21, 1403-1414.	3.8	15
75	Exploring the Precision Limitation for RRAM-Based Analog Approximate Computing. IEEE Design and Test, 2016, 33, 51-58.	1.1	15
76	Guided, Fusion-Based, Large Depth-of-field 3D Imaging Using a Focal Stack. Sensors, 2019, 19, 4845.	2.1	15
77	Enabling Secure NVM-Based in-Memory Neural Network Computing by Sparse Fast Gradient Encryption. IEEE Transactions on Computers, 2020, 69, 1596-1610.	2.4	15
78	Unsupervised Domain Adaptation for ECG Arrhythmia Classification. , 2020, 2020, 304-307.		15
79	FPGA based memory efficient high resolution stereo vision system for video tolling. , 2012, , .		14
80	FeFET-based low-power bitwise logic-in-memory with direct write-back and data-adaptive dynamic sensing interface. , 2020, , .		14
81	An analytical phase noise model of charge pump mismatch in sigma-delta frequency synthesizer. Analog Integrated Circuits and Signal Processing, 2006, 48, 223-229.	0.9	13
82	Performance analysis of data hiding in MPEG-4 AAC audio. Tsinghua Science and Technology, 2009, 14, 55-61.	4.1	13
83	Intra-task scheduling for storage-less and converter-less solar-powered nonvolatile sensor nodes. , 2014, , .		13
84	Design exploration of inrush current aware controller for nonvolatile processor. , 2015, , .		13
85	A Multi-accuracy-Level Approximate Memory Architecture Based on Data Significance Analysis. , 2016, , .		13
86	HyVE: Hybrid vertex-edge memory hierarchy for energy-efficient graph processing. , 2018, , .		13
87	A 130-nm Ferroelectric Nonvolatile System-on-Chip With Direct Peripheral Restore Architecture for Transient Computing System. IEEE Journal of Solid-State Circuits, 2019, 54, 885-895.	3.5	13
88	Enabling Efficient and Flexible FPGA Virtualization for Deep Learning in the Cloud. , 2020, , .		13
89	MACSen: A Processing-In-Sensor Architecture Integrating MAC Operations Into Image Sensor for Ultra-Low-Power BNN-Based Intelligent Visual Perception. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 627-631.	2.2	13
90	A New Family of Sequential Elements With Built-in Soft Error Tolerance for Dual-VDD Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1372-1384.	2.1	12

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91	Design of Signal Constellations in the Presence of Phase Noise. , 2008, , .		12
92	Design methodology of variable latency adders with multistage function speculation. , 2010, , .		12
93	Robust and transparent audio watermarking based on improved spread spectrum and psychoacoustic masking. , 2012, , .		12
94	PAGANI Toolkit: Parallel graphâ€theoretical analysis package for brain network big data. Human Brain Mapping, 2018, 39, 1869-1885.	1.9	12
95	Low-Power and Scalable Retention-Enhanced IGZO TFT eDRAM-Based Charge-Domain Computing. , 2021, , .		12
96	Design of Circular Signal Constellations in the Presence of Phase Noise. , 2008, , .		11
97	Approximate Computing in Chrominance Cache for Image/Video Processing. , 2015, , .		11
98	Dynamic Channel Modeling and OFDM System Analysis for Capacitive Coupling Body Channel Communication. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 735-745.	2.7	11
99	A Sparse-Adaptive CNN Processor with Area/Performance balanced N-Way Set-Associate PE Arrays Assisted by a Collision-Aware Scheduler. , 2019, , .		11
100	Soft Error Mitigation for Deep Convolution Neural Network on FPGA Accelerators. , 2020, , .		11
101	Explore-Bench: Data Sets, Metrics and Evaluations for Frontier-based and Deep-reinforcement-learning-based Autonomous Exploration. , 2022, , .		11
102	Drift detection and calibration of sensor networks. , 2015, , .		10
103	CORAL: Coarse-grained reconfigurable architecture for Convolutional Neural Networks. , 2017, , .		10
104	An Auto Loss Compensation System for Capacitive-Coupled Body Channel Communication. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 756-765.	2.7	10
105	CLECG: A Novel Contrastive Learning Framework for Electrocardiogram Arrhythmia Classification. IEEE Signal Processing Letters, 2021, 28, 1993-1997.	2.1	10
106	High PE Utilization CNN Accelerator with Channel Fusion Supporting Pattern-Compressed Sparse Neural Networks. , 2020, , .		10
107	Low Voltage Low Power Class-AB OTA with Negative Resistance Load. , 2006, , .		9
108	A precision adaptive average time synchronization protocol in wireless sensor networks. , 2008, , .		9

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109	A blind audio watermarking algorithm by logarithmic quantization index modulation. Multimedia Tools and Applications, 2014, 71, 1157-1177.	2.6	9
110	An FPGA-based real-time simultaneous localization and mapping system. , 2015, , .		9
111	Noise Margin Modeling for Zero-$V_{ext {GS}}$ Load TFT Circuits and Yield Estimation. IEEE Transactions on Electron Devices, 2016, 63, 684-690.	1.6	9
112	Low-overhead implementation of logic encryption using gate replacement techniques. , 2017, , .		9
113	AICNN: Implementing Typical CNN Algorithms with Analog-to-Information Conversion Architecture. , 2017, , .		9
114	A 4-Mbps 41-pJ/bit On-off Keying Transceiver for Body-channel Communication with Enhanced Auto Loss Compensation Technique. , 2019, , .		9
115	Long Live TIME: Improving Lifetime and Security for NVM-Based Training-in-Memory Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4707-4720.	1.9	9
116	FTT-NAS: Discovering Fault-tolerant Convolutional Neural Architecture. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-24.	1.9	9
117	A low power error detection in the syndrome calculator block for reed-solomon codes: RS(204,188). Tsinghua Science and Technology, 2009, 14, 474-477.	4.1	8
118	Lightweight Precision-Adaptive Time Synchronization in Wireless Sensor Networks. IEICE Transactions on Communications, 2010, E93-B, 2299-2308.	0.4	8
119	Exploration of Electrical and Novel Optical Chip-to-Chip Interconnects. IEEE Design and Test, 2014, 31, 28-35.	1.1	8
120	A novel quasi-static channel enhancing technique for body channel communication. , 2014, , .		8
121	All-Digital Galvanically-Coupled BCC Receiver Resilient to Frequency Misalignment. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 714-726.	2.7	8
122	A 65-nm ReRAM-Enabled Nonvolatile Processor With Time-Space Domain Adaption and Self-Write-Termination Achieving $> 4imes $ Faster Clock Frequency and $> 6imes $ Higher Restore Speed. IEEE Journal of Solid-State Circuits, 2017, 52, 2769-2785.	3.5	8
123	An Auto Loss Compensation System for Non-contact Capacitive Coupled Body Channel Communication. , 2018, , .		8
124	Mixup Asymmetric Tri-Training for Heartbeat Classification Under Domain Shift. IEEE Signal Processing Letters, 2021, 28, 718-722.	2.1	8
125	Almost-Nonvolatile IGZO-TFT-Based Near-Sensor In-Memory Computing. , 2021, , .		8
126	An Ultra Low Output Resistance and Wide Swing Voltage Follower. , 2007, , .		7

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127	A power efficient digitally programmable delay element for low power VLSI applications. , 2009, , .		7
128	Hardware computing for brain network analysis. , 2010, , .		7
129	Blind drift calibration of sensor networks using signal space projection and Kalman filter. , 2015, , .		7
130	The effects of GND electrodes in capacitive-coupling body channel communication. , 2015, , .		7
131	A 3T/Cell Practical Embedded Nonvolatile Memory Supporting Symmetric Read and Write Access Based on Ferroelectric FETs. , 2019, , .		7
132	CNN-based Monocular Decentralized SLAM on embedded FPGA. , 2020, , .		7
133	Bridge Dynamic Displacement Monitoring Using Adaptive Data Fusion of GNSS and Accelerometer Measurements. IEEE Sensors Journal, 2021, 21, 24359-24370.	2.4	7
134	Temperature-Aware NBTI Modeling Techniques in Digital Circuits. IEICE Transactions on Electronics, 2009, E92-C, 875-886.	0.3	7
135	Gibbon: Efficient Co-Exploration of NN Model and Processing-In-Memory Architecture. , 2022, , .		7
136	The NBTI Impact on RF Front End in Wireless Sensor Networks. , 2009, , .		6
137	A 250KS/s, 0.8V ultra low power successive approximation register ADC using a Dynamic rail-to-rail comparator. IEICE Electronics Express, 2010, 7, 261-267.	0.3	6
138	Making Human Connectome Faster: GPU Acceleration of Brain Network Analysis. , 2010, , .		6
139	Probabilistic Brain Fiber Tractography on GPUs. , 2012, , .		6
140	Efficient region-aware P/G TSV planning for 3D ICs. , 2014, , .		6
141	A 5-tissue-layer lumped-element based HBC circuit model compatible to IEEE802.15.6. , 2015, , .		6
142	NVPsim: A simulator for architecture explorations of nonvolatile processors. , 2016, , .		6
143	DVFS-Based Long-Term Task Scheduling for Dual-Channel Solar-Powered Sensor Nodes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2981-2994.	2.1	6
144	CMOS Image Sensor Data-Readout Method for Convolutional Operations with Processing Near Sensor Architecture. , 2018, , .		6

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145	Design of FPGA-Based Accelerator for Convolutional Neural Network under Heterogeneous Computing Framework with OpenCL. International Journal of Reconfigurable Computing, 2018, 2018, 1-10.	0.2	6
146	HyVE: Hybrid Vertex-Edge Memory Hierarchy for Energy-Efficient Graph Processing. IEEE Transactions on Computers, 2019, 68, 1131-1146.	2.4	6
147	A 2.2-GHz Configurable Direct Digital Frequency Synthesizer Based on LUT and Rotation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1970-1980.	3.5	6
148	Temporal Matrices Mapping-Based Calibration Method for Event-Driven Structured Light Systems. IEEE Sensors Journal, 2021, 21, 1799-1808.	2.4	6
149	Epipolar Geometry Guided Highly Robust Structured Light 3D Imaging. IEEE Signal Processing Letters, 2021, 28, 887-891.	2.1	6
150	STICKER-T: An Energy-Efficient Neural Network Processor Using Block-Circulant Algorithm and Unified Frequency-Domain Acceleration. IEEE Journal of Solid-State Circuits, 2021, 56, 1936-1948.	3.5	6
151	Selective Host-Interference Cancellation: A New Informed Embedding Strategy for Spread Spectrum Watermarking. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2012, E95.A, 1065-1073.	0.2	6
152	High-Quality Single-Model Deep Video Compression with Frame-Conv3D and Multi-frame Differential Modulation. Lecture Notes in Computer Science, 2020, , 239-254.	1.0	6
153	NS-KWS. , 2020, , .		6
154	An energy efficient fully integrated OOK transceiver SoC for wireless body area networks. , 2013, , .		5
155	A hybrid cache architecture with 2D-based prefetching scheme for image and video processing. , 2013, , .		5
156	A novel redundant pipelined successive approximation register ADC. IEICE Electronics Express, 2013, 10, 20130047-20130047.	0.3	5
157	Statistical analysis of random telegraph noise in digital circuits. , 2014, , .		5
158	Supply-Noise Interactions Among Submodules Inside a Charge-Pump PLL. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 771-775.	2.1	5
159	Noise Margin, Delay, and Power Model for Pseudo-CMOS TFT Logic Circuits. IEEE Transactions on Electron Devices, 2017, 64, 2635-2642.	1.6	5
160	CP-FPGA: Energy-Efficient Nonvolatile FPGA With Offline/Online Checkpointing Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2153-2163.	2.1	5
161	Redundancyâ€bandwidth scalable techniques for signalâ€independent element transition rates in highâ€speed currentâ€steering DACs. International Journal of Circuit Theory and Applications, 2018, 46, 1006-1027.	1.3	5
162	Energy-efficient MFCC extraction architecture in mixed-signal domain for automatic speech recognition. , 2018, , .		5

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163	RRAM Based Buffer Design for Energy Efficient CNN Accelerator. , 2018, , .		5
164	AERIS. , 2019, , .		5
165	Optimization and Evaluation of Energy-Efficient Mixed-Signal MFCC Feature Extraction Architecture. , 2020, , .		5
166	INCA: INterruptible CNN Accelerator for Multi-tasking in Embedded Robots. , 2020, , .		5
167	Black Box Search Space Profiling for Accelerator-Aware Neural Architecture Search. , 2020, , .		5
168	Lifetime-Aware Battery Allocation for Wireless Sensor Network under Cost Constraints. IEICE Transactions on Communications, 2012, E95.B, 1651-1660.	0.4	5
169	A Fast Parallel Sparse Solver for SPICE-Based Circuit Simulators. , 2015, , .		5
170	Computing-in-memory with thin-filmtransistors: challenges and opportunities. Flexible and Printed Electronics, 2022, 7, 024001.	1.5	5
171	A Novel Low-Power and High-Speed Master-Slave D Flip-Flop. , 2006, , .		4
172	A novel low power time-mode comparator for successive approximation register ADC. IEICE Electronics Express, 2009, 6, 1155-1160.	0.3	4
173	A low-power robust GFSK demodulation technique for WBAN applications. , 2013, , .		4
174	Design of RF transceivers for wireless sensor networks in hazardous applications. Analog Integrated Circuits and Signal Processing, 2014, 79, 319-329.	0.9	4
175	Design considerations for low power timeâ€mode SAR ADC. International Journal of Circuit Theory and Applications, 2014, 42, 707-730.	1.3	4
176	GoHop: Personal VPN to defend from censorship. , 2014, , .		4
177	Optimizing convolutional neural network on FPGA under heterogeneous computing framework with OpenCL. , 2016, , .		4
178	Scene-Adaptive Image Acquisition for Focus Stacking. , 2018, , .		4
179	On-Chip Instruction Generation for Cross-Layer CNN Accelerator on FPGA. , 2019, , .		4
180	Dynamic Ternary Content-Addressable Memory Is Indeed Promising: Design and Benchmarking Using Nanoelectromechanical Relays. , 2021, , .		4

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181	Balanced Switching Schemes for Gradient-Error Compensation in Current-Steering DACs. IEICE Transactions on Electronics, 2012, E95.C, 1790-1798.	0.3	4
182	Accuracy Optimization With the Framework of Non-Volatile Computing-In-Memory Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 518-529.	3.5	4
183	PACA: A Pattern Pruning Algorithm and Channel-Fused High PE Utilization Accelerator for CNNs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 5043-5056.	1.9	4
184	A low power ROM-less direct digital frequency synthesizer with preset value pipelined accumulator. , 2006, , .		3
185	Virtual Transmission Method, A New Distributed Algorithm to Solve Sparse Linear Systems. , 2008, , .		3
186	A voltage-controlled oscillator with an ultra-low supply voltage and its application to a fractional-N phase-locked loop. International Journal of Electronics, 2009, 96, 1011-1022.	0.9	3
187	A highly linear low-voltage source-degeneration transconductor based on unity-gain buffer. Tsinghua Science and Technology, 2009, 14, 698-702.	4.1	3
188	A fast-locking all-digital phase-locked loop with a novel counter-based mode switching controller. , 2009, , .		3
189	MDCT spectrum separation: Catching the fine spectral structures for stereo coding. , 2010, , .		3
190	Low-Power Off-Chip Memory Design for Video Decoder Using Embedded Bus-Invert Coding. , 2011, , .		3
191	A PLL based WSN transmitter and I/Q LO signal generator at 430â€“435ÂMHz. Analog Integrated Circuits and Signal Processing, 2011, 67, 293-308.	0.9	3
192	A heterogeneous accelerator platform for multi-subject voxel-based brain network analysis. , 2011, , .		3
193	HS3DPG: Hierarchical simulation for 3D P/G network. , 2013, , .		3
194	Design of variable latency adder based on present and transitional states prediction. , 2013, , .		3
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196	Multistage Latency Adders Architecture Employing Approximate Computing. Journal of Circuits, Systems and Computers, 2017, 26, 1750039.	1.0	3
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198	ASP-SIFT: Using Analog Signal Processing Architecture to Accelerate Keypoint Detection of SIFT Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 198-211.	2.1	3

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199	Investigation and Modeling of Multi-Node Body Channel Wireless Power Transfer. Sensors, 2020, 20, 156.	2.1	3
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