Ali Jahanian

List of Publications by Year
in descending order

64 papers	220 citations	1307366 7 h-index	1281743 11 g-index
64 all docs	64 docs citations	64 times ranked	147 citing authors

#	Article	IF	Citations
1	Improved CMOS (4;2) compressor designs for parallel multipliers. Computers and Electrical Engineering, 2012, 38, 1703-1716.	3.0	35
2	High-performance CMOS (4:2) compressors. International Journal of Electronics, 2014, 101, 1511-1525.	0.9	21
3	Prediction and reduction of routing congestion. , 2006, , .		20
4	Redesigned CMOS (4; 2) compressor for fast binary multipliers. Canadian Journal of Electrical and Computer Engineering, 2013, 36, 111-115.	1.5	17
5	A fast placement algorithm for embedded just-in-time reconfigurable extensible processing platform. Journal of Supercomputing, 2015, 71, 121-143.	2.4	13
6	Evaluation, prediction and reduction of routing congestion. Microelectronics Journal, 2007, 38, 942-958.	1.1	8
7	Higher security of ASIC fabrication process against reverse engineering attack using automatic netlist encryption methodology. Microprocessors and Microsystems, 2016, 42, 1-9.	1.8	7
8	Multiâ€threshold and multiâ€input DNA logic design style for profiling the microRNA biomarkers of real cancers. IET Nanobiotechnology, 2019, 13, 665-673.	1.9	7
9	ParSA: Parallel simulated annealing placement algorithm for multi-core systems. , 2012, , .		6
10	Automatic netlist scrambling methodology in ASIC design flow to hinder the reverse engineering. , 2013, , .		6
11	A general-purpose field-programmable pin-constrained digital microfluidic biochip. , 2015, , .		6
12	Improved timing closure by early buffer planning in floor-placement design flow. , 2007, , .		5
13	Higher Flexibililty of Recongurable Digital Micro/Nano Fluidic Biochips using an FPGA-Inspired Architecture. Scientia Iranica, 2016, 23, 1554-1562.	0.3	5
14	Fault-tolerant architecture and CAD algorithm for field-programmable pin-constrained digital microfluidic biochips. , 2015, , .		4
15	Security Improvement of FPGA Design Against Timing Side Channel Attack Using Dynamic Delay Management. , 2018, , .		4
16	Metro-on-chip: an efficient physical design technique for congestion reduction. IEICE Electronics Express, 2007, 4, 510-516.	0.3	3
17	Using metro-on-chip in physical design flow for congestion and routability improvement. Microelectronics Journal, 2008, 39, 261-274.	1.1	3
18	Feasibility Study of Using the RF Interconnects in Large FPGAs to Improve Routing Tracks Usage. , 2011, , .		3

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19	Security improvement of FPGA configuration file against the reverse engineering attack. , 2016, , .		3
20	Customized Placement Algorithm of Nanoscale DNA Logic Circuits. Journal of Circuits, Systems and Computers, 2017, 26, 1750150.	1.0	3
21	Three-Dimensional Physical Design Flow for Monolithic 3D-FPGAs to Improve Timing Closure and Chip Area. Journal of Circuits, Systems and Computers, 2017, 26, 1750154.	1.0	3
22	Power side-channel leakage assessment and locating the exact sources of leakage at the early stages of ASIC design process. Journal of Supercomputing, 2022, 78, 2219-2244.	2.4	3
23	Trojan Vulnerability Map: An Efficient Metric for Modeling and Improving the Security Level of Hardware. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2014, E97.A, 2218-2226.	0.2	3
24	Performance and Timing Yield Enhancement using Highway-on-Chip Planning. , 2008, , .		2
25	A Hybrid RF/Metal Clock Routing Algorithm to Improve Clock Delay and Routing Congestion. , 2011, , .		2
26	Parallelizing the FPGA global routing algorithm on multi-core systems without quality degradation. IEICE Electronics Express, 2011, 8, 2061-2067.	0.3	2
27	Improved timing closure by analytical buffer and TSV planning in three-dimensional chips. IEICE Electronics Express, 2012, 9, 1849-1854.	0.3	2
28	Three-dimensional switchbox multiplexing in emerging 3D-FPGAs to reduce chip footprint and improve TSV usage. The Integration VLSI Journal, 2015, 50, 81-90.	1.3	2
29	Security Path: An Emerging Design Methodology to Protect the FPGA IPs Against Passive/Active Design Tampering. Journal of Electronic Testing: Theory and Applications (JETTA), 2016, 32, 329-343.	0.9	2
30	Layout Vulnerability Reduction against Trojan Insertion Using Security-Aware White Space Distribution. , 2017, , .		2
31	Drug Discovery Evolution Using the Customized Digital Microfluidic Biochips. , 2018, , .		2
32	Real parallel and constant delay logic circuit design methodology based on the DNA model-of-computation. Microprocessors and Microsystems, 2018, 61, 217-226.	1.8	2
33	Improved experimental time of ultraâ€large bioassays using a parallelised microfluidic biochip architecture/scheduling. IET Nanobiotechnology, 2018, 12, 484-490.	1.9	2
34	EJOP: An Extensible Java Processor with Reasonable Performance/Flexibility Trade-off. , 2012, , .		1
35	Improved performance and power consumption of three-dimensional FPGAs using Carbon Nanotube interconnects. , 2012, , .		1
36	Modeling, evaluation and mitigation of SEU error in three-dimensional FPGAs. , 2012, , .		1

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37	Multiplexed switch box architecture in three-dimensional FPGAs to reduce silicon area and improve TSV usage. , 2012, , .		1
38	Field-programmable cell array pin-constrained digital microfluidic biochip. , 2015, , .		1
39	Efficient mapping of DNA logic circuits on parallelized digital microfluidic architcture. , 2017, , .		1
40	Scalable security path methodology: A cost-security trade-off to protect FPGA IPs against active and passive tampers. , 2017, , .		1
41	Drug Discovery Applications: A Customized Digital Microfluidic Biochip Architecture/CAD Flow. IEEE Nanotechnology Magazine, 2019, 13, 25-34.	0.9	1
42	High Accuracy Multi-input DNA Logic Gate Using The Spatially Localized DNA Structures. , 2020, , .		1
43	Analytical design of multi-threshold and high fan-in DNA-based logical sensors to profile the pattern of MS microRNAs. Biomedical Engineering Letters, 2021, 11, 131-145.	2.1	1
44	A Closed-Form Transient Response of Coupled Transmission Lines. IEEE Systems Journal, 2022, 16, 801-809.	2.9	1
45	Accurate Crosstalk Noise Modeling and Analysis of Non-Identical Lossy Interconnections Using Convex Optimization Method. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 4168-4176.	3.5	1
46	Performance Improvement of Physical Retiming with Shortcut Insertion. , 2008, , .		0
47	A LANDMARK-BASED NAVIGATION SYSTEM FOR HIGH SPEED CARS IN THE ROADS WITH BRANCHES. International Journal of Information Acquisition, 2009, 06, 193-202.	0.2	0
48	EARLY BUFFER PLANNING WITH CONGESTION CONTROL USING BUFFER REQUIREMENT MAP. Journal of Circuits, Systems and Computers, 2010, 19, 949-973.	1.0	0
49	Chip master planning: An efficient methodology to improve design closure and complexity management of ultra large chips. , 2010, , .		0
50	Improved predictability, timing yield and power consumption using hierarchical highways-on-chip planning methodology. The Integration VLSI Journal, 2011, 44, 123-135.	1.3	0
51	Congestion and track usage improvement of large FPGAs using metro-on-FPGA methodology. , 2011, , .		0
52	VMAP: A Variation Map-Aware Placement Algorithm for Leakage Power Reduction in FPGAs. , 2011, , .		0
53	RF-Interconnect Resource Assignment and Placement Algorithms in Application Specific ICs to Improve Performance and Reduce Routing Congestion. , 2012, , .		0
54	TrueFlex: A flexible and efficient evaluation platform for networked automotive systems. , 2012, , .		0

#	Article	IF	Citations
55	RF resource planning in application specific integrated circuits to improve timing closure. , 2013, , .		0
56	Improved performance and resource usage of FPGA using resource-aware design; the case of a decimal array multiplier. , 2013, , .		0
57	IMPROVED DELAY AND PROCESS VARIATION TOLERANT CLOCK TREE NETWORK IN ULTRA-LARGE CIRCUITS USING HYBRID RF/METAL CLOCK ROUTING. Journal of Circuits, Systems and Computers, 2014, 23, 1450050.	1.0	0
58	Design of CAD ASIP for JIT extensible processor: Case study on PathFinder routing algorithm. , 2015, , .		0
59	A new Nano-scale differential logic style for power analysis attack. , 2015, , .		0
60	Vulnerability Analysis Against Fault Attack in terms of the Timing Behavior of Fault Injection. , 2020, , .		0
61	Evaluating the Metro-on-Chip Methodology to Improve the Congestion and Routability. Communications in Computer and Information Science, 2008, , 689-696.	0.4	0
62	Performance Improvement and Congestion Reduction of Large FPGAs Using On-Chip Microwave Interconnects. IEICE Transactions on Electronics, 2012, E95.C, 1610-1619.	0.3	0
63	RNA secondary structured logic gates for profiling the microRNA cancer biomarkers. IET Nanobiotechnology, 2020, 14, 181-190.	1.9	0
64	Flexible and Automatable Microfluidic-based Architecture and CAD Algorithm for Implementation of Large DNA Digital Storage. , 2022, , .		0