Jari Nurmi

List of Publications by Year in descending order

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245	1,714	566801	580395
papers	citations	15 h-index	25 g-index

260	260	260	904
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Performance Evaluation of Adaptive Tracking Techniques with Direct-State Kalman Filter. Sensors, 2022, 22, 420.	2.1	8
2	A Survey of Security in Cloud, Edge, and Fog Computing. Sensors, 2022, 22, 927.	2.1	75
3	Managing Perceived Loneliness and Social-Isolation Levels for Older Adults: A Survey with Focus on Wearables-Based Solutions. Sensors, 2022, 22, 1108.	2.1	8
4	Guest Editorial Special Issue on Advanced Sensors and Sensing Technologies for Indoor Positioning and Navigation. IEEE Sensors Journal, 2022, 22, 4754-4754.	2.4	0
5	Cloud Platforms for Context-Adaptive Positioning and Localisation in GNSS-Denied Scenariosâ€”A Systematic Review. Sensors, 2022, 22, 110.	2.1	5
6	Towards Approximate Computing for Achieving Energy vs. Accuracy Trade-offs. , 2022, , .		2
7	Towards Accelerated Localization Performance Across Indoor Positioning Datasets. , 2022, , .		1
8	Low-Complexity Adaptive Direct-State Kalman Filter for Robust GNSS Carrier Tracking. , 2022, , .		3
9	Implementation of Embedded Multiple Signal Classification Algorithm for Mesh IoT Networks. , 2022, , .		1
10	A Machine-Learning-Based Analysis of the Relationships between Loneliness Metrics and Mobility Patterns for Elderly. Sensors, 2022, 22, 4946.	2.1	8
11	Direct Lightweight Temporal Compression for Wearable Sensor Data. , 2021, 5, 1-4.		8
12	Collaborative Indoor Positioning Systems: A Systematic Review. Sensors, 2021, 21, 1002.	2.1	77
13	Run-to-Completion versus Pipelined: The Case of 100 Gbps Packet Parsing. , 2021, , .		0
14	Adaptive Techniques in Scalar Tracking Loops with Direct-State Kalman-Filter. , 2021, , .		5
15	Systematic Review on Machine-Learning Algorithms Used in Wearable-Based eHealth Data Analysis. IEEE Access, 2021, 9, 112221-112235.	2.6	21
16	Evaluation of Adaptive Loop-Bandwidth Tracking Techniques in GNSS Receivers. Sensors, 2021, 21, 502.	2.1	13
17	Understanding the Performance of Task Offloading for Wearables in a Two-Tier Edge Architecture. , 2021, , .		2
18	Intelligent Cognitive Radio Architecture Applying Machine Learning and Reconfigurability. , 2021, , .		1

#	Article	IF	Citations
19	Lightweight Wi-Fi Fingerprinting with a Novel RSS Clustering Algorithm. , 2021, , .		3
20	A custom processor for protocol-independent packet parsing. Microprocessors and Microsystems, 2020, 72, 102910.	1.8	7
21	Flexible Software-Defined Packet Processing Using Low-Area Hardware. IEEE Access, 2020, 8, 98929-98945.	2.6	8
22	New Cluster Selection and Fine-grained Search for k-Means Clustering and Wi-Fi Fingerprinting. , 2020, , .		12
23	Towards Energy Efficiency in the Internet of Wearable Things: A Systematic Review. IEEE Access, 2020, 8, 175412-175435.	2.6	52
24	HTC Vive as a Ground-Truth System for Anchor-Based Indoor Localization. , 2020, , .		6
25	RSS Fingerprinting Dataset Size Reduction Using Feature-Wise Adaptive k-Means Clustering. , 2020, , .		13
26	Improving DBSCAN for Indoor Positioning Using Wi-Fi Radio Maps in Wearable and IoT Devices. , 2020, , .		2
27	Effects of Multipath Attenuation in the Optical Communication-Based Internet of Underwater Things. Sensors, 2020, 20, 6201.	2.1	10
28	Reducing Crossbar Costs in the Match-Action Pipeline. , 2019, , .		2
29	An Explicitly Parallel Architecture for Packet Processing in Software Defined Networks. , 2019, , .		0
30	Errata to â€œEvaluation of a Heterogeneous Multicore Architecture by Design and Test of an OFDM Receiverâ€• IEEE Transactions on Parallel and Distributed Systems, 2018, 29, 719-719.	4.0	4
31	Delayâ€“Accuracy Tradeoff in Opportunistic Time-of-Arrival Localization. IEEE Signal Processing Letters, 2018, 25, 763-767.	2.1	3
32	Design and Implementation of Multi-Purpose DCT/DST-Specific Accelerator on Heterogeneous Multicore Architecture. , 2018, , .		1
33	Design and Implementation of 2D IDCT/IDST-Specific Accelerator on Heterogeneous Multicore Architecture. , 2018, , .		0
34	Low-latency Packet Parsing in Software Defined Networks. , 2018, , .		5
35	Power mitigation of a heterogeneous multicore architecture on FPGA/ASIC by DFS/DVFS techniques. Microprocessors and Microsystems, 2018, 63, 259-268.	1.8	1
36	A low-cost high-speed self-checking carry select adder with multiple-fault detection. Microelectronics Journal, 2018, 81, 16-27.	1.1	10

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37	An Explicitly Parallel Architecture for Packet Parsing in Software Defined Networks. , 2018, , .		7
38	Joint Tracking of Multiple Frequency Signals from the same GNSS satellite. , 2018, , .		4
39	Power Mitigation by Performance Equalization in a Heterogeneous Reconfigurable Multicore Architecture. Journal of Signal Processing Systems, 2017, 87, 287-297.	1.4	3
40	Evaluation of a Heterogeneous Multicore Architecture by Design and Test of an OFDM Receiver. IEEE Transactions on Parallel and Distributed Systems, 2017, 28, 3171-3187.	4.0	15
41	FPGA Applications in Unmanned Aerial Vehicles - A Review. Lecture Notes in Computer Science, 2017, , 217-228.	1.0	11
42	FPGA Implementation Issues of a Flexible Synchronizer Suitable for NC-OFDM-Based Cognitive Radios. Journal of Systems Architecture, 2017, 76, 102-116.	2.5	10
43	Design and Implementation of IEEE 802.11a/g Receiver Blocks on a Coarse-Grained Reconfigurable Array. , 2017, , 61-89.		0
44	Integration issues of a run-time configurable memory management unit to a RISC processor on FPGA. Microprocessors and Microsystems, 2017, 49, 179-191.	1.8	1
45	A comparison of Bayesian localization methods in the presence of outliers. , 2017, , .		1
46	Guest Editorial: Implementation Issues in System-on-Chip. Journal of Signal Processing Systems, 2017, 87, 269-270.	1.4	1
47	HW/SW Co-design of an IEEE 802.11a/g Receiver on Xilinx Zynq SoC using High-Level Synthesis. , 2017, , .		1
48	Power mitigation of a heterogeneous multicore architecture by frequency scaling in an OFDM receiver test case. , 2017, , .		2
49	Ninesilica: A Homogeneous MPSoC Approach for SDR Platforms. , 2017, , 107-119.		2
50	Design Transformation from a Single-Core to a Multi-Core Architecture Targeting Massively Parallel Signal Processing Algorithms. , 2017, , 7-28.		0
51	FPGA implementation and integration of a reconfigurable CAN-based co-processor to the coffee risc processor. , 2016, , .		0
52	Using OpenCL to rapidly prototype FPGA designs. , 2016, , .		6
53	Accelerating Computation on an Android Phone with OpenCL Parallelism and Optimizing Workload Distribution between a Phone and a Cloud Service. , 2016, , .		1
54	Multi-GNSS analysis based on full constellations simulated data. , 2016, , .		2

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55	Blind sub-Nyquist GNSS signal detection. , 2016, , .		2
56	HARP2: An X-Scale Reconfigurable Accelerator-Rich Platform for Massively-Parallel Signal Processing Algorithms. Journal of Signal Processing Systems, 2016, 85, 341-353.	1.4	7
57	MULTI-POS: Marie Curie Network in Multi-technology Positioning. , 2016, , .		0
58	Software Simulators and Multi-Frequency Test Scenarios for GALILEO. Signals and Communication Technology, 2015, , 289-321.	0.4	0
59	An example of scenario-based evaluation of military capability areas An impact assessment of alternative systems on operations. , 2015, , .		4
60	Hybrid Cooperative Positioning in Harsh Environments. , 2015, , .		0
61	WarmPie: A bare-bones implementation of message passing interface for embedded many-cores. , 2015, , .		1
62	Design of a hybrid multicore platform for high performance reconfigurable computing. , 2015, , .		3
63	Design and evaluation of correlation accelerator in IEEE-802.11a/g receiver using a template-based Coarse-Grained Reconfigurable Array. , 2015, , .		4
64	Design, implementation and analysis of a run-time configurable Memory Management Unit on FPGA. , 2015, , .		6
65	Implementation of IEEE-802.11a/g receiver blocks on a coarse-grained reconfigurable array. , 2015, , .		2
66	Baseband Hardware Implementations for Galileo Receiver. Signals and Communication Technology, 2015, , 121-137.	0.4	0
67	Relaxed direct position estimation as strategy for open-loop GNSS receivers. , 2015, , .		1
68	Design and Implementation of a Power-aware FFT Core for OFDM-based DSA-enabled Cognitive Radios. Journal of Signal Processing Systems, 2015, 78, 257-265.	1.4	6
69	PVT Computation Issues in Mixed Galileo/GPS Reception. Signals and Communication Technology, 2015, , 139-167.	0.4	1
70	Galileo Signals. Signals and Communication Technology, 2015, , 35-56.	0.4	0
71	Approximate computing for complexity reduction in timing synchronization. Eurasip Journal on Advances in Signal Processing, 2014, 2014, .	1.0	3
72	MULTI-POS - multi-technology positioning professionals training network. , 2014, , .		0

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73	Transport triggered architecture to perform carrier synchronization for LTE. Transactions on Embedded Computing Systems, 2014, 13, 1-15.	2.1	0
74	Hand-grip impact on range-based cooperative positioning. , 2014, , .		1
75	Stand-alone GNSS time synchronization architecture. , 2014, , .		0
76	FPGA implementation of a flexible synchronizer for cognitive radio applications. , 2014, , .		5
77	Constraint-driven frequency scaling in a Coarse Grain Reconfigurable Array. , 2014, , .		2
78	Area estimation of time-domain GNSS receiver architectures. , 2014, , .		1
79	Accomodating the fast-paced evolution of VLSI in engineering curricula. , 2014, , .		0
80	Design of an accelerator-rich architecture by integrating multiple heterogeneous coarse grain reconfigurable arrays over a network-on-chip. , 2014, , .		10
81	Training communication skills in project-oriented microelectronics courses. , 2014, , .		1
82	Cyclostationary features of downsampled 802.11g OFDM signal for cognitive positioning systems. , 2014, , .		0
83	High-level parameterizable area estimation modeling for ASIC designs. The Integration VLSI Journal, 2014, 47, 461-475.	1.3	3
84	MPSoC based on Transport Triggered Architecture for baseband processing of an LTE receiver. Journal of Systems Architecture, 2014, 60, 140-149.	2.5	5
85	Design of a Flexible, Energy Efficient (Auto)Correlator Block for Timing Synchronization. , 2014, , .		0
86	Faster than real-time GNSS receiver testing. , 2014, , .		0
87	Effects of Radio Front-end PLL Phase Noise on GNSS Baseband Correlation. Navigation, Journal of the Institute of Navigation, 2014, 61, 13-21.	1.7	3
88	Correctly rounded architectures for Floating-Point multi-operand addition and dot-product computation. , 2013, , .		7
89	Design & implementation of software defined radios on a homogeneous multi-processor architecture. , 2013, , .		2
90	Correlator design and implementation for GNSS receivers. , 2013, , .		3

#	Article	IF	Citations
91	A Reconfigurable Application-specific Instruction-set Processor for Fast Fourier Transform processing. , 2013, , .		6
92	Design of a reconfigurable multi-core architecture for streaming applications with a case study on performance evaluation of FIR-filters. , 2013, , .		0
93	A scalable FFT processor architecture for OFDM based communication systems. , 2013, , .		5
94	Exploiting RSS measurements among neighbouring devices: A matter of trust. , 2013, , .		1
95	Evaluation of WCDMA receiver baseband processing on a Multi-Processor System-On-Chip. , 2013, , .		0
96	Event Report. International Journal of Embedded and Real-Time Communication Systems, 2013, 4, 85-89.	0.3	0
97	Application Workload Modelling via Run-Time Performance Statistics. International Journal of Embedded and Real-Time Communication Systems, 2013, 4, 1-35.	0.3	1
98	The role of the propagation environment in RSS-based indoor positioning using mass market devices. , 2012, , .		3
99	Human-Induced Effects on RSS Ranging Measurements for Cooperative Positioning. International Journal of Navigation and Observation, 2012, 2012, 1-13.	0.8	29
100	Profiling of GNSS receiver navigation software on embedded processor. , 2012, , .		0
101	Effects of scaling a coarse-grain reconfigurable array on power and energy consumption. , 2012, , .		7
102	Energy and power estimation of Coarse-Grain Reconfigurable Array based Fast Fourier Transform accelerators. , 2012, , .		5
103	Bandpass-sampling based GNSS sampled data generator — A design perspective. , 2012, , .		2
104	Reconfigurable multi-processor architecture for streaming applications. , 2012, , .		1
105	Improving logic-to-memory ratio in an embedded Multi-Processor system via code compression. , 2012, , .		0
106	Designing Fast Fourier Transform Accelerators for Orthogonal Frequency-Division Multiplexing Systems. Journal of Signal Processing Systems, 2012, 69, 161-171.	1.4	20
107	Optimizing off-chip memory access costs in low power MPEG-4 decoder. , 2012, , .		0
108	International Conference on Localization and Global Navigation Satellite Systems 2011. International Journal of Embedded and Real-Time Communication Systems, 2012, 3, 88-93.	0.3	0

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109	International Symposium on System-on-Chip 2011. International Journal of Embedded and Real-Time Communication Systems, 2012, 3, 83-90.	0.3	0
110	GNSS baseband processing in a multi-core platform. , 2011, , .		5
111	Application-driven dimensioning of a Coarse-Grain Reconfigurable Array. , 2011, , .		6
112	Relative positioning of mass market devices in ad-hoc networks. , 2011, , .		4
113	Analyzing transport and MAC layer in system-level performance simulation. , 2011, , .		2
114	Local oscillator phase noise effects on phase angle component of GNSS code correlation. , 2011, , .		5
115	Efficient FFT pruning algorithm for non-contiguous OFDM systems. , 2011, , .		2
116	Hand-grip and body-loss impact on RSS measurements for localization of mass market devices. , 2011, , .		20
117	Improving Reconfigurable Hardware Energy Efficiency and Robustness via DVFS-Scaled Homogeneous MP-SoC. , 2011, , .		10
118	International Symposium on System-on-Chip 2010. International Journal of Embedded and Real-Time Communication Systems, 2011, 2, 38-45.	0.3	0
119	State of the art baseband DSP platforms for Software Defined Radio: A survey. Eurasip Journal on Wireless Communications and Networking, 2011, 2011, .	1.5	26
120	Implementation of W-CDMA Cell Search on a Highly Parallel and Scalable MPSoC. Journal of Signal Processing Systems, 2011, 64, 137-148.	1.4	5
121	System Level Performance Simulation of Distributed GENESYS Applications on Multi-core Platforms. , 2011, , .		1
122	Performance evaluation of distributed NoTA applications on multi-core platforms. , 2011, , .		2
123	CRISP: Cutting Edge Reconfigurable ICs for Stream Processing. , 2011, , 211-237.		18
124	Message from Conference Chairs. , 2010, , .		0
125	51.4: 3D Video Framework Design for FVV Realization. Digest of Technical Papers SID International Symposium, 2010, 41, 770.	0.1	0
126	Energy-Efficient Fast Fourier Transforms for Cognitive Radio Systems. IEEE Micro, 2010, 30, 66-76.	1.8	18

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127	Parameterized MAC unit generation for a scalable embedded DSP core. Microprocessors and Microsystems, 2010, 34, 138-150.	1.8	7
128	A coarse-grain reconfigurable architecture for multimedia applications supporting subword and floating-point calculations. Journal of Systems Architecture, 2010, 56, 38-47.	2.5	12
129	Parameterized decompression hardware for a program memory compression system. , 2010, , .		2
130	A case study of hierarchically heterogeneous application modelling using UML and Ptolemy II. , 2010, , .		0
131	Evaluating the impact of communication latency on applications running over on-chip multiprocessing platforms: A layered approach. , 2010, , .		1
132	From Y-chart to seamless integration of application design and performance simulation. , 2010, , .		3
133	High-performance NoC Interface with interrupt batching for Micronmesh MPSoC prototype platform on FPGA. , 2010, , .		2
134	Flexible hardware implementation of collaborative GNSS tracking channel. , 2010, , .		2
135	FFT Algorithms Evaluation on a Homogeneous Multi-processor System-on-Chip. , 2010, , .		9
136	Homogeneous MPSoC as baseband signal processing engine for OFDM systems. , 2010, , .		14
137	Instantiating GENESYS Application Architecture Modeling via UML 2.0 Constructs and MARTE Profile. , 2010, , .		1
138	Wideband, high gain, high linearity, low noise amplifier for GNSS frequencies with compensation for low frequency instability. , 2010, , .		6
139	Ad-hoc networks aiding indoor calibrations of heterogeneous devices for Fingerprinting applications. , 2010, , .		14
140	A cooperative framework for path loss calibration and indoor mobile positioning. , 2010, , .		8
141	Exploiting control management to accelerate Radix-4 FFT on a reconfigurable platform. , 2010, , .		9
142	Control Techniques for Coupling a Coarse-Grain Reconfigurable Array with a Generic RISC Core. , 2010, , .		2
143	Evaluation of Radix-2 and Radix-4 FFT processing on a reconfigurable platform. , 2010, , .		14
144	Model-based design flow for NoC-based MPSoCs. , 2010, , .		0

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145	Implementation and benchmarking of FFT algorithms on multicore platforms. , 2010, , .		3
146	TUTGNSS University based hardware/software GNSS receiver for research purposes. , 2010, , .		10
147	GRAMMAR: Challenges and solutions for multi-constellation Mass Market user Receivers. , 2010, , .		2
148	Vector tracking loop design for degraded signal environment. , 2010, , .		11
149	Joint Validation of Application Models and Multi-Abstraction Network-on-Chip Platforms. International Journal of Embedded and Real-Time Communication Systems, 2010, 1, 86-101.	0.3	4
150	Implementation of FFT on General-Purpose Architectures for FPGA. International Journal of Embedded and Real-Time Communication Systems, 2010, 1, 24-43.	0.3	0
151	Characterising embedded applications using a UML profile. , 2009, , .		5
152	Minimizing area costs in GPS applications on a programmable DSP by code compression. , 2009, , .		3
153	Multicore Software-Defined Radio Architecture for GNSS Receiver Signal Processing. Eurasip Journal on Embedded Systems, 2009, 2009, 1-10.	1.2	21
154	A reconfigurable SoC tailored to Software Defined Radio applications. , 2009, , .		14
155	Implementation of the W-CDMA cell search on a MPSOC designed for software defined radios. , 2009, , .		4
156	CREMA: A coarse-grain reconfigurable array with mapping adaptiveness. , 2009, , .		26
157	Mapping of the FFT on a reconfigurable architecture targeted to SDR applications. , 2009, , .		8
158	A switched interconnection infrastructure to tightly-couple a RISC processor core with a coarse grain reconfigurable array. , 2009, , .		3
159	NoC Interface for fault-tolerant Message-Passing communication on Multiprocessor SoC platform. , 2009, , .		6
160	A novel virtual frame synthesis approach for FVV. , 2009, , .		1
161	Implementation of a 64-point FFT on a Multi-Processor System-on-Chip. , 2009, , .		9
162	Implementation of W-CDMA cell search on a runtime reconfigurable coarse-grain array. , 2009, , .		1

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163	Physical realization oriented area-power-delay tradeoff exploration. , 2009, , .		1
164	Optimal dual frequency combination for Galileo mass market receiver baseband. , 2009, , .		11
165	Fault-tolerant communication over Micronmesh NOC with Micron Message-Passing protocol. , 2009, , .		7
166	Realization of Free Viewpoint TV Based on Improved MVC. Lecture Notes in Computer Science, 2009, , 143-151.	1.0	2
167	A coarse-grain reconfigurable architecture for multimedia applications featuring subword computation capabilities. Journal of Real-Time Image Processing, 2008, 3, 21-32.	2.2	31
168	Design space exploration of an open-source, IP-reusable, scalable floating-point engine for embedded applications. Journal of Systems Architecture, 2008, 54, 1143-1154.	2.5	7
169	Implementation of a floating-point matrix-vector multiplication on a reconfigurable architecture. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	10
170	Micronmesh for fault-tolerant GALS Multiprocessors on FPGA. , 2008, , .		4
171	Parameterized MAC unit generation for a scalable embedded DSP core. , 2008, , .		2
172	A dedicated DMA logic addressing a time multiplexed memory to reduce the effects of the system bus bottleneck. , 2008, , .		20
173	Reconfigurable hardware: The holy grail of matching performance with programming productivity. , 2008, , .		4
174	Validation of executable application models mapped onto network-on-chip platforms. , 2008, , .		11
175	Multiple Gate Delay Tracking Structures for GNSS Signals and Their Evaluation with Simulink, SystemC, and VHDL. International Journal of Navigation and Observation, 2008, 2008, 1-17.	0.8	27
176	A simplified executable model to evaluate latency and throughput of networks-on-chip. , 2008, , .		12
177	Improving the Efficiency of Run Time Reconfigurable Devices by Configuration Locking. , 2008, , .		2
178	Implementation of W-CDMA slot synchronization on a reconfigurable System-on-Chip. , 2008, , .		3
179	Specification of GNSS application for multiprocessor platform. , 2008, , .		2
180	GNSS Receiver Reference Design. , 2008, , .		4

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181	2008 International symposium on System-on-Chip proceedings. , 2008, , .		0
182	Design Flow Instantiation for Run-Time Reconfigurable Systems: A Case Study. Eurasip Journal on Embedded Systems, 2008, 2008, 1-9.	1.2	6
183	Code compression in DSP processor systems. International Journal of Embedded Systems, 2008, 3, 256.	0.2	3
184	Comparing Two Non-Blocking Concurrent Data Switching Schemes for Network-on-Chip. , 2007, , .		1
185	Hierarchically Heterogeneous Network-on-Chip. , 2007, , .		24
186	A Configuration Locking Technique to Reduce the Configuration Overhead of Run-Time Reconfigurable Devices. , 2007, , .		0
187	Processor Design. , 2007, , .		12
188	Modeling A Code-Division Multiple-Access Network-on-Chip using SystemC. , 2007, , .		0
189	System-Level Design for Partially Reconfigurable Hardware. , 2007, , .		0
190	Hardware platform for software-defined WCDMA/OFDM baseband receiver implementation. IET Computers and Digital Techniques, 2007, 1, 640.	0.9	4
191	Applying CDMA Technique to Network-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 1091-1100.	2.1	50
192	A Genetic Algorithm for Scheduling Tasks onto Dynamically Reconfigurable Hardware. , 2007, , .		8
193	Using Dynamic Voltage Scaling to Reduce the Configuration Energy of Run Time Reconfigurable Devices. , 2007, , .		6
194	Implementation of a tracking channel of a GPS receiver on a reconfigurable machine. , 2007, , .		2
195	Comparison of a Ring On-Chip Network and a Code-Division Multiple-Access On-Chip Network. VLSI Design, 2007, 2007, 1-14.	0.5	4
196	Static scheduling techniques for dependent tasks on dynamically reconfigurable devices. Journal of Systems Architecture, 2007, 53, 861-876.	2.5	33
197	General-Purpose Embedded Processor Cores â€“ The COFFEE RISC Example. , 2007, , 83-100.		38
198	Coprocessor Approach to Accelerating Multimedia Applications. , 2007, , 209-228.		0

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199	Future Directions in Processor Design. , 2007, , 483-485.		0
200	Embedded Computer Architecture Fundamentals. , 2007, , 7-26.		0
201	Programming Tools for Reconfigurable Processors. , 2007, , 427-446.		0
202	System Level Simulations. , 2007, , 405-426.		0
203	Processor Design Flow. , 2007, , 69-82.		1
204	On-Line Reconfigurable XGFT Network-on-Chip Designed for Improving the Fault-Tolerance and Manufacturability of the MPSoC Chips. , 2006, , .		2
205	Extensible and Configurable Processors for System-on-Chip Design. , 2006, , .		5
206	Using Constraint Programming to Achieve Optimal Prefetch Scheduling for Dependent Tasks on Run-Time Reconfigurable Devices. , 2006, , .		2
207	SystemC Model of an Interoperative GPS/Galileo Code Correlator Channel. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2006, , .	0.0	3
208	A RTL Asynchronous FIFO Design Using Modified Micropipeline. International Biennial Baltic Electronics Conference, 2006, , .	0.0	8
209	Prototyping a Globally Asynchronous Locally Synchronous Network-On-Chip on a Conventional FPGA Device Using Synchronous Design Tools. , 2006, , .		7
210	Design And Verification of a VHDL Model of a Floating-Point Unit for a RISC Microprocessor. , 2006, , .		0
211	Performance enhancements for embedded software implementation of GNSS navigation algorithms. , 2006, , .		0
212	From Buses to Networks. , 2005, , 231-251.		4
213	Flexible Implementation of a WCDMA Rake Receiver. Journal of Signal Processing Systems, 2005, 39, 147-160.	1.0	19
214	A Brunch from the Coffee Table-Case Study in NoC Platform Design. , 2005, , 425-453.		5
215	Arbitration and Routing Schemes for on-Chip Packet Networks. , 2005, , 253-282.		4
216	DSPxPlore. , 2004, , .		8

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217	Issues in the development of a practical NoC: the Proteo concept. The Integration VLSI Journal, 2004, 38, 95-105.	1.3	30
218	A scalable instruction buffer and align unit for xDSPcore. IEEE Journal of Solid-State Circuits, 2004, 39, 1094-1100.	3.5	4
219	Topology optimization for application-specific networks-on-chip. , 2004, , .		69
220	An IP-Based On-Chip Packet-Switched Network. , 2003, , 193-213.		7
221	Comparison of bulk and SOI CMOS technologies in a DSP processor circuit implementation. , 2001, , .		15
222	A flexible DSP core for embedded systems. IEEE Design and Test of Computers, 1997, 14, 60-68.	1.4	19
223	A flexible RAKE receiver architecture for WCDMA mobile terminals. , 0, , .		10
224	Interconnect IP node for future system-on-chip designs. , 0, , .		38
225	VHDL-based simulation environment for Proteo NoC. , 0, , .		23
226	Flexible implementation of a WCDMA Rake receiver. , 0, , .		9
227	Advanced instruction set architectures for reducing program memory usage in a DSP processor. , 0, , .		3
228	Scaleable shadow stack for a configurable DSP concept. , 0, , .		3
229	Variable-length instruction compression for area minimization. , 0, , .		2
230	A scaleable instruction buffer for a configurable DSP core. , 0, , .		3
231	Block-wise extraction of Rent's exponents for an extensible processor. , 0, , .		2
232	FSEL - selective predicated execution for a configurable DSP core. , 0, , .		5
233	Topology design for global link optimization in application specific network-on-chips. , 0, , .		0
234	A programmable baseband receiver platform for WCDMA/OFDM mobile terminals. , 0, , .		8

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235	Fault-tolerant XGFT network-on-chip for multi-processor system-on-chip circuits. , 0, , .		15
236	Asynchronous network node design for network-on-chip. , 0, , .		4
237	The SoC-Mobinet Model in System-on-Chip Education. , 0, , .		2
238	A flexible multiplier for media processing. , 0, , .		4
239	Integration of a noc-based multimedia processing platform. , 0, , .		2
240	An efficient approach to hide the run-time reconfiguration from SW applications. , 0, , .		0
241	Fault-tolerant 2-D Mesh Network-On-Chip for MultiProcessor Systems-on-Chip. , 0, , .		5
242	Ad Hoc Networks for Cooperative Mobile Positioning. , 0, , .		4
243	Implementation of FFT on General-Purpose Architectures for FPGA. , 0, , 156-175.		0
244	Joint Validation of Application Models and Multi-Abstraction Network-on-Chip Platforms. , 0, , 263-277.		0
245	Implementation of FFT on General-Purpose Architectures for FPGA. , 0, , 658-676.		0