Sheldon Tan

List of Publications by Year in Descending Order

220 papers	1,583 citations	18 h-index	28 g-index
269 ext. papers	2,025 ext. citations	1.9 avg, IF	4.97 L-index

#	Paper	IF	Citations
220	Electrothermal Simulation and Optimal Design of Thermoelectric Cooler using Analytical Approach. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	
219	EM Lifetime Constrained Optimization for Multi-Segment Power Grid Networks. *Embedded Systems*, **2021**, 365-383		0
218	Runtime Long-Term Reliability Management Using Stochastic Computing in Deep Neural Networks **2021**,		1
217	The 2021 Asia and South Pacific Design Automation Conference (ASPDAC). *IEEE Design and Test*, **2021**, 38, 121-122	1.4	
216	Fast Physics-Based Electromigration Analysis for Full-Chip Networks by Efficient Eigenfunction-Based Solution. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 507-520	2.5	1
215	A Fast Semi-Analytic Approach for Combined Electromigration and Thermomigration Analysis for General Multisegment Interconnects. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 350-363	2.5	1
214	Robust power grid network design considering EM aging effects for multi-segment wires. *The Integration VLSI Journal*, **2021**, 77, 38-47	1.4	0
213	Post-Silicon Heat-Source Identification and Machine-Learning-Based Thermal Modeling Using Infrared Thermal Imaging. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 694-707	2.5	5
212	Full-Chip Power Density and Thermal Map Characterization for Commercial Microprocessors under Heat Sink Cooling. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	0
211	Real-Time Full-Chip Thermal Tracking: A Post-Silicon, Machine Learning Perspective. *IEEE Transactions on Computers*, **2021**, 1-1	2.5	1
210	GLU3.0: Fast GPU-based Parallel Sparse LU Factorization for Circuit Simulation. *IEEE Design and Test* , **2020**, 37, 78-90	1.4	5
209	An Adaptive Electromigration Assessment Algorithm for Full-chip Power/Ground Networks **2020**,		1
208	Machine Learning Based Online Full-Chip Heatmap Estimation **2020**,		4
207	**2020**,		2
206	Interconnect Electromigration Modeling and Analysis for Nanometer ICs: From Physics to Full-Chip. *IPSJ Transactions on System LSI Design Methodology*, **2020**, 13, 42-55	0.2	0
205	HAT-DRL: Hotspot-Aware Task Mapping for Lifetime Improvement of Multicore System using Deep Reinforcement Learning **2020**,		1
204	GridNet **2020**,		5

203	EM-GAN: Data-Driven Fast Stress Analysis for Multi-Segment Interconnects **2020**,		3
202	Full-chip wire-oriented back-end-of-line TDDB hotspot detection and lifetime analysis. *The Integration VLSI Journal*, **2020**, 70, 90-98	1.4	0
201	Fast Analytic Electromigration Analysis for General Multisegment Interconnect Wires. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 421-432	2.6	5
200	Leakage-Aware Predictive Thermal Management for Multicore Systems Using Echo State Network. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 1400-1413	2.5	7
199	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 885-894	2.5	5
198	EMSpice: Physics-Based Electromigration Check Using Coupled Electronic and Stress Simulation. *IEEE Transactions on Device and Materials Reliability*, **2020**, 20, 376-389	1.6	5
197	Dynamic Reliability Management for Multi-Core Processor Based on Deep Reinforcement Learning **2019**,		1
196	Long-Term Reliability of Nanometer VLSI Systems **2019**,		8
195	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 940-953	2.6	5
194	Hot Spot Identification and System Parameterized Thermal Modeling for Multi-Core Processors Through Infrared Thermal Imaging **2019**,		4
193	Reliability based hardware Trojan design using physics-based electromigration models. *The Integration VLSI Journal*, **2019**, 66, 9-15	1.4	0
192	Saturation-Volume Estimation for Multisegment Copper Interconnect Wires. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 1666-1674	2.6	2
191	GPU-based Ising computing for solving max-cut combinatorial optimization problems. *The Integration VLSI Journal*, **2019**, 69, 335-344	1.4	9
190	Compact EM Models for Multi-Segment Interconnect Wires **2019**, 121-151		
189	Dynamic EM Models for Transient Stress Evolution and Recovery **2019**, 97-120		
188	Physics-Based EM Modeling **2019**, 13-45		
187	Learning-Based DRM and Energy Optimization for Manycore Dark Silicon Processors **2019**, 217-245		
186	Resource-Based EM Modeling DRM for Multi-Core Microprocessors **2019**, 177-194		

185	EM Assessment for Power Grid Networks **2019**, 153-175		
184	Fast EM Stress Evolution Analysis Using Krylov Subspace Method **2019**, 47-66		
183	Fast EM Immortality Analysis for Multi-Segment Copper Interconnect Wires **2019**, 67-96		
182	. *IEEE Transactions on Computers*, **2019**, 68, 526-541	2.5	7
181	Dynamic reliability management based on resource-based EM modeling for multi-core microprocessors. *Microelectronics Journal*, **2018**, 74, 106-115	1.8	2
180	Electromigration-lifetime constrained power grid optimization considering multi-segment interconnect wires **2018**,		6
179	Physics-Based Compact TDDB Models for Low- k BEOL Copper Interconnects With Time-Varying Voltage Stressing. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 239-248	2.6	2
178	Accelerating electromigration aging for fast failure detection for nanometer ICs **2018**,		6
177	A Fast Leakage-Aware Full-Chip Transient Thermal Estimation Method. *IEEE Transactions on Computers*, **2018**, 67, 617-630	2.5	12
176	Fast Electromigration Immortality Analysis for Multisegment Copper Interconnect Wires. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 3137-3150	2.5	18
175	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 969-980	2.6	17
174	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 531-543	2.6	4
173	Recent advances in EM and BTI induced reliability modeling, analysis and optimization (invited). *The Integration VLSI Journal*, **2018**, 60, 132-152	1.4	25
172	Thermal-Sensor-Based Occupancy Detection for Smart Buildings Using Machine-Learning Methods. *ACM Transactions on Design Automation of Electronic Systems*, **2018**, 23, 1-21	1.5	16
171	Prediction of chaotic time series by using ANNs, ANFIS and SVMs **2018**,		3
170	SVM Based Intrusion Detection Using Nonlinear Scaling Scheme **2018**,		8
169	Multi-physics-based FEM analysis for post-voiding analysis of electromigration failure effects **2018**,		5
168	Postvoiding FEM Analysis for Electromigration Failure Characterization. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 2483-2493	2.6	7

167	Accelerating Electromigration Wear-Out Effects Based on Configurable Sink-Structured Wires **2018** ,		1
166	Detection of counterfeited ICs via on-chip sensor and post-fabrication authentication policy. *The Integration VLSI Journal*, **2018**, 63, 31-40	1.4	3
165	Dynamic electromigration modeling for transient stress evolution and recovery under time-dependent current and temperature stressing. *The Integration VLSI Journal*, **2017**, 58, 518-527	1.4	11
164	Energy and Lifetime Optimizations for Dark Silicon Manycore Microprocessor Considering Both Hard and Soft Errors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2561-2574	2.6	16
163	Recovery-aware proactive TSV repair for electromigration in 3D ICs **2017**,		2
162	Physics-based electromigration modeling and assessment for multi-segment interconnects in power grid networks **2017**,		16
161	Fast physics-based electromigration analysis for multi-branch interconnect trees **2017**,		6
160	. *IEEE Transactions on Device and Materials Reliability*, **2017**, 17, 653-666	1.6	13
159	Prediction of chaotic time-series with different MLE values using FPGA-based ANNs **2017**,		1
158	Comprehensive detection of counterfeit ICs via on-chip sensor and post-fabrication authentication policy **2017**,		2
157	Dynamic temperature-aware reliability modeling for multi-branch interconnect trees **2017**,		1
156	Leveraging recovery effect to reduce electromigration degradation in power/ground TSV **2017**,		3
155	Parallel GMRES solver for fast analysis of large linear dynamic systems on GPU platforms. *The Integration VLSI Journal*, **2016**, 52, 10-22	1.4	6
154	EM-Based On-Chip Aging Sensor for Detection of Recycled ICs. *IEEE Design and Test*, **2016**, 33, 56-64	1.4	6
153	Overview of cyber-physical temperature estimation in smart buildings: From modeling to measurements **2016**,		2
152	Learning-based occupancy behavior detection for smart buildings **2016**,		3
151	Finite difference method for electromigration analysis of multi-branch interconnects **2016**,		9
150	Energy-efficient wireless temperature sensoring for smart building applications **2016**,		3

149	Electromigration assessment for power grid networks considering temperature and thermal stress effects. *The Integration VLSI Journal*, **2016**, 55, 307-315	1.4	15
148	Fast stress analysis for runtime reliability enhancement of 3D IC using artificial neural network **2016**,		1
147	Electromigration recovery modeling and analysis under time-dependent current and temperature stressing **2016**,		17
146	Corrections to "GPU-Accelerated Parallel Sparse LU Factorization Method for Fast Circuit Analysis" [2015 DOI: 10.1109/TVLSI.2015.2421287]. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 1212-1212	2.6	
145	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1811-1824	2.5	30
144	Physics-Based Electromigration Models and Full-Chip Assessment for Power Grid Networks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1848-1861	2.5	49
143	Learning-based dynamic reliability management for dark silicon processor considering EM effects **2016**,		5
142	Statistical Rare-Event Analysis and Parameter Guidance by Elite Learning Sample Selection. *ACM Transactions on Design Automation of Electronic Systems*, **2016**, 21, 1-21	1.5	4
141	New power budgeting and thermal management scheme for multi-core systems in dark silicon **2016**,		5
140	Dynamic reliability management for near-threshold dark silicon processors **2016**,		4
139	Occupancy Detection in Smart Buildings Using Support Vector Regression Method **2016**,		2
138	Physics-based full-chip TDDB assessment for BEOL interconnects **2016**,		1
137	Voltage-based electromigration immortality check for general multi-branch interconnects **2016**,		13
136	Invited - Cross-layer modeling and optimization for electromigration induced reliability **2016**,		4
135	Hierarchical Dynamic Thermal Management Method for High-Performance Many-Core Microprocessors. *ACM Transactions on Design Automation of Electronic Systems*, **2016**, 22, 1-21	1.5	19
134	New electromigration modeling and analysis considering time-varying temperature and current densities **2015**,		3
133	H -Matrix-Based Finite-Element-Based Thermal Analysis for 3D ICs. *ACM Transactions on Design Automation of Electronic Systems*, **2015**, 20, 1-25	1.5	4
132	Interconnect reliability modeling and analysis for multi-branch interconnect trees **2015**,		10

131	2-matrix-based finite element linear solver for fast transient thermal analysis of high-performance ICs. *International Journal of Circuit Theory and Applications*, **2015**, 43, 1953-1970	2	
130	Task Migrations for Distributed Thermal Management Considering Transient Effects. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 397-401	2.6	29
129	Parallel Thermal Analysis of 3-D Integrated Circuits With Liquid Cooling on CPU-GPU Platforms. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 575-579	2.6	10
128	A GPU-Accelerated Parallel Shooting Algorithm for Analysis of Radio Frequency and Microwave Integrated Circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 480-492	2.6	6
127	Statistical rare event analysis using smart sampling and parameter guidance **2015**,		2
126	From robust chip to smart building: CAD algorithms and methodologies for uncertainty analysis of building performance **2015**,		5
125	Full-chip electromigration assessment: Effect of cross-layout temperature and thermal stress distributions **2015**,		1
124	EM-based on-chip aging sensor for detection and prevention of counterfeit and recycled ICs **2015**,		19
123	Learning based compact thermal modeling for energy-efficient smart building management **2015**,		4
122	Time-domain performance bound analysis for analog and interconnect circuits considering process variations **2014**,		1
121	Compact Lateral Thermal Resistance Model of TSVs for Fast Finite-Difference Based Thermal Analysis of 3-D Stacked ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1490-1502	2.5	31
120	Direct finite-element-based solver for 3D-IC thermal analysis via H-matrix representation **2014**,		2
119	Physics-based Electromigration Assessment for Power Grid Networks **2014**,		71
118	Compact thermal modeling for packaged microprocessor design with practical power maps. *The Integration VLSI Journal*, **2014**, 47, 71-85	1.4	15
117	IR-drop based electromigration assessment: Parametric failure chip-scale analysis **2014**,		15
116	Lifetime optimization for real-time embedded systems considering electromigration effects **2014**,		5
115	Battery Management and Application for Energy-Efficient Buildings **2014**,		26
114	A new segmentation-based GPU-accelerated sparse matrix-vector multiplication **2014**,		2

113	Hybrid dynamic thermal management method with model predictive control **2014**,		1
112	Dynamic thermal management for multi-core microprocessors considering transient thermal effects **2013**,		2
111	Performance bound and yield analysis for analog circuits under process variations **2013**,		2
110	Compact nonlinear thermal modeling of packaged integrated systems **2013**,		2
109	A power-driven thermal sensor placement algorithm for dynamic thermal management **2013**,		8
108	Statistical full-chip total power estimation considering spatially correlated process variations. *The Integration VLSI Journal*, **2013**, 46, 80-88	1.4	1
107	Symbolic Moment Computation for Statistical Analysis of Large Interconnect Networks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 944-957	2.6	5
106	Parallel power grid analysis using preconditioned GMRES solver on CPU-GPU platforms **2013**,		9
105	Performance bound analysis of analog circuits in frequency- and time-domain considering process variations. *ACM Transactions on Design Automation of Electronic Systems*, **2013**, 19, 1-22	1.5	6
104	Composable thermal modeling and simulation for architecture-level thermal designs of multicore microprocessors. *ACM Transactions on Design Automation of Electronic Systems*, **2013**, 18, 1-27	1.5	15
103	Compact lateral thermal resistance modeling and characterization for TSV and TSV array **2013**,		6
102	Distributed task migration for thermal hot spot reduction in many-core microprocessors **2013**,		1
101	Fast timing analysis of clock networks considering environmental uncertainty. *The Integration VLSI Journal*, **2012**, 45, 376-387	1.4	5
100	Full-chip thermal analysis of 3D ICs with liquid cooling by GPU-accelerated GMRES method **2012**,		7
99	Time-domain performance bound analysis of analog circuits considering process variations **2012**,		1
98	General Parameterized Thermal Modeling for High-Performance Microprocessor Design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 211-224	2.6	10
97	Statistical extraction and modeling of inductance considering spatial correlation. *Analog Integrated Circuits and Signal Processing*, **2012**, 73, 3-11	1.2	2
96	Symbolic nodal analysis of analog integrated circuits using pathological elements **2012**,		4

95	Transient analysis of large linear dynamic networks on hybrid GPU-multicore platforms **2012**,		3
94	Decentralized and Passive Model Order Reduction of Linear Networks With Massive Ports. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 865-877	2.6	6
93	Localized relaxation theory of circuits and its applications in electro-thermal analyses. *Science China Information Sciences*, **2012**, 55, 938-950	3.4	
92	Compact Modeling of Interconnect Circuits over Wide Frequency Band by Adaptive Complex-Valued Sampling Method. *ACM Transactions on Design Automation of Electronic Systems*, **2012**, 17, 1-22	1.5	5
91	Fast Statistical Full-Chip Leakage Analysis for Nanometer VLSI Systems. *ACM Transactions on Design Automation of Electronic Systems*, **2012**, 17, 1-19	1.5	5
90	Parallel statistical analysis of analog circuits by GPU-accelerated graph-based approach **2012**,		1
89	Thermal characterization of TSV based 3D stacked ICs **2012**,		7
88	A new voltage binning technique for yield improvement based on graph theory **2012**,		4
87	Statistical Capacitance Modeling and Extraction **2012**, 163-182		
86	Statistical Power Grid Analysis by Variational Subspace Method **2012**, 145-159		
85	Voltage Binning Technique for Yield Optimization **2012**, 273-286		
84	Statistical Total Power Estimation Techniques **2012**, 93-103		
83	Statistical Power Grid Analysis Considering Log-Normal Leakage Current Variations **2012**, 107-126		
82	Linear Statistical Leakage Analysis by Virtual Grid-Based Modeling **2012**, 65-82		
81	Statistical Dynamic Power Estimation Techniques **2012**, 83-92		
80	Statistical Power Grid Analysis by Stochastic Extended Krylov Subspace Method **2012**, 127-144		
79	Fundamentals of Statistical Analysis **2012**, 15-36		
78	Statistical Yield Analysis and Optimization **2012**, 253-272		

77	Statistical Inductance Modeling and Extraction **2012**, 209-218		
76	Statistical Leakage Power Analysis by Spectral Stochastic Method **2012**, 55-63		
75	Statistical Performance Analysis and Modeling Techniques for Nanometer VLSI Designs **2012**,		16
74	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2011**, 58, 1382-1395	3.9	84
73	Full-chip runtime error-tolerant thermal estimation and prediction for practical thermal management **2011**,		10
72	Statistical full-chip dynamic power estimation considering spatial correlations **2011**,		4
71	Performance bound analysis of analog circuits considering process variations **2011**,		11
70	An efficient statistical chip-level total power estimation method considering process variations with spatial correlation **2011**,		3
69	A structured parallel periodic Arnoldi shooting algorithm for RF-PSS analysis based on GPU platforms **2011**,		2
68	A robust periodic arnoldi shooting algorithm for efficient analysis of large-scale RF/MM ICs **2010**,		3
67	Symbolic noise analysis of low voltage amplifiers by using nullors **2010**,		3
66	Fast Analysis of a Large-Scale Inductive Interconnect by Block-Structure-Preserved Macromodeling. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1399-1411	2.6	8
65	General behavioral thermal modeling and characterization for multi-core microprocessor design **2010**,		9
64	Parameterized architecture-level dynamic thermal models for multicore microprocessors. *ACM Transactions on Design Automation of Electronic Systems*, **2010**, 15, 1-22	1.5	16
63	Passive Rational Interpolation-Based Reduction via Carath□dory Extension for General Systems. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2010**, 57, 750-755	3.5	2
62	Variational Capacitance Extraction and Modeling Based on Orthogonal Polynomial Method. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1556-1566	2.6	17
61	Composable thermal modeling and characterization for fast temperature estimation **2010**,		2
60	Statistical extraction and modeling of 3-D inductance with spatial correlation **2010**,		2

59	Efficient model reduction of interconnects via double gramians approximation **2010**,		3
58	A fast analog mismatch analysis by an incremental and stochastic trajectory piecewise linear macromodel **2010**,		2
57	Symbolic analysis of analog circuits containing voltage mirrors and current mirrors. *Analog Integrated Circuits and Signal Processing*, **2010**, 65, 89-95	1.2	39
56	Statistical modeling and analysis of chip-level leakage power by spectral stochastic method. *The Integration VLSI Journal*, **2010**, 43, 156-165	1.4	7
55	Statistical analysis of large on-chip power grid networks by variational reduction scheme. *The Integration VLSI Journal*, **2010**, 43, 167-175	1.4	2
54	Recent advance in non-Krylov subspace model order reduction of interconnect circuits. *Tsinghua Science and Technology*, **2010**, 15, 151-168	3.4	2
53	A linear algorithm for full-chip statistical leakage power analysis considering weak spatial correlation **2010**,		12
52	GPU friendly fast Poisson solver for structured power grid network analysis **2009**,		24
51	Multiple block structure-preserving reduced order modeling of interconnect circuits. *The Integration VLSI Journal*, **2009**, 42, 158-168	1.4	2
50	Hierarchical Krylov subspace based reduction of large interconnects. *The Integration VLSI Journal*, **2009**, 42, 193-202	1.4	3
49	Fast analysis of nontree-clock network considering environmental uncertainty by parameterized and incremental macromodeling **2009**,		2
48	Statistical analysis of on-chip power grid networks by variational extended truncated balanced realization method **2009**,		2
47	Architecture-Level Thermal Characterization for Multicore Microprocessors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 1495-1507	2.6	9
46	Symbolic formulation method for mixed-mode analog circuits using nullors **2009**,		9
45	Statistical modeling and analysis of chip-level leakage power by spectral stochastic method **2009**,		1
44	Fast Analysis of On-Chip Power Grid Circuits by Extended Truncated Balanced Realization Method. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2009**, E92-A, 3061-3069	0.4	2
43	Efficient statistical analysis method of power/ground (P/G) network. *Progress in Natural Science: Materials International*, **2008**, 18, 189-196	3.6	1
42	Vector Edge Detection in H.264 Implementation **2008**,		1

41	Fast Variational Analysis of On-Chip Power Grids by Stochastic Extended Krylov Subspace Method. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2008**, 27, 1996-2006	2.5	19
40	ETBR: Extended Truncated Balanced Realization Method for On-Chip Power Grid Network Analysis **2008**,		3
39	Random Walk Guided Decap Embedding for Power/Ground Network Optimization. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2008**, 55, 36-40	3.5	
38	Parameterized transient thermal behavioral modeling for chip multiprocessors **2008**,		1
37	Statistical Analysis of On-Chip Power Delivery Networks Considering Lognormal Leakage Current Variations With Spatial Correlation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2008** , 55, 2064-2075	3.9	17
36	Architecture-level thermal behavioral characterization for multi-core microprocessors **2008**,		1
35	Second-Order Balanced Truncation for Passive-Order Reduction of RLCK Circuits. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2008**, 55, 942-946	3.5	22
34	Statistic Analysis of Power/Ground Networks Using Single-Node SOR Method **2008**,		1
33	Variational capacitance modeling using orthogonal polynomial method **2008**,		8
32	ETBR **2008**,		14
31	Modeling and simulation for on-chip power grid networks by locally dominant Krylov subspace method **2008**,		1
30	Large scale P/G grid transient simulation using hierarchical relaxed approach. *The Integration VLSI Journal*, **2008**, 41, 153-160	1.4	2
29	An efficient terminal and model order reduction algorithm. *The Integration VLSI Journal*, **2008**, 41, 210-218	1.4	13
28	Practical Implementation of Stochastic Parameterized Model Order Reduction via Hermite Polynomial Chaos **2007**,		15
27	General Block Structure-Preserving Reduced Order Modeling of Linear Dynamic Circuits **2007**,		2
26	Improving the reliability of on-chip data caches under process variations **2007**,		4
25	Minimum Decoupling Capacitor Insertion in VLSI Power/Ground Supply Networks by Semidefinite and Linear Programs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2007**, 15, 1284-1287	2.6	
24	Passive Interconnect Macromodeling Via Balanced Truncation of Linear Systems in Descriptor Form **2007**,		8

23	Partitioning-based decoupling capacitor budgeting via sequence of linear programming. *The Integration VLSI Journal*, **2007**, 40, 516-524	1.4	1
22	Passive Modeling of Interconnects by Waveform Shaping **2007**,		3
21	Fast Decoupling Capacitor Budgeting for Power/Ground Network Using Random Walk Approach **2007**,		1
20	Statistical Model Order Reduction for Interconnect Circuits Considering Spatial Correlations **2007**,		5
19	Efficient power modeling and software thermal sensing for runtime temperature monitoring. *ACM Transactions on Design Automation of Electronic Systems*, **2007**, 12, 1-29	1.5	24
18	SBPOR. *Proceedings - Design Automation Conference*, **2007**,		5
17	Pattern-Based Iterative Method for Extreme Large Power/Ground Analysis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 680-692	2.5	12
16	TermMerg: An Efficient Terminal-Reduction Method for Interconnect Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 1382-1392	2.5	8
15	Stochastic extended Krylov subspace method for variational analysis of on-chip power grid networks. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2007**,		1
14	Advanced Model Order Reduction Techniques in VLSI Design **2007**,		57
13	Nonlinear Transient and Distortion Analysis via Frequency Domain Volterra Series. *Circuits, Systems, and Signal Processing*, **2006**, 25, 295-314	2.2	10
12	Efficient decoupling capacitor planning via convex programming methods **2006**,		6
11	A systematic method for functional unit power estimation in microprocessors **2006**,		33
10	High accurate pattern based precondition method for extremely large power/ground grid analysis **2006**,		3
9	Symbolic Analysis of Analog Circuits By Boolean Logic Operations. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2006**, 53, 1313-1317		17
8	Statistical Analysis of Power Grid Networks Considering Lognormal Leakage Current Variations with Spatial Correlation. *Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors*, **2006**,		3
7	Fast Thermal Simulation for Runtime Temperature Tracking and Management. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2006**, 25, 2882-2893	2.5	16
6	**2006**,		7

5	Simulation of Power Grid Networks Considering Wires and Lognormal Leakage Current Variations **2006**,		5
4	An Extended SVD-based Terminal and Model Order Reduction Algorithm **2006**,		6
3	Partitioning-based approach to fast on-chip decap budgeting and minimization **2005**,		25
2	Balanced multi-level multi-way partitioning of analog integrated circuits for hierarchical symbolic analysis. *The Integration VLSI Journal*, **2003**, 34, 65-86	1.4	1
1	Fast thermal simulation for architecture level dynamic thermal management		7