Yuan Xie

List of Publications by Year in Descending Order

142 papers	4,162 citations	34 h-index	61 g-index
161 ext. papers	5,584 ext. citations	4 avg, IF	5.71 L-index

#	Paper	IF	Citations
142	SDP: Co-Designing Algorithm, Dataflow, and Architecture for in-SRAM Sparse NN Acceleration. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2022**, 1-1	2.5	
141	Practical Near-Data-Processing Architecture for Large-Scale Distributed Graph Neural Network. *IEEE Access*, **2022**, 10, 46796-46807	3.5	
140	H2Learn: High-Efficiency Learning Accelerator for High-Accuracy Spiking Neural Networks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	2
139	PLSAV: Parallel loop searching and verifying for loop closure detection. *IET Intelligent Transport Systems*, **2021**, 15, 683-698	2.4	0
138	Fast Search of the Optimal Contraction Sequence in Tensor Networks. *IEEE Journal on Selected Topics in Signal Processing*, **2021**, 15, 574-586	7.5	2
137	Practical Attacks on Deep Neural Networks by Memory Trojaning. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 1230-1243	2.5	4
136	Evolver: A Deep Learning Processor With On-Device Quantization–Voltage–Frequency Tuning. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 658-673	5.5	17
135	DLUX: A LUT-Based Near-Bank Accelerator for Data Center Deep Learning Training Workloads. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 1586-1599	2.5	3
134	Hardware Acceleration for GCNs via Bidirectional Fusion. *IEEE Computer Architecture Letters*, **2021**, 1-1	1.8	0
133	STPAcc: Structural TI-based Pruning for Accelerating Distance-related Algorithms on CPU-FPGA Platforms. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	1
132	Rubik: A Hierarchical Architecture for Efficient Graph Neural Network Training. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	2
131	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 2049-2062	2.5	2
130	Power-efficient neural network with artificial dendrites. *Nature Nanotechnology*, **2020**, 15, 776-782	28.7	55
129	Training high-performance and large-scale deep neural networks with full 8-bit integers. *Neural Networks*, **2020**, 125, 70-82	9.1	17
128	Characterizing and Understanding GCNs on GPU. *IEEE Computer Architecture Letters*, **2020**, 19, 22-25	1.8	14
127	HyGCN: A GCN Accelerator with Hybrid Architecture **2020**,		41
126	A Case for 3D Integrated System Design for Neuromorphic Computing and AI Applications. *International Journal of Semantic Computing*, **2020**, 14, 457-475	0.7	1

125	iPIM: Programmable In-Memory Image Processing Accelerator Using Near-Bank Architecture **2020**,		12
124	Comparing SNNs and RNNs on neuromorphic vision datasets: Similarities and differences. *Neural Networks*, **2020**, 132, 108-120	9.1	15
123	Rethinking the performance comparison between SNNS and ANNS. *Neural Networks*, **2020**, 121, 294-307	9.1	49
122	SemiMap: A Semi-Folded Convolution Mapping for Speed-Overhead Balance on Crossbars. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 117-130	2.5	7
121	CORN: In-Buffer Computing for Binary Neural Network **2019**,		5
120	DASM: Data-Streaming-Based Computing in Nonvolatile Memory Architecture for Embedded System. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 2046-2059	2.6	8
119	NNBench-X: Benchmarking and Understanding Neural Network Workloads for Accelerator Designs. *IEEE Computer Architecture Letters*, **2019**, 18, 38-42	1.8	3
118	An Instruction Set Architecture for Machine Learning. *ACM Transactions on Computer Systems*, **2019**, 36, 1-35	1.1	5
117	Memory-Bound Proof-of-Work Acceleration for Blockchain Applications **2019**,		2
116	PXNOR-BNN: In/With Spin-Orbit Torque MRAM Preset-XNOR Operation-Based Binary Neural Networks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 2668-2679	2.6	20
115	Towards artificial general intelligence with hybrid Tianjic chip architecture. *Nature*, **2019**, 572, 106-111	50.4	215
114	Alleviating Irregularity in Graph Analytics Acceleration **2019**,		27
113	Memory Trojan Attack on Neural Network Accelerators **2019**,		14
112	Towards a polynomial algorithm for optimal contraction sequence of tensor networks from trees. *Physical Review E*, **2019**, 100, 043309	2.4	2
111	GraphH: A Processing-in-Memory Architecture for Large-Scale Graph Processing. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 640-653	2.5	33
110	TIME: A Training-in-Memory Architecture for RRAM-Based Deep Neural Networks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 834-847	2.5	32
109	An Adaptive 3T-3MTJ Memory Cell Design for STT-MRAM-Based LLCs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 484-495	2.6	11
108	AIM: Fast and energy-efficient AES in-memory implementation for emerging non-volatile main memory **2018**,		9

107	Bridge the Gap between Neural Networks and Neuromorphic Hardware with a Neural Network Compiler **2018**,		24
106	Memory that never forgets: emerging nonvolatile memory and the implication for architecture design. *National Science Review*, **2018**, 5, 577-592	10.8	10
105	Stuck-at Fault Tolerance in RRAM Computing Systems. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2018**, 8, 102-115	5.2	46
104	Fast Object Tracking on a Many-Core Neural Network Chip. *Frontiers in Neuroscience*, **2018**, 12, 841	5.1	5
103	Packet Pump: Overcoming Network Bottleneck in On-Chip Interconnects for GPGPUs* **2018**,		1
102	Securing Emerging Nonvolatile Main Memory With Fast and Energy-Efficient AES In-Memory Implementation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 2443-2455	2.6	5
101	Spendthrift: Machine learning based resource and frequency scaling for ambient energy harvesting nonvolatile processors **2017**,		13
100	Building energy-efficient multi-level cell STT-RAM caches with data compression **2017**,		9
99	Dynamic Power and Energy Management for Energy Harvesting Nonvolatile Processor Systems. *Transactions on Embedded Computing Systems*, **2017**, 16, 1-23	1.8	13
98	Thermomechanical Stress-Aware Management for 3-D IC Designs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2678-2682	2.6	8
97	Cost-effective design of scalable high-performance systems using active and passive interposers **2017**,		36
96	MNSIM: Simulation Platform for Memristor-Based Neuromorphic Computing System. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 1-1	2.5	12
95	A Study on Practically Unlimited Endurance of STT-MRAM. *IEEE Transactions on Electron Devices*, **2017**, 64, 3639-3646	2.9	43
94	DRISA **2017**,		112
93	**2017**,		8
92	Scalable memory fabric for silicon interposer-based multi-core systems **2016**,		10
91	Cambricon: An Instruction Set Architecture for Neural Networks **2016**,		46
90	Cost and Thermal Analysis of High-Performance 2.5D and 3D Integrated Circuit Design Space **2016**,		7

89	PRIME: A Novel Processing-in-Memory Architecture for Neural Network Computation in ReRAM-Based Main Memory **2016**,		153
88	Mellow Writes: Extending Lifetime in Resistive Memories through Selective Slow Write Backs **2016**,		22
87	BACH: A Bandwidth-Aware Hybrid Cache Hierarchy Design with Nonvolatile Memories. *Journal of Computer Science and Technology*, **2016**, 31, 20-35	1.7	3
86	Architecture design with STT-RAM: Opportunities and challenges **2016**,		18
85	PRIME. *Computer Architecture News*, **2016**, 44, 27-39		482
84	MNSIM: Simulation platform for memristor-based neuromorphic computing system **2016**,		15
83	A Real-Time and Energy-Efficient Implementation of Difference-of-Gaussian with Flexible Thin-Film Transistors **2016**,		1
82	Pinatubo **2016**,		200
81	NEUTRAMS: Neural network transformation and co-design under neuromorphic hardware constraints **2016**,		37
80	Adapting $text{B}^{+}$ -Tree for Emerging Nonvolatile Memory-Based Main Memory. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1461-1474	2.5	3
79	Hybrid Drowsy SRAM and STT-RAM Buffer Designs for Dark-Silicon-Aware NoC. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 3041-3054	2.6	19
78	Heterogeneous architecture design with emerging 3D and non-volatile memory technologies **2015**,		1
77	Exploring memory controller configurations for many-core systems with 3D stacked DRAMs **2015**,		2
76	Modeling framework for cross-point resistive memory design emphasizing reliability and variability issues **2015**,		4
75	Whitespace-Aware TSV Arrangement in 3-D Clock Tree Synthesis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 1842-1853	2.6	2
74	Nonvolatile memory allocation and hierarchy optimization for high-level synthesis **2015**,		3
73	NVMain 2.0: A User-Friendly Memory Simulator to Model (Non-)Volatile Memory Systems. *IEEE Computer Architecture Letters*, **2015**, 14, 140-143	1.8	92
72	Dynamic machine learning based matching of nonvolatile processor microarchitecture to harvested energy profile **2015**,		15

71	Impact of Write Pulse and Process Variation on 22 nm FinFET-Based STT-RAM Design: A Device-Architecture Co-Optimization Approach. *IEEE Transactions on Multi-Scale Computing Systems* , **2015**, 1, 195-206		22
70	Building energy-efficient multi-level cell STT-MRAM based cache through dynamic data-resistance encoding **2014**,		14
69	Efficient region-aware P/G TSV planning for 3D ICs **2014**,		5
68	PS3-RAM: A Fast Portable and Scalable Statistical STT-RAM Reliability/Energy Analysis Method. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1644-1656	2.5	13
67	Optimizing the NoC Slack Through Voltage and Frequency Scaling in Hard Real-Time Embedded Systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1632-1643	2.5	6
66	Using multi-level cell STT-RAM for fast and energy-efficient local checkpointing **2014**,		14
65	Through Silicon Via Aware Design Planning for Thermally Efficient 3-D Integrated Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 1335-1346	2.5	21
64	Lazy Precharge: An overhead-free method to reduce precharge overhead for memory parallelism improvement of DRAM system **2013**,		1
63	Design of cross-point metal-oxide ReRAM emphasizing reliability and cost **2013**,		19
62	TS-Router: On maximizing the Quality-of-Allocation in the On-Chip Network **2013**,		5
61	NVSim: A Circuit-Level Performance, Energy, and Area Model for Emerging Nonvolatile Memory. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 994-1007	2.5	534
60	NVMain: An Architectural-Level Main Memory Simulator for Emerging Non-volatile Memories **2012**,		94
59	Low power memristor-based ReRAM design with Error Correcting Code **2012**,		35
58	ESL Design Methodology. *Journal of Electrical and Computer Engineering*, **2012**, 2012, 1-2	1.9	
57	Bandwidth-aware reconfigurable cache design with hybrid memory technologies **2011**,		9
56	Design implications of memristor-based RRAM cross-point structures **2011**,		19
55	Device-architecture co-optimization of STT-RAM based memory for low power embedded systems **2011**,		18
54	Energy-efficient multi-level cell phase-change memory system with data encoding **2011**,		45

53	Leakage Power and Circuit Aging Cooptimization by Gate Replacement Techniques. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 615-628	2.6	37
52	Variation-Aware Task and Communication Mapping for MPSoC Architecture. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 295-307	2.5	21
51	Enabling quality-of-service in nanophotonic network-on-chip **2011**,		4
50	Impact of Circuit Degradation on FPGA Design Security **2011**,		1
49	AdaMS: Adaptive MLC/SLC phase-change memory design for file storage **2011**,		43
48	An energy-efficient 3D CMP design with fine-grained voltage scaling **2011**,		1
47	Leveraging on-chip DRAM stacking in an embedded 3D multi-core DSP system **2011**,		3
46	A 3D SoC design for H.264 application with on-chip DRAM stacking **2010**,		14
45	Energy- and endurance-aware design of phase change memory caches **2010**,		2
44	Simple but Effective Heterogeneous Main Memory with On-Chip Memory Controller Support **2010**,		95
43	A customized design of DRAM controller for on-chip 3D DRAM stacking **2010**,		4
42	Three-dimensional integrated circuits (3D IC) Floorplan and Power/Ground Network Co-synthesis **2010**,		31
41	Evaluation of using inductive/capacitive-coupling vertical interconnects in 3D network-on-chip **2010** ,		13
40	Modeling TSV open defects in 3D-stacked DRAM **2010**,		20
39	LOFT: A High Performance Network-on-Chip Providing Quality-of-Service Support **2010**,		17
38	Variable-Latency Adder (VL-Adder) Designs for Low Power and NBTI Tolerance. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1621-1624	2.6	20
37	Fabrication Cost Analysis and Cost-Aware Design Space Exploration for 3-D ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 1959-1972	2.5	39
36	Processor Architecture Design Using 3D Integration Technology **2010**,		42

35	Architectural benefits and design challenges for three-dimensional integrated circuits **2010**,		3
34	3D memory stacking for fast checkpointing/restore applications **2010**,		5
33	Cost-effective integration of three-dimensional (3D) ICs emphasizing testing cost analysis **2010**,		36
32	Total Power Optimization for Combinational Logic Using Genetic Algorithms. *Journal of Signal Processing Systems*, **2010**, 58, 145-160	1.4	2
31	A criticality-driven microarchitectural three dimensional (3D) floorplanner **2009**,		3
30	Investigation and comparison of thermal distribution in synchronous and asynchronous 3D ICs **2009** ,		1
29	New-Age: A Negative Bias Temperature Instability-Estimation Framework for Microarchitectural Components. *International Journal of Parallel Programming*, **2009**, 37, 417-431	1.5	10
28	Test-wrapper optimization for embedded cores in TSV-based three-dimensional SOCs **2009**,		32
27	3D optical networks-on-chip (NoC) for multiprocessor systems-on-chip (MPSoC) **2009**,		17
26	Power and performance of read-write aware Hybrid Caches with non-volatile memories **2009**,		3
25	System-level cost analysis and design exploration for three-dimensional integrated circuits (3D ICs) **2009**,		72
24	NBTI-aware statistical circuit delay assessment **2009**,		9
23	Process-Variation-Aware Adaptive Cache Architecture and Management. *IEEE Transactions on Computers*, **2009**, 58, 865-877	2.5	19
22	Statistical High-Level Synthesis under Process Variability. *IEEE Design and Test of Computers*, **2009**, 26, 78-87		10
21	3D GPU architecture using cache stacking: Performance, cost, power and thermal analysis **2009**,		18
20	Thermal-aware reliability analysis for Platform FPGAs **2008**,		16
19	Case Study of Reliability-Aware and Low-Power Design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2008**, 16, 861-873	2.6	7
18	MIRA: A Multi-layered On-Chip Interconnect Router Architecture **2008**,		60

17	Two-dimensional crosstalk avoidance codes **2008**,		1
16	Design Space Exploration for 3-D Cache. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2008**, 16, 444-455	2.6	43
15	Thermal-aware Design Considerations for Application-Specific Instruction Set Processor **2008**,		2
14	Test-Access Solutions for Three-Dimensional SOCs **2008**,		1
13	Toward Increasing FPGA Lifetime. *IEEE Transactions on Dependable and Secure Computing*, **2008**, 5, 115-127	3.9	57
12	Test-access mechanism optimization for core-based three-dimensional SOCs **2008**,		55
11	Scan chain design for three-dimensional integrated circuits (3D ICs) **2007**,		38
10	Code Decompression Unit Design for VLIW Embedded Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2007**, 15, 975-980	2.6	3
9	Code compression for embedded VLIW processors using variable-to-fixed coding. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2006**, 14, 525-536	2.6	15
8	Crosstalk-Aware Energy Efficient Encoding for Instruction Bus through Code Compression **2006**,		3
7	A hybrid SoC interconnect with dynamic TDMA-based transaction-less buses and on-chip networks **2006**,		38
6	Guaranteeing Performance Yield in High-Level Synthesis. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2006**,		10
5	Modeling the Impact of Process Variation on Critical Charge Distribution **2006**,		17
4	Temperature-Aware Task Allocation and Scheduling for Embedded Multiprocessor Systems-on-Chip (MPSoC) Design. *Journal of Signal Processing Systems*, **2006**, 45, 177-189		68
3	Impact of process variation on soft error vulnerability for nanometer VLSI circuits		4
2	Three-dimensional cache design exploration using 3DCacti		34
1	Evaluation of thermal-aware design techniques for microprocessors		2