Yuan Xie

List of Publications by Year in descending order

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160	6,976	236833	118793
papers	citations	25 h-index	62 g-index

161	161	161	3856
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	PRIME. Computer Architecture News, 2016, 44, 27-39.	2.5	823
2	NVSim: A Circuit-Level Performance, Energy, and Area Model for Emerging Nonvolatile Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 994-1007.	1.9	778
3	Towards artificial general intelligence with hybrid Tianjic chip architecture. Nature, 2019, 572, 106-111.	13.7	517
4	Pinatubo. , 2016, , .		314
5	PRIME: A Novel Processing-in-Memory Architecture for Neural Network Computation in ReRAM-Based Main Memory. , 2016, , .		238
6	DRISA. , 2017, , .		214
7	NVMain 2.0: A User-Friendly Memory Simulator to Model (Non-)Volatile Memory Systems. IEEE Computer Architecture Letters, 2015, 14, 140-143.	1.0	172
8	HyGCN: A GCN Accelerator with Hybrid Architecture. , 2020, , .		160
9	NVMain: An Architectural-Level Main Memory Simulator for Emerging Non-volatile Memories. , 2012, , .		144
10	Power-efficient neural network with artificial dendrites. Nature Nanotechnology, 2020, 15, 776-782.	15.6	141
11	Rethinking the performance comparison between SNNS and ANNS. Neural Networks, 2020, 121, 294-307.	3.3	131
12	Simple but Effective Heterogeneous Main Memory with On-Chip Memory Controller Support. , 2010, , .		108
13	System-level cost analysis and design exploration for three-dimensional integrated circuits (3D ICs). , 2009, , .		101
14	Stuck-at Fault Tolerance in RRAM Computing Systems. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 102-115.	2.7	88
15	Temperature-Aware Task Allocation and Scheduling for Embedded Multiprocessor Systems-on-Chip (MPSoC) Design. Journal of Signal Processing Systems, 2006, 45, 177-189.	1.0	84
16	MIRA: A Multi-layered On-Chip Interconnect Router Architecture. , 2008, , .		76
17	GraphH: A Processing-in-Memory Architecture for Large-Scale Graph Processing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 640-653.	1.9	75
18	Toward Increasing FPGA Lifetime. IEEE Transactions on Dependable and Secure Computing, 2008, 5, 115-127.	3.7	73

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19	Cambricon: An Instruction Set Architecture for Neural Networks. , 2016, , .		73
20	A hybrid SoC interconnect with dynamic TDMA-based transaction-less buses and on-chip networks. , 2006, , .		71
21	A Study on Practically Unlimited Endurance of STT-MRAM. IEEE Transactions on Electron Devices, 2017, 64, 3639-3646.	1.6	67
22	Design Space Exploration for 3-D Cache. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 444-455.	2.1	66
23	Test-access mechanism optimization for core-based three-dimensional SOCs. , 2008, , .		66
24	Training high-performance and large-scale deep neural networks with full 8-bit integers. Neural Networks, 2020, 125, 70-82.	3.3	64
25	Fabrication Cost Analysis and Cost-Aware Design Space Exploration for 3-D ICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1959-1972.	1.9	62
26	Comparing SNNs and RNNs on neuromorphic vision datasets: Similarities and differences. Neural Networks, 2020, 132, 108-120.	3.3	62
27	Processor Architecture Design Using 3D Integration Technology. , 2010, , .		58
28	Design implications of memristor-based RRAM cross-point structures. , 2011, , .		56
29	Cost-effective design of scalable high-performance systems using active and passive interposers. , 2017, , .		56
30	Energy-efficient multi-level cell phase-change memory system with data encoding. , 2011, , .		55
31	NEUTRAMS: Neural network transformation and co-design under neuromorphic hardware constraints. , 2016, , .		55
32	AdaMS: Adaptive MLC/SLC phase-change memory design for file storage. , 2011, , .		54
33	Alleviating Irregularity in Graph Analytics Acceleration. , 2019, , .		53
34	Three-dimensional cache design exploration using 3DCacti. , 0, , .		51
35	Leakage Power and Circuit Aging Cooptimization by Gate Replacement Techniques. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 615-628.	2.1	49
36	Cost-effective integration of three-dimensional (3D) ICs emphasizing testing cost analysis. , 2010, , .		47

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37	Low power memristor-based ReRAM design with Error Correcting Code. , 2012, , .		47
38	Scan chain design for three-dimensional integrated circuits (3D ICs). , 2007, , .		46
39	TIME: A Training-in-Memory Architecture for RRAM-Based Deep Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 834-847.	1.9	44
40	MNSIM: Simulation Platform for Memristor-based Neuromorphic Computing System. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, , 1-1.	1.9	42
41	Test-wrapper optimization for embedded cores in TSV-based three-dimensional SOCs. , 2009, , .		41
42	Three-dimensional integrated circuits (3D IC) Floorplan and Power/Ground Network Co-synthesis. , 2010, , .		41
43	PXNOR-BNN: In/With Spin-Orbit Torque MRAM Preset-XNOR Operation-Based Binary Neural Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2668-2679.	2.1	41
44	Evolver: A Deep Learning Processor With On-Device Quantizationâ€“Voltageâ€“Frequency Tuning. IEEE Journal of Solid-State Circuits, 2021, 56, 658-673.	3.5	38
45	Design of cross-point metal-oxide ReRAM emphasizing reliability and cost. , 2013, , .		35
46	Characterizing and Understanding GCNs on GPU. IEEE Computer Architecture Letters, 2020, 19, 22-25.	1.0	35
47	Bridge the Gap between Neural Networks and Neuromorphic Hardware with a Neural Network Compiler. , 2018, , .		34
48	iPIM: Programmable In-Memory Image Processing Accelerator Using Near-Bank Architecture. , 2020, , .		34
49	LOFT: A High Performance Network-on-Chip Providing Quality-of-Service Support. , 2010, , .		31
50	Variable-Latency Adder (VL-Adder) Designs for Low Power and NBTI Tolerance. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1621-1624.	2.1	30
51	Architecture design with STT-RAM: Opportunities and challenges. , 2016, , .		28
52	Code compression for embedded VLIW processors using variable-to-fixed coding. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 525-536.	2.1	27
53	3D optical networks-on-chip (NoC) for multiprocessor systems-on-chip (MPSoC). , 2009, , .		27
54	3D GPU architecture using cache stacking: Performance, cost, power and thermal analysis. , 2009, , .		27

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55	Variation-Aware Task and Communication Mapping for MPSoC Architecture. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 295-307.	1.9	27
56	Through Silicon Via Aware Design Planning for Thermally Efficient 3-D Integrated Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1335-1346.	1.9	27
57	MNSIM: Simulation Platform for Memristor-based Neuromorphic Computing System. , 2016, , .		27
58	Impact of Write Pulse and Process Variation on 22Ânm FinFET-Based STT-RAM Design: A Device-Architecture Co-Optimization Approach. IEEE Transactions on Multi-Scale Computing Systems, 2015, 1, 195-206.	2.5	26
59	Mellow Writes: Extending Lifetime in Resistive Memories through Selective Slow Write Backs. , 2016, , .		26
60	Hybrid Drowsy SRAM and STT-RAM Buffer Designs for Dark-Silicon-Aware NoC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3041-3054.	2.1	25
61	Memory Trojan Attack on Neural Network Accelerators. , 2019, , .		24
62	Modeling TSV open defects in 3D-stacked DRAM. , 2010, , .		22
63	Modeling the Impact of Process Variation on Critical Charge Distribution. , 2006, , .		21
64	Rubik: A Hierarchical Architecture for Efficient Graph Neural Network Training. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 936-949.	1.9	21
65	Process-Variation-Aware Adaptive Cache Architecture and Management. IEEE Transactions on Computers, 2009, 58, 865-877.	2.4	20
66	Device-architecture co-optimization of STT-RAM based memory for low power embedded systems. , 2011, , .		20
67	Building energy-efficient multi-level cell STT-MRAM based cache through dynamic data-resistance encoding. , 2014, , .		20
68	Thermal-aware reliability analysis for Platform FPGAs. , 2008, , .		19
69	Spendthrift: Machine learning based resource and frequency scaling for ambient energy harvesting nonvolatile processors. , 2017, , .		18
70	Dynamic Power and Energy Management for Energy Harvesting Nonvolatile Processor Systems. Transactions on Embedded Computing Systems, 2017, 16, 1-23.	2.1	18
71	An Adaptive 3T-3MTJ Memory Cell Design for STT-MRAM-Based LLCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 484-495.	2.1	18
72	Memory that never forgets: emerging nonvolatile memory and the implication for architecture design. National Science Review, 2018, 5, 577-592.	4.6	18

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73	A 3D SoC design for H.264 application with on-chip DRAM stacking. , 2010, , .		17
74	Using multi-level cell STT-RAM for fast and energy-efficient local checkpointing. , 2014, , .		16
75	Dynamic machine learning based matching of nonvolatile processor microarchitecture to harvested energy profile. , 2015, , .		16
76	Practical Attacks on Deep Neural Networks by Memory Trojaning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1230-1243.	1.9	16
77	Evaluation of using inductive/capacitive-coupling vertical interconnects in 3D network-on-chip. , 2010, , .		15
78	SemiMap: A Semi-Folded Convolution Mapping for Speed-Overhead Balance on Crossbars. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 117-130.	1.9	15
79	Guaranteeing Performance Yield in High-Level Synthesis. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	14
80	PS3-RAM: A Fast Portable and Scalable Statistical STT-RAM Reliability/Energy Analysis Method. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1644-1656.	1.9	14
81	Building energy-efficient multi-level cell STT-RAM caches with data compression. , 2017, , .		14
82	DIMMining. , 2022, , .		14
83	Impact of Process Variation on Soft Error Vulnerability for Nanometer VLSI Circuits. , 0, , .		13
84	Optimizing the NoC Slack Through Voltage and Frequency Scaling in Hard Real-Time Embedded Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1632-1643.	1.9	13
85	Securing Emerging Nonvolatile Main Memory With Fast and Energy-Efficient AES In-Memory Implementation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2443-2455.	2.1	13
86	DASM: Data-Streaming-Based Computing in Nonvolatile Memory Architecture for Embedded System. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2046-2059.	2.1	13
87	Scalable memory fabric for silicon interposer-based multi-core systems. , 2016, , .		12
88	Thermomechanical Stress-Aware Management for 3-D IC Designs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2678-2682.	2.1	12
89	PRESCOTT: Preset-based cross-point architecture for spin-orbit-torque magnetic random access memory. , 2017, , .		12
90	New-Age: A Negative Bias Temperature Instability-Estimation Framework for Microarchitectural Components. International Journal of Parallel Programming, 2009, 37, 417-431.	1.1	11

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91	NBTI-aware statistical circuit delay assessment. , 2009, , .		11
92	TS-Router: On maximizing the Quality-of-Allocation in the On-Chip Network. , 2013, , .		11
93	Cost and Thermal Analysis of High-Performance 2.5D and 3D Integrated Circuit Design Space. , 2016, , .		11
94	AIM: Fast and energy-efficient AES in-memory implementation for emerging non-volatile main memory. , 2018, , .		11
95	CORN: In-Buffer Computing for Binary Neural Network. , 2019, , .		11
96	IronMan-Pro: Multiobjective Design Space Exploration in HLS via Reinforcement Learning and Graph Neural Network-Based Modeling. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 900-913.	1.9	11
97	Statistical High-Level Synthesis under Process Variability. IEEE Design and Test of Computers, 2009, 26, 78-87.	1.4	10
98	Case Study of Reliability-Aware and Low-Power Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 861-873.	2.1	9
99	A customized design of DRAM controller for on-chip 3D DRAM stacking. , 2010, , .		9
100	Bandwidth-aware reconfigurable cache design with hybrid memory technologies. , 2011, , .		9
101	An energy-efficient 3D CMP design with fine-grained voltage scaling. , 2011, , .		9
102	Fast Object Tracking on a Many-Core Neural Network Chip. Frontiers in Neuroscience, 2018, 12, 841.	1.4	9
103	Rescuing RRAM-Based Computing From Static and Dynamic Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2049-2062.	1.9	8
104	H2Learn: High-Efficiency Learning Accelerator for High-Accuracy Spiking Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 4782-4796.	1.9	8
105	An Instruction Set Architecture for Machine Learning. ACM Transactions on Computer Systems, 2019, 36, 1-35.	0.6	7
106	DLUX: A LUT-Based Near-Bank Accelerator for Data Center Deep Learning Training Workloads. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1586-1599.	1.9	7
107	Evaluation of Thermal-Aware Design Techniques for Microprocessors. , 0, , .		6
108	3D memory stacking for fast checkpointing/restore applications. , 2010, , .		6

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109	Efficient region-aware P/G TSV planning for 3D ICs. , 2014, , .		6
110	Adapting <inline-formula> <tex-math notation="LaTeX">$ext{B}^{+}$ </tex-math> </inline-formula>-Tree for Emerging Nonvolatile Memory-Based Main Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1461-1474.	1.9	6
111	NNBench-X: Benchmarking and Understanding Neural Network Workloads for Accelerator Designs. IEEE Computer Architecture Letters, 2019, 18, 38-42.	1.0	6
112	Total Power Optimization for Combinational Logic Using Genetic Algorithms. Journal of Signal Processing Systems, 2010, 58, 145-160.	1.4	5
113	Enabling quality-of-service in nanophotonic network-on-chip. , 2011, , .		5
114	Heterogeneous architecture design with emerging 3D and non-volatile memory technologies. , 2015, , .		5
115	Modeling framework for cross-point resistive memory design emphasizing reliability and variability issues. , 2015, , .		5
116	BACH: A Bandwidth-Aware Hybrid Cache Hierarchy Design with Nonvolatile Memories. Journal of Computer Science and Technology, 2016, 31, 20-35.	0.9	5
117	Fast Search of the Optimal Contraction Sequence in Tensor Networks. IEEE Journal on Selected Topics in Signal Processing, 2021, 15, 574-586.	7.3	5
118	SDP: Co-Designing Algorithm, Dataflow, and Architecture for In-SRAM Sparse NN Acceleration. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 109-121.	1.9	5
119	Crosstalk-Aware Energy Efficient Encoding for Instruction Bus through Code Compression. , 2006, , .		4
120	Code Decompression Unit Design for VLIW Embedded Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 975-980.	2.1	4
121	Two-dimensional crosstalk avoidance codes. , 2008, , .		4
122	Power and performance of read-write aware Hybrid Caches with non-volatile memories. , 2009, , .		4
123	Architectural benefits and design challenges for three-dimensional integrated circuits. , 2010, , .		4
124	Whitespace-Aware TSV Arrangement in 3-D Clock Tree Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1842-1853.	2.1	4
125	Memory-Bound Proof-of-Work Acceleration for Blockchain Applications. , 2019, , .		4
126	A criticality-driven microarchitectural three dimensional (3D) floorplanner. , 2009, , .		3

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127	Energy- and endurance-aware design of phase change memory caches. , 2010, , .		3
128	Leveraging on-chip DRAM stacking in an embedded 3D multi-core DSP system. , 2011, , .		3
129	Exploring memory controller configurations for many-core systems with 3D stacked DRAMs. , 2015, , .		3
130	Nonvolatile memory allocation and hierarchy optimization for high-level synthesis. , 2015, , .		3
131	Towards a polynomial algorithm for optimal contraction sequence of tensor networks from trees. Physical Review E, 2019, 100, 043309.	0.8	3
132	Hardware Acceleration for GCNs via Bidirectional Fusion. IEEE Computer Architecture Letters, 2021, 20, 66-4.	1.0	3
133	STPAcc: Structural TI-Based Pruning for Accelerating Distance-Related Algorithms on CPU-FPGA Platforms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1358-1370.	1.9	3
134	An Instruction-Level Analytical Power Model for DeSigning the Low Power Systems on a Chip. , 0, , .		2
135	Thermal-aware Design Considerations for Application-Specific Instruction Set Processor. , 2008, , .		2
136	Investigation and comparison of thermal distribution in synchronous and asynchronous 3D ICs. , 2009, , .		2
137	Cost-Aware Lifetime Yield Analysis of Heterogeneous 3D On-chip Cache. , 2009, , .		2
138	Impact of Circuit Degradation on FPGA Design Security. , 2011, , .		2
139	Lazy Precharge: An overhead-free method to reduce precharge overhead for memory parallelism improvement of DRAM system. , 2013, , .		2
140	A Real-Time and Energy-Efficient Implementation of Difference-of-Gaussian with Flexible Thin-Film Transistors. , 2016, , .		2
141	Packet Pump: Overcoming Network Bottleneck in On-Chip Interconnects for GPGPUs*. , 2018, , .		2
142	A Case for 3D Integrated System Design for Neuromorphic Computing and AI Applications. International Journal of Semantic Computing, 2020, 14, 457-475.	0.4	2
143	Practical Near-Data-Processing Architecture for Large-Scale Distributed Graph Neural Network. IEEE Access, 2022, 10, 46796-46807.	2.6	2
144	Adaptive Power Management in Software Radios Using Resolution Adaptive Analog to Digital Converters. , 0, , .		1

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145	Test-Access Solutions for Three-Dimensional SOCs. , 2008, , .		1
146	Tolerating process variations in high-level synthesis using transparent latches. , 2009, , .		1
147	Designing vertical bandwidth reconfigurable 3D NoCs for many core systems. , 2014, , .		1
148	Taming Unstructured Sparsity on GPUs via Latency-Aware Optimization. , 2020, , .		1
149	PLSAV: Parallel loop searching and verifying for loop closure detection. IET Intelligent Transport Systems, 2021, 15, 683-698.	1.7	1
150	Brain-Inspired Computing: Adventure from Beyond CMOS Technologies to Beyond von Neumann Architectures ICCAD Special Session Paper. , 2021, , .		1
151	Leakage Optimized DECAP Design for FPGAs. , 2006, , .		0
152	An Isolation-Based Circuit Design for Soft Error Suppression. , 2007, , .		0
153	FPGA routing architecture analysis under variations. , 2007, , .		0
154	Power and area reduction using carbon nanotube bundle interconnect in global clock tree distribution network. , 2009, , .		0
155	Modeling and design exploration of FBDRAM as on-chip memory. , 2012, , .		0
156	ESL Design Methodology. Journal of Electrical and Computer Engineering, 2012, 2012, 1-2.	0.6	0
157	A cost benefit analysis: The impact of defect clustering on the necessity of pre-bond tests. , 2014, , .		0
158	Using Multiple-Input NEMS for Parallel A/D Conversion and Image Processing. , 2015, , .		0
159	Utilizing 3D ICs in architectures for neural networks. , 2016, , .		0
160	POSTER: Bridge the Gap Between Neural Networks and Neuromorphic Hardware. , 2017, , .		0