Peng Cao

List of Publications by Year
in descending order

42 papers	180 citations	1478505 6 h-index	1281871 11 g-index
42 all docs	42 docs citations	42 times ranked	134 citing authors

#	Article	IF	Citations
1	Topology-Aided Multicorner Timing Predictor for Wide Voltage Design. IEEE Design and Test, 2023, 40, 62-69.	1.2	3
2	A Graph Neural Network Method for Fast ECO Leakage Power Optimization. , 2022, , .		3
3	Pre-Routing Path Delay Estimation Based on Transformer and Residual Framework. , 2022, , .		8
4	Semi-Analytical Path Delay Variation Model With Adjacent Gates Decorrelation for Subthreshold Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 931-944.	2.7	3
5	A Timing Prediction Framework for Wide Voltage Design with Data Augmentation Strategy. , 2021, , .		5
6	An Adaptive Delay Model for Timing Yield Estimation under Wide-Voltage Range. , 2021, , .		0
7	Analytical Delay Model in Near-Threshold Domain Considering Transition Time. , 2021, , .		0
8	Novel Prediction Framework for Path Delay Variation Based on Learning Method. Electronics (Switzerland), 2020, 9, 157.	3.1	2
9	An Accurate and Efficient Timing Prediction Framework for Wide Supply Voltage Design Based on Learning Method. Electronics (Switzerland), 2020, 9, 580.	3.1	3
10	Analytical Gate Delay Variation Model with Temperature Effects in Near-Threshold Region Based on Log-Skew-Normal Distribution. Electronics (Switzerland), 2019, 8, 501.	3.1	1
11	A Statistical Timing Model for CMOS Inverter in Near-threshold Region Considering Input Transition Time. , 2019, , .		2
12	A Statistical Timing Model for Low Voltage Design Considering Process Variation. , 2019, , .		1
13	An Analytical Gate Delay Model in Near/Subthreshold Domain Considering Process Variation. IEEE Access, 2019, 7, 171515-171524.	4.2	11
14	Path Delay Variation Prediction Model with Machine Learning. , 2018, , .		0
15	Context Management Scheme Optimization of Coarse-Grained Reconfigurable Architecture for Multimedia Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2321-2331.	3.1	4
16	Efficient AES cipher on coarse-grained reconfigurable architecture. IEICE Electronics Express, 2017, 14, 20170449-20170449.	0.8	1
17	Coarse-grained reconfigurable architecture with hierarchical context cache structure and management approach. IEICE Electronics Express, 2017, 14, 20170090-20170090.	0.8	2
18	Timing monitoring paths selection for wide voltage IC. IEICE Electronics Express, 2016, 13, 20160095-20160095.	0.8	6

#	Article	IF	Citations
19	Image Arbitrary-Ratio Down- and Up-Sampling Scheme Exploiting DCT Low Frequency Components and Sparsity in High Frequency Components. IEICE Transactions on Information and Systems, 2016, E99.D, 475-487.	0.7	6
20	An Energy-Efficient Coarse-Grained Reconfigurable Processing Unit for Multiple-Standard Video Decoding. IEEE Transactions on Multimedia, 2015, 17, 1706-1720.	7.2	29
21	A Configuration Compression Approach for Coarse-Grain Reconfigurable Architecture for Radar Signal Processing. , 2014, , .		6
22	Implementation of multi-standard video decoder on a heterogeneous coarse-grained reconfigurable processor. Science China Information Sciences, 2014, 57, 1-14.	4.3	1
23	A parallel arithmetic array for accelerating compute-intensive applications. IEICE Electronics Express, 2014, 11, 20130981-20130981.	0.8	0
24	Reduced-error constant correction truncated multiplier. IEICE Electronics Express, 2014, 11, 20140481-20140481.	0.8	0
25	VLSI design of a reconfigurable S-box based on memory sharing method. IEICE Electronics Express, 2014, 11, 20130872-20130872.	0.8	5
26	A Robust and Efficient Minutia-Based Fingerprint Matching Algorithm. , 2013, , .		0
27	Hierarchical representation of on-chip context to reduce reconfiguration time and implementation area for coarse-grained reconfigurable architecture. Science China Information Sciences, 2013, 56, 1-20.	4.3	2
28	Exploration of Full HD Media Decoding on a Software Defined Radio Baseband Processor. IEEE Transactions on Signal Processing, 2013, 61, 4438-4449.	5.3	3
29	An energy-efficient coarse-grained dynamically reconfigurable fabric for multiple-standard video decoding applications. , 2013, , .		24
30	Evaluation of Correlation Power Analysis Resistance and Its Application on Asymmetric Mask Protected Data Encryption Standard Hardware. IEEE Transactions on Instrumentation and Measurement, 2013, 62, 2716-2724.	4.7	12
31	An improved timing monitor for deep dynamic voltage scaling system. IEICE Electronics Express, 2013, 10, 20130089-20130089.	0.8	5
32	Hardware Software Co-design of H.264 Baseline Encoder on Coarse-Grained Dynamically Reconfigurable Computing System-on-Chip. IEICE Transactions on Information and Systems, 2013, E96.D, 601-615.	0.7	4
33	Parallelism Analysis of H.264 Decoder and Realization on a Coarse-Grained Reconfigurable SoC. IEICE Transactions on Information and Systems, 2013, E96.D, 1654-1666.	0.7	0
34	The Organization of On-Chip Data Memory in One Coarse-Grained Reconfigurable Architecture. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2013, E96.A, 2218-2229.	0.3	0
35	Reconfiguration Process Optimization of Dynamically Coarse Grain Reconfigurable Architecture for Multimedia Applications. IEICE Transactions on Information and Systems, 2012, E95.D, 1858-1871.	0.7	8
36	Date Flow Optimization of Dynamically Coarse Grain Reconfigurable Architecture for Multimedia Applications. IEICE Transactions on Information and Systems, 2012, E95-D, 374-382.	0.7	15

#	Article	IF	Citations
37	Implementation of H.264/AVC encoder on coarse-grained dynamically reconfigurable computing system. , 2012, , .		0
38	Hybrid-Priority Configuration Cache Supervision Method for Coarse Grained Reconfigurable Architecture. , 2012, , .		1
39	Exploration of Full HD Media Decoding on SDR Baseband Processor. , 2012, , .		0
40	Configuration Cache Management for Coarse-Grained Reconfigurable Architecture with Multi-Array. , 2012, , .		2
41	A New Approach to Implement Discrete Wavelet Transform on Coarse-Grained Reconfigurable Architecture. , 2012, , .		2
42	Memory-Efficient and High-Performance Two-Dimensional Discrete Wavelet Transform Architecture Based on Decomposed Lifting Algorithm. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 2000-2008.	0.3	0