Taesik Na

List of Publications by Year
in descending order

15 papers	227 citations	1307594 7 h-index	1372567 10 g-index
15 all docs	15 docs citations	15 times ranked	272 citing authors

#	Article	IF	Citations
1	A Universal Modular Hybrid LDO With Fast Load Transient Response and Programmable PSRR in 14-nm CMOS Featuring Dynamic Clamp Strength Tuning. IEEE Journal of Solid-State Circuits, 2021, 56, 2402-2415.	5.4	9
2	Cross-Layer Noise Analysis in Smart Digital Pixel Sensors With Integrated Deep Neural Network. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 444-457.	3.6	2
3	WarningNet: A Deep Learning Platform for Early Warning of Task Failures under Input Perturbation for Reliable Autonomous Platforms. , 2020, , .		2
4	Effect of Process Variations in Digital Pixel Circuits on the Accuracy of DNN based Smart Sensor. , 2020, , .		3
5	CAMEL: An Adaptive Camera With Embedded Machine Learning-Based Sensor Parameter Control. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 498-508.	3.6	13
6	Mixture of Pre-processing Experts Model for Noise Robust Deep Learning on Resource Constrained Platforms. , 2019, , .		9
7	A Camera with Brain â€“ Embedding Machine Learning in 3D Sensors. , 2019, , .		4
8	Design and Analysis of a Neural Network Inference Engine Based on Adaptive Weight Compression. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 109-121.	2.7	12
9	3-D Stacked Image Sensor With Deep Neural Network Computation. IEEE Sensors Journal, 2018, 18, 4187-4199.	4.7	30
10	An Energy-Quality Scalable Wireless Image Sensor Node for Object-Based Video Surveillance. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 591-602.	3.6	7
11	ReRAM-Based Processing-in-Memory Architecture for Recurrent Neural Network Acceleration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2781-2794.	3.1	81
12	DeepTrain: A Programmable Embedded Platform for Training Deep Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2360-2370.	2.7	21
13	On-chip training of recurrent neural networks with limited numerical precision. , 2017, , .		22
14	Clock Data Compensation Aware Digital Circuits Design for Voltage Margin Reduction. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2401-2413.	5.4	1
15	A Single-Chip Image Sensor Node With Energy Harvesting From a CMOS Pixel Array. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2295-2307.	5.4	11