Mohammad Yavari

List of Publications by Year in Descending Order

97 papers	531 citations	11 h-index	17 g-index
123 ext. papers	725 ext. citations	1.8 avg, IF	4.63 L-index

#	Paper	IF	Citations
97	A push-pull FVF based LDO voltage regulator with slew rate enhancement at the gate of power transistor. *Microelectronics Journal*, **2022**, 122, 105389	1.8	1
96	A front-end amplifier with tunable bandwidth and high value pseudo resistor for neural recording implants. *Microelectronics Journal*, **2021**, 119, 105333	1.8	1
95	A Low-Power High-Gain Low-Dropout Regulator for Implantable Biomedical Applications. *Circuits, Systems, and Signal Processing*, **2021**, 40, 1041-1060	2.2	2
94	A Linear Wideband CMOS Balun-LNA with Balanced Loads. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 1-1	3.5	0
93	A three-stage NMC operational amplifier with enhanced slew rate for switched-capacitor circuits. *Analog Integrated Circuits and Signal Processing*, **2021**, 106, 697-706	1.2	1
92	A +7.6 dBm IIP3 2.4-GHz Double-Balanced Mixer With 10.5 dB NF in 65-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 3214-3218	3.5	1
91	A 56-to-66 GHz CMOS Low-Power Phased-Array Receiver Front-End With Hybrid Phase Shifting Scheme. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 4002-4014	3.9	3
90	Shifting the sampled input signal in successive approximation register analog-to-digital converters to reduce the digital-to-analog converter switching energy and area. *International Journal of Circuit Theory and Applications*, **2020**, 48, 1873-1886	2	0
89	A 55–64-GHz Low-Power Small-Area LNA in 65-nm CMOS With 3.8-dB Average NF and ~12.8-dB Power Gain. *IEEE Microwave and Wireless Components Letters*, **2019**, 29, 128-130	2.6	12
88	A 17-to-24 GHz Low-Power Variable-Gain Low-Noise Amplifier in 65-nm CMOS for Phased-Array Receivers. *Circuits, Systems, and Signal Processing*, **2019**, 38, 5448-5466	2.2	5
87	Digital Calibration of Elements Mismatch in Multirate Predictive SAR ADCs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 4571-4581	3.9	1
86	An adaptive continuous-time incremental ΔΣADC for neural recording implants. *International Journal of Circuit Theory and Applications*, **2019**, 47, 187-203	2	4
85	A Wideband High Linearity and Low-Noise CMOS Active Mixer Using the Derivative Superposition and Noise Cancellation Techniques. *Circuits, Systems, and Signal Processing*, **2019**, 38, 2910-2930	2.2	11
84	An Automatic Action Potential Detector for Neural Recording Implants. *Circuits, Systems, and Signal Processing*, **2019**, 38, 1923-1941	2.2	2
83	A power conversion chain with an internally-set voltage reference and reusing the power receiver coil for wireless bio-implants. *Microelectronics Journal*, **2018**, 74, 69-78	1.8	2
82	Digital Background Calibration With Histogram of Decision Points in Pipelined ADCs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 16-20	3.5	7
81	. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 41-45	3.5	20

80	An oscillatory noise-shaped quantizer for time-based continuous-time sigma-delta modulators. *International Journal of Circuit Theory and Applications*, **2018**, 46, 384-400	2	1
79	Statistics-Based Digital Background Calibration of Residue Amplifier Nonlinearity in Pipelined ADCs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 4097-4109	3.9	8
78	A Single Channel Split ADC Structure for Digital Background Calibration in Pipelined ADCs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 1563-1567	2.6	7
77	Digital Blind Background Calibration of Imperfections in Time-Interleaved ADCs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2017**, 64, 1504-1514	3.9	26
76	A power efficient buck-boost converter by reusing the coil inductor for wireless bio-implants. *International Journal of Circuit Theory and Applications*, **2017**, 45, 1673-1685	2	4
75	A wide-band CMOS active mixer with linearity improvement technique **2017**,		1
74	MASH modulators with a noise-shaped two-step ADC in the second stage. *The Integration VLSI Journal*, **2017**, 56, 77-85	1.4	1
73	A Simple Structure for MASH (Sigma Delta) Modulators with Highly Reduced In-Band Quantization Noise. *Circuits, Systems, and Signal Processing*, **2017**, 36, 2125-2153	2.2	4
72	High-performance time-based continuous-time sigma-delta modulators using single-opamp resonator and noise-shaped quantizer. *Microelectronics Journal*, **2016**, 56, 110-121	1.8	3
71	An NTF-enhanced incremental modulator using a SAR quantizer. *The Integration VLSI Journal*, **2016**, 55, 212-219	1.4	5
70	Using the GateBulk Interaction and a Fundamental Current Injection to Attenuate IM3 and IM2 Currents in RF Transconductors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 223-232	2.6	12
69	Digital Calibration of DAC Unit Elements Mismatch in Pipelined ADCs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2016**, 63, 34-45	3.9	6
68	An IIP3 enhancement technique for CMOS active mixers with a source-degenerated transconductance stage. *Microelectronics Journal*, **2016**, 50, 44-49	1.8	10
67	Digital Background Calibration of Residue Amplifier Non-idealities in Pipelined ADCs. *Circuits, Systems, and Signal Processing*, **2016**, 35, 3675-3699	2.2	3
66	Digital Calibration of Amplifier Finite DC Gain and Gain Bandwidth in MASH $SigmaDelta$ Modulators. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2016**, 63, 321-325	3.5	9
65	A wideband time-based continuous-time sigma-delta modulator with 2nd order noise-coupling based on passive elements. *International Journal of Circuit Theory and Applications*, **2016**, 44, 759-779	2	5
64	A UWB CMOS low-noise amplifier with noise reduction and linearity improvement techniques. *Microelectronics Journal*, **2015**, 46, 198-206	1.8	18
63	A simple structure for noise-shaping SAR ADC in 90 nm CMOS technology. *AEU - International Journal of Electronics and Communications*, **2015**, 69, 1085-1093	2.8	8

62	A three-stage class AB operational amplifier with enhanced slew rate for switched-capacitor circuits. *Analog Integrated Circuits and Signal Processing*, **2015**, 83, 111-118	1.2	6
61	System level design and optimization of single-loop CT sigma-delta modulators for high resolution wideband applications. *Microelectronics Journal*, **2015**, 46, 1073-1081	1.8	5
60	A pseudo-differential current-reuse structure for opamp-sharing pipelined analog-to-digital converters. *International Journal of Circuit Theory and Applications*, **2015**, 43, 917-928	2	3
59	A Predetermined LMS Digital Background Calibration Technique for Pipelined ADCs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2015**, 62, 841-845	3.5	13
58	A Calibration Technique for Pipelined ADCs Using Self-Measurement and Histogram-Based Test Methods. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2015**, 62, 826-830	3.5	4
57	An NTF-enhanced time-based continuous-time sigma-delta modulator. *Analog Integrated Circuits and Signal Processing*, **2015**, 85, 283-297	1.2	2
56	Second-order intermodulation cancelation and conversion-gain enhancement techniques for CMOS active mixers. *International Journal of Circuit Theory and Applications*, **2015**, 43, 1508-1522	2	5
55	MASH modulator with highly reduced in-band quantisation noise. *Electronics Letters*, **2014**, 50, 161-163	1.1	4
54	A zero-crossing based 10-bit 100 MS/s pipeline ADC with controlled current in 90 nm CMOS. *Analog Integrated Circuits and Signal Processing*, **2014**, 80, 141-151	1.2	2
53	A single-stage operational amplifier with enhanced transconductance and slew rate for switched-capacitor circuits. *Analog Integrated Circuits and Signal Processing*, **2014**, 79, 589-598	1.2	20
52	Energy-efficient high-accuracy switching method for SAR ADCs. *Electronics Letters*, **2014**, 50, 499-501	1.1	51
51	A pseudo-differential MDAC with a gain-boosting inverter for pipelined ADCs. *Analog Integrated Circuits and Signal Processing*, **2014**, 79, 255-266	1.2	5
50	Design of CMOS three-stage amplifiers for fast-settling switched-capacitor circuits. *Analog Integrated Circuits and Signal Processing*, **2014**, 80, 195-208	1.2	8
49	An LO architecture with novel wide locking range, quadrature output RILFDs and ILROs for cognitive radio applications. *Analog Integrated Circuits and Signal Processing*, **2014**, 80, 483-498	1.2	
48	Equalization-Based Digital Background Calibration Technique for Pipelined ADCs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 322-333	2.6	15
47	A low-power four-stage amplifier for driving large capacitive loads. *International Journal of Circuit Theory and Applications*, **2014**, 42, 978-988	2	8
46	A high IIP2 and IIP3 CMOS down-conversion active mixer **2014**,		1
45	A 10-BIT 0.5 V 100 kS/s SAR ADC WITH A NEW RAIL-TO-RAIL COMPARATOR FOR ENERGY LIMITED APPLICATIONS. *Journal of Circuits, Systems and Computers*, **2014**, 23, 1450026	0.9	4

44	A 2.6–3.7 GHz highly linear CMOS low noise amplifier for UWB applications **2014**,		1
43	A simple global resonation strategy for wideband discrete-time MASH Δ modulators **2014**,		1
42	Using interaction between two nonlinear systems to improve IIP3 in active mixers. *Electronics Letters*, **2014**, 50, 76-77	1.1	9
41	High-speed three-stage operational transconductance amplifiers for switched-capacitor circuits **2014**,		5
40	An error-feedback noise-shaping SAR ADC in 90 nm CMOS. *Analog Integrated Circuits and Signal Processing*, **2014**, 81, 805-814	1.2	3
39	A time-domain noise-coupling technique for continuous-time sigma-delta modulators. *Analog Integrated Circuits and Signal Processing*, **2014**, 78, 439-452	1.2	4
38	A 13 bit 10 MHz bandwidth MASH 3Δ modulator in 90 nm CMOS. *International Journal of Circuit Theory and Applications*, **2013**, 41, 1136-1153	2	9
37	An efficient threshold voltage generation for SAR ADCs. *Analog Integrated Circuits and Signal Processing*, **2013**, 75, 161-169	1.2	4
36	A noise-shaping SAR ADC for energy limited applications in 90 nm CMOS technology. *Analog Integrated Circuits and Signal Processing*, **2013**, 77, 257-269	1.2	7
35	A new linearization technique for CMOS low noise amplifiers with balun circuitry **2013**,		1
34	A /spl Sigma/ /spl Delta/-FIR-DAC for Multi-Bit /spl Sigma/ /spl Delta/ Modulators. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2013**, 60, 2321-2332	3.9	4
33	On the design and optimization of a switched-capacitor interface circuit for MEMS capacitive sensors **2012**,		1
32	A SAR ADC with an efficient threshold voltage generation **2012**,		1
31	A VERY LOW NOISE WIDEBAND CLASS-C CMOS LC VCO. *Journal of Circuits, Systems and Computers*, **2012**, 21, 1250033	0.9	1
30	A hybrid CT/DT double-sampled SMASH Δ modulator for broadband applications in 90 nm CMOS technology. *Analog Integrated Circuits and Signal Processing*, **2012**, 73, 101-114	1.2	1
29	AN EFFICIENT LOW-POWER SIGMA-DELTA MODULATOR FOR MULTI-STANDARD WIRELESS APPLICATIONS. *Journal of Circuits, Systems and Computers*, **2012**, 21, 1250028	0.9	2
28	A very wideband low noise amplifier for cognitive radios **2011**,		4
27	A 2.2GHz high-swing class-C VCO with wide tuning range **2011**,		1

26	A highly linear mixer with inherent balun using a new technique to remove common mode currents **2011**,		6
25	Minimum detectable capacitance in capacitive readout circuits **2011**,		1
24	A low power UWB very low noise amplifier using an improved noise reduction technique **2011**,		5
23	A new digital background correction algorithm with non-precision calibration signals for pipelined ADCs **2011**,		1
22	A linearization technique for active mixers in zero-IF receivers with inherent balun. *IEICE Electronics Express*, **2011**, 8, 2080-2086	0.5	1
21	A Design Procedure for CMOS Three-Stage NMC Amplifiers. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2011**, E94-A, 639-645	0.4	8
20	ACTIVE-FEEDBACK SINGLE MILLER CAPACITOR FREQUENCY COMPENSATION TECHNIQUES FOR THREE-STAGE AMPLIFIERS. *Journal of Circuits, Systems and Computers*, **2010**, 19, 1381-1398	0.9	7
19	A LOW-VOLTAGE LOW-POWER 10-BIT 200 MS/S PIPELINED ADC IN 90 NM CMOS. *Journal of Circuits, Systems and Computers*, **2010**, 19, 393-405	0.9	2
18	LOW-VOLTAGE DOUBLE-SAMPLED HYBRID CT/DT Σ∆MODULATOR FOR WIDEBAND APPLICATIONS. *Journal of Circuits, Systems and Computers*, **2010**, 19, 1743-1751	0.9	2
17	Single-stage class AB operational amplifier for SC circuits. *Electronics Letters*, **2010**, 46, 977	1.1	20
16	A novel digital calibration technique for pipelined ADCs. *IEICE Electronics Express*, **2010**, 7, 1741-1746	0.5	2
15	A new input matching technique for ultra wideband LNAs. *IEICE Electronics Express*, **2010**, 7, 1376-1381	0.5	5
14	Multirate double-sampling hybrid CT/DT sigma-delta modulators for wideband applications **2009**,		5
13	On the design of a less jitter sensitive NTF for NRZ multi-bit continuous-time Σ∆modulators **2009**,		1
12	A noise-canceling CMOS LNA design for the upper band of UWB DS-CDMA receivers **2009**,		8
11	A new class AB folded-cascode operational amplifier. *IEICE Electronics Express*, **2009**, 6, 395-402	0.5	6
10	A Linear wideband CMOS LNA for 3Ð5 GHZ UWB systems **2008**,		1
9	A novel topology in reversed nested miller compensation using dual-active capacitance **2008**,		5

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8	A linear current-reused LNA for 3.1-10.6GHz UWB receivers. *IEICE Electronics Express*, **2008**, 5, 908-914	0.5	4
7	A novel topology in RNMC amplifiers with single miller compensation capacitor **2008**,		5
6	Accurate and simple modeling of amplifier dc gain nonlinearity in switched-capacitor circuits **2007**,		5
5	Efficient double-sampled cascaded .SIGMA..DELTA. modulator topologies for low OSRs. *IEICE Electronics Express*, **2005**, 2, 404-410	0.5	
4	A novel fully-differential class AB folded-cascode OTA for switched-capacitor applications **2005**,		1
3	A novel fully-differential class AB folded-cascode OTA. *IEICE Electronics Express*, **2004**, 1, 358-362	0.5	1
2	Low-voltage low-power fast-settling CMOS operational transconductance amplifiers for switched-capacitor applications **2003**,		4
1	Very low-voltage, low-power and fast-settling OTA for switched-capacitor applications		5