Mohammad Yavari

List of Publications by Year
in descending order

123 papers	850 citations	687335 13 h-index	713444 21 g-index
123 all docs	123 docs citations	123 times ranked	518 citing authors

#	Article	IF	Citations
1	Energy‐efficient high‐accuracy switching method for SAR ADCs. Electronics Letters, 2014, 50, 499-501.	1.0	69
2	Digital Blind Background Calibration of Imperfections in Time-Interleaved ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1504-1514.	5.4	33
3	A single-stage operational amplifier with enhanced transconductance and slew rate for switched-capacitor circuits. Analog Integrated Circuits and Signal Processing, 2014, 79, 589-598.	1.4	32
4	Single-stage class AB operational amplifier for SC circuits. Electronics Letters, 2010, 46, 977.	1.0	27
5	An Energy-Efficient DAC Switching Method for SAR ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 41-45.	3.0	27
6	A UWB CMOS low-noise amplifier with noise reduction and linearity improvement techniques. Microelectronics Journal, 2015, 46, 198-206.	2.0	26
7	A 55–64-GHz Low-Power Small-Area LNA in 65-nm CMOS With 3.8-dB Average NF and ~12.8-dB Power Gain. IEEE Microwave and Wireless Components Letters, 2019, 29, 128-130.	3.2	26
8	Equalization-Based Digital Background Calibration Technique for Pipelined ADCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 322-333.	3.1	25
9	Using the Gate–Bulk Interaction and a Fundamental Current Injection to Attenuate IM3 and IM2 Currents in RF Transconductors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 223-232.	3.1	19
10	Digital Calibration of Amplifier Finite DC Gain and Gain Bandwidth in MASH Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 321-325.	3.0	17
11	A Predetermined LMS Digital Background Calibration Technique for Pipelined ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 841-845.	3.0	16
12	A Wideband High Linearity and Low-Noise CMOS Active Mixer Using the Derivative Superposition and Noise Cancellation Techniques. Circuits, Systems, and Signal Processing, 2019, 38, 2910-2930.	2.0	16
13	A noise-canceling CMOS LNA design for the upper band of UWB DS-CDMA receivers. , 2009, , .		14
14	Digital Background Calibration With Histogram of Decision Points in Pipelined ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 16-20.	3.0	14
15	A simple structure for noise-shaping SAR ADC in 90nm CMOS technology. AEU - International Journal of Electronics and Communications, 2015, 69, 1085-1093.	2.9	13
16	A noise-shaping SAR ADC for energy limited applications in 90Ânm CMOS technology. Analog Integrated Circuits and Signal Processing, 2013, 77, 257-269.	1.4	12
17	An IIP3 enhancement technique for CMOS active mixers with a source-degenerated transconductance stage. Microelectronics Journal, 2016, 50, 44-49.	2.0	12
18	A 56-to-66 GHz CMOS Low-Power Phased-Array Receiver Front-End With Hybrid Phase Shifting Scheme. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4002-4014.	5.4	12

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19	A 13 bit 10â€‰MHz bandwidth MASH 3â€"2 Î£â^† modulator in 90â€‰nm CMOS. International Journal of Circuit Theory and Applications, 2013, 41, 1136-1153.	2.0	11
20	Using interaction between two nonlinear systems to improve IIP3Âin active mixers. Electronics Letters, 2014, 50, 76-77.	1.0	11
21	A lowâ€power fourâ€stage amplifier for driving large capacitive loads. International Journal of Circuit Theory and Applications, 2014, 42, 978-988.	2.0	11
22	A power efficient buckâ€boost converter by reusing the coil inductor for wireless bioâ€implants. International Journal of Circuit Theory and Applications, 2017, 45, 1673-1685.	2.0	11
23	Statistics-Based Digital Background Calibration of Residue Amplifier Nonlinearity in Pipelined ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 4097-4109.	5.4	11
24	An adaptive continuousâ€time incremental Î£â^† ADC for neural recording implants. International Journal of Circuit Theory and Applications, 2019, 47, 187-203.	2.0	11
25	Very low-voltage, low-power and fast-settling OTA for switched-capacitor applications. , 0, , .		10
26	ACTIVE-FEEDBACK SINGLE MILLER CAPACITOR FREQUENCY COMPENSATION TECHNIQUES FOR THREE-STAGE AMPLIFIERS. Journal of Circuits, Systems and Computers, 2010, 19, 1381-1398.	1.5	10
27	Design of CMOS three-stage amplifiers for fast-settling switched-capacitor circuits. Analog Integrated Circuits and Signal Processing, 2014, 80, 195-208.	1.4	10
28	A 17-to-24ÂGHz Low-Power Variable-Gain Low-Noise Amplifier in 65-nm CMOS for Phased-Array Receivers. Circuits, Systems, and Signal Processing, 2019, 38, 5448-5466.	2.0	10
29	A Linear Wideband CMOS Balun-LNA With Balanced Loads. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 754-758.	3.0	10
30	A front-end amplifier with tunable bandwidth and high value pseudo resistor for neural recording implants. Microelectronics Journal, 2022, 119, 105333.	2.0	10
31	A new class AB folded-cascode operational amplifier. IEICE Electronics Express, 2009, 6, 395-402.	0.8	9
32	A low power UWB very low noise amplifier using an improved noise reduction technique. , 2011, , .		9
33	A three-stage class AB operational amplifier with enhanced slew rate for switched-capacitor circuits. Analog Integrated Circuits and Signal Processing, 2015, 83, 111-118.	1.4	9
34	A Low-Power High-Gain Low-Dropout Regulator for Implantable Biomedical Applications. Circuits, Systems, and Signal Processing, 2021, 40, 1041-1060.	2.0	9
35	A Design Procedure for CMOS Three-Stage NMC Amplifiers. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2011, E94-A, 639-645.	0.3	9
36	Low-voltage low-power fast-settling CMOS operational transconductance amplifiers for switched-capacitor applications. , 2003, , .		8

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37	A $Sigma Delta$-FIR-DAC for Multi-Bit $Sigma Delta$ Modulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2321-2332.	5.4	8
38	A 10-BIT 0.5 V 100 kS/s SAR ADC WITH A NEW RAIL-TO-RAIL COMPARATOR FOR ENERGY LIMITED APPLICATIONS. Journal of Circuits, Systems and Computers, 2014, 23, 1450026.	1.5	8
39	High-speed three-stage operational transconductance amplifiers for switched-capacitor circuits. , 2014, , .		8
40	Digital Calibration of DAC Unit Elements Mismatch in Pipelined ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 34-45.	5.4	8
41	A Single Channel Split ADC Structure for Digital Background Calibration in Pipelined ADCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1563-1567.	3.1	8
42	A +7.6 dBm IIP3 2.4-GHz Double-Balanced Mixer With 10.5 dB NF in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3214-3218.	3.0	8
43	A new input matching technique for ultra wideband LNAs. IEICE Electronics Express, 2010, 7, 1376-1381.	0.8	7
44	A highly linear mixer with inherent balun using a new technique to remove common mode currents. , 2011, , .		7
45	An error-feedback noise-shaping SAR ADC in 90Ânm CMOS. Analog Integrated Circuits and Signal Processing, 2014, 81, 805-814.	1.4	7
46	Secondâ€order intermodulation cancelation and conversionâ€gain enhancement techniques for CMOS active mixers. International Journal of Circuit Theory and Applications, 2015, 43, 1508-1522.	2.0	7
47	A push-pull FVF based LDO voltage regulator with slew rate enhancement at the gate of power transistor. Microelectronics Journal, 2022, 122, 105389.	2.0	7
48	A novel topology in reversed nested miller compensation using dual-active capacitance. , 2008, , .		6
49	Multirate double-sampling hybrid CT/DT sigma-delta modulators for wideband applications. , 2009, , .		6
50	A 2.2GHz high-swing class-C VCO with wide tuning range. , 2011, , .		6
51	A Calibration Technique for Pipelined ADCs Using Self-Measurement and Histogram-Based Test Methods. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 826-830.	3.0	6
52	System level design and optimization of single-loop CT sigma-delta modulators for high resolution wideband applications. Microelectronics Journal, 2015, 46, 1073-1081.	2.0	6
53	A wideband timeâ€based continuousâ€time sigmaâ€delta modulator with 2nd order noiseâ€coupling based on passive elements. International Journal of Circuit Theory and Applications, 2016, 44, 759-779.	2.0	6
54	An Automatic Action Potential Detector for Neural Recording Implants. Circuits, Systems, and Signal Processing, 2019, 38, 1923-1941.	2.0	6

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55	Accurate and simple modeling of amplifier dc gain nonlinearity in switched-capacitor circuits. , 2007, , .		5
56	A novel topology in RNMC amplifiers with single miller compensation capacitor. , 2008, , .		5
57	A linear current-reused LNA for 3.1-10.6GHz UWB receivers. IEICE Electronics Express, 2008, 5, 908-914.	0.8	5
58	A very wideband low noise amplifier for cognitive radios. , 2011, , .		5
59	MASH Î£Î" modulator with highly reduced in-band quantisation noise. Electronics Letters, 2014, 50, 161-163.	1.0	5
60	A pseudo-differential MDAC with a gain-boosting inverter for pipelined ADCs. Analog Integrated Circuits and Signal Processing, 2014, 79, 255-266.	1.4	5
61	High-performance time-based continuous-time sigma-delta modulators using single-opamp resonator and noise-shaped quantizer. Microelectronics Journal, 2016, 56, 110-121.	2.0	5
62	An NTF-enhanced incremental Î£Î" modulator using a SAR quantizer. The Integration VLSI Journal, 2016, 55, 212-219.	2.1	5
63	A Simple Structure for MASH $$Sigma Delta $$ Î£ Î" Modulators with Highly Reduced In-Band Quantization Noise. Circuits, Systems, and Signal Processing, 2017, 36, 2125-2153.	2.0	5
64	A power conversion chain with an internally-set voltage reference and reusing the power receiver coil for wireless bio-implants. Microelectronics Journal, 2018, 74, 69-78.	2.0	5
65	An efficient threshold voltage generation for SAR ADCs. Analog Integrated Circuits and Signal Processing, 2013, 75, 161-169.	1.4	4
66	A time-domain noise-coupling technique for continuous-time sigma-delta modulators. Analog Integrated Circuits and Signal Processing, 2014, 78, 439-452.	1.4	4
67	Digital Calibration of Elements Mismatch in Multirate Predictive SAR ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4571-4581.	5.4	4
68	Shifting the sampled input signal in successive approximation register analog-to-digital converters to reduce the digital-to-analog converter switching energy and area. International Journal of Circuit Theory and Applications, 2020, 48, 1873-1886.	2.0	4
69	A three-stage NMC operational amplifier with enhanced slew rate for switched-capacitor circuits. Analog Integrated Circuits and Signal Processing, 2021, 106, 697-706.	1.4	4
70	A novel fully-differential class AB folded-cascode OTA. IEICE Electronics Express, 2004, 1, 358-362.	0.8	3
71	A novel fully-differential class AB folded-cascode OTA for switched-capacitor applications. , 2005, , .		3
72	A Linear wideband CMOS LNA for 3–5 GHZ UWB systems. , 2008, , .		3

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73	A novel digital calibration technique for pipelined ADCs. IEICE Electronics Express, 2010, 7, 1741-1746.	0.8	3
74	A new digital background correction algorithm with non-precision calibration signals for pipelined ADCs. , 2011, , .		3
75	AN EFFICIENT LOW-POWER SIGMA-DELTA MODULATOR FOR MULTI-STANDARD WIRELESS APPLICATIONS. Journal of Circuits, Systems and Computers, 2012, 21, 1250028.	1.5	3
76	A 2.6&#x2013;13.7 GHz highly linear CMOS low noise amplifier for UWB applications. , 2014, , .		3
77	A pseudoâ€differential currentâ€reuse structure for opampâ€sharing pipelined analogâ€toâ€digital converters. International Journal of Circuit Theory and Applications, 2015, 43, 917-928.	2.0	3
78	Digital Background Calibration of Residue Amplifier Non-idealities in Pipelined ADCs. Circuits, Systems, and Signal Processing, 2016, 35, 3675-3699.	2.0	3
79	A LOW-VOLTAGE LOW-POWER 10-BIT 200 MS/S PIPELINED ADC IN 90 NM CMOS. Journal of Circuits, Systems and Computers, 2010, 19, 393-405.	1.5	2
80	LOW-VOLTAGE DOUBLE-SAMPLED HYBRID CT/DT Î£Î" MODULATOR FOR WIDEBAND APPLICATIONS. Journal of Circuits, Systems and Computers, 2010, 19, 1743-1751.	1.5	2
81	Minimum detectable capacitance in capacitive readout circuits. , 2011, , .		2
82	A high IIP2 and IIP3 CMOS down-conversion active mixer. , 2014, , .		2
83	A simple global resonation strategy for wideband discrete-time MASH &#x03A3;&#x0394; modulators. , 2014, , .		2
84	A zero-crossing based 10-bit 100 MS/s pipeline ADC with controlled current in 90Ânm CMOS. Analog Integrated Circuits and Signal Processing, 2014, 80, 141-151.	1.4	2
85	An NTF-enhanced time-based continuous-time sigma-delta modulator. Analog Integrated Circuits and Signal Processing, 2015, 85, 283-297.	1.4	2
86	A wide-band CMOS active mixer with linearity improvement technique. , 2017, , .		2
87	MASH Î£Î" modulators with a noise-shaped two-step ADC in the second stage. The Integration VLSI Journal, 2017, 56, 77-85.	2.1	2
88	A Digital Method for Offset Cancellation of Fully Dynamic Latched Comparators. , 2021, , .		2
89	A Low Power Wideband Balun-LNA Employing Local Feedback, Modified Current-Bleeding Technique and Balanced Loads. , 2020, , .		2
90	A Fully-Differential Chopper Capacitively-Coupled Amplifier with High Input Impedance for Closed-Loop Neural Recording. Circuits, Systems, and Signal Processing, 2022, 41, 3679-3705.	2.0	2

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91	MASH sigma-delta modulators with reduced sensitivity to the circuit non-idealities. , 2009, , .		1
92	On the design of a less jitter sensitive NTF for NRZ multi-bit continuous-time ΔΣ modulators. , 2009, , .		1
93	A novel frequency compensation scheme for on-chip low-dropout voltage regulators. , 2011, , .		1
94	A linearization technique for active mixers in zero-IF receivers with inherent balun. IEICE Electronics Express, 2011, 8, 2080-2086.	0.8	1
95	On the design and optimization of a switched-capacitor interface circuit for MEMS capacitive sensors. , 2012, , .		1
96	A SAR ADC with an efficient threshold voltage generation. , 2012, , .		1
97	A VERY LOW NOISE WIDEBAND CLASS-C CMOS LC VCO. Journal of Circuits, Systems and Computers, 2012, 21, 1250033.	1.5	1
98	A hybrid CT/DT double-sampled SMASH Î£â†ˆ modulator for broadband applications in 90Ânm CMOS technology. Analog Integrated Circuits and Signal Processing, 2012, 73, 101-114.	1.4	1
99	A new linearization technique for CMOS low noise amplifiers with balun circuitry. , 2013, , .		1
100	An oscillatory noiseâ€shaped quantizer for timeâ€based continuousâ€time sigmaâ€delta modulators. International Journal of Circuit Theory and Applications, 2018, 46, 384-400.	2.0	1
101	A High Input Impedance Fully-Differential Chopper Amplifier for Closed-Loop Neural Recording. , 2020, , .		1
102	A High Dynamic Range Differential Rectifier for RF Energy Harvesting. , 2021, , .		1
103	A Time-Based Analogue-to-Digital Converter for ECG Applications. , 2021, , .		1
104	A Low-Power Low-Noise Neural Recording Amplifier With Improved Telescopic-Cascode OTA. , 2021, , .		1
105	A low-power low-noise neural recording amplifier with an improved recycling telescopic-cascode OTA. AEU - International Journal of Electronics and Communications, 2022, 154, 154312.	2.9	1
106	Efficient double-sampled cascaded .SIGMA..DELTA. modulator topologies for low OSRs. IEICE Electronics Express, 2005, 2, 404-410.	0.8	0
107	A systematic design procedure for CMOS three-stage NMC amplifiers. , 2009, , .		0
108	A double-sampled hybrid CT/DT SMASH ΣΔ modulator for wideband applications. , 2009, , .		0

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109	A new architecture for low-power high-speed pipelined ADCs using double-sampling and opamp-sharing techniques. , 2009, , .		0
110	A simple digital background gain error calibration technique for pipelined ADCs. , 2010, , .		0
111	A digital calibration technique combined with DWA for multibit ΣΔ ADCs. , 2010, , .		0
112	A digital background correction technique combined with DWA for DAC mismatch errors in multibit &#x03A3;&#x0394; ADCs. , 2010, , .		0
113	Dual quantization continuous time &#x03A3;&#x0394; modulators with spectrally shaped feedback. , 2011, , .		0
114	A fast settling on-chip low-dropout regulator with a robust frequency compensation scheme. , 2012, , .		0
115	A noise reduction technique for wideband LNAs in low-power digital TV applications. , 2012, , .		0
116	A ring-type ILFD with locking range of 91% for divide-by-4 and 40% for divide-by-8 with quadrature outputs. , 2013, , .		0
117	Design of a continuous-time &#x03A3;&#x0394; modulator using the time domain quantization approach. , 2014, , .		0
118	An LO architecture with novel wide locking range, quadrature output RILFDs and ILROs for cognitive radio applications. Analog Integrated Circuits and Signal Processing, 2014, 80, 483-498.	1.4	0
119	A fully digital calibration technique for nonlinearity correction in pipelined ADCs. , 2015, , .		0
120	A power conversion chain by coil inductor sharing in voltage converter structure for wireless bio-implants. , 2017, , .		0
121	A Comprehensive Analysis of the Noise Power of Three-Stage OTAs in Switched-Capacitor Circuits. , 2020, , .		0
122	A Wideband Low-Noise Inductor less CMOS Active Mixer With Improved Linearity. , 2021, , .		0
123	A Low-Power Delta-Modulation-Based ADC for Wearable Electrocardiogram Sensors. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3670-3674.	3.0	0