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List of Publications by Year
in descending order

15 papers	**189** citations	1478505 **6** h-index	1720034 **7** g-index
15 all docs	**15** docs citations	**15** times ranked	**139** citing authors

#	Article	IF	Citations
1	Evaluating the Ballistic Transport in nFinFETs: A Carrier Centric Perspective. IEEE Nanotechnology Magazine, 2022, 21, 311-319.	2.0	2
2	3-D non-isothermal particle-based device simulator for p-type MOSFETs. Journal of Computational Electronics, 2021, 20, 1644-1656.	2.5	1
3	3-D TCAD Monte Carlo Device Simulator: State-of-the-art FinFET Simulation. Journal of Integrated Circuits and Systems, 2021, 16, 1-11.	0.4	5
4	A new efficient permutation-diffusion encryption algorithm based on a chaotic map. Chaos, Solitons and Fractals, 2021, 151, 111235.	5.1	9
5	Statistical analysis of the impact of charge traps in p-type MOSFETs via particle-based Monte Carlo device simulations. Journal of Computational Electronics, 2020, 19, 648-657.	2.5	9
6	3-D Monte Carlo device simulator for variability modeling of p-MOSFETs. Journal of Computational Electronics, 2020, 19, 668-676.	2.5	7
7	Maximizing Side Channel Attack-Resistance and Energy-Efficiency of the STTL Combining Multi-Vt Transistors with Current and Capacitance Balancing. , 2019, , .		0
8	A Novel Sizing Method Aiming Security Against Differential Power Analysis. , 2018, , .		1
9	Circuit simulation of workload-dependent RTN and BTI based on trap kinetics. Microelectronics Reliability, 2014, 54, 2364-2370.	1.7	8
10	Use of SSTA Tools for Evaluating BTI Impact on Combinational Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 280-285.	3.1	7
11	Behavioral modeling of continuous-time ΣΔ modulators in matlab/simulink. , 2013, , .		3
12	Atomistic approach to variability of bias-temperature instability in circuit simulations. , 2011, , .		102
13	Time and workload dependent device variability in circuit simulations. , 2011, , .		23
14	Impact of RDF and RTS on the performance of SRAM cells. Journal of Computational Electronics, 2010, 9, 122-127.	2.5	8
15	NBTI-aware technique for transistor sizing of high-performance CMOS gates. , 2009, , .		4