

Andrea Bonfanti

List of Publications by Year in descending order

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43
papers

1,294
citations

471371

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30
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times ranked

865
citing authors

#	ARTICLE	IF	CITATIONS
1	A 900-MS/s SAR-Based Time-Interleaved ADC With a Fully Programmable Interleaving Factor and On-Chip Scalable Background Calibrations. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3645-3649.	2.2	0
2	A Generalization of the Groszkowski's Result in Differential Oscillator Topologies. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2800-2812.	3.5	3
3	A Drift-Resilient Hardware Implementation of Neural Accelerators Based on Phase Change Memory Devices. IEEE Transactions on Electron Devices, 2021, 68, 6076-6081.	1.6	6
4	On amplitude-gain-control optimization for Lissajous frequency modulated MEMS gyroscopes. , 2021, , .		2
5	Fully Integrated, 406 μs , 5×10^5 /hr, Full Digital Output Lissajous Frequency-Modulated Gyroscope. IEEE Transactions on Industrial Electronics, 2019, 66, 7386-7396.	5.2	30
6	High Scale-Factor Stability Frequency-Modulated MEMS Gyroscope: 3-Axis Sensor and Integrated Electronics Design. IEEE Transactions on Industrial Electronics, 2018, 65, 5040-5050.	5.2	48
7	Efficient Behavioral Simulation of Charge-Pump Phase-Locked Loops. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1968-1980.	3.5	12
8	The First Frequency-Modulated (FM) Pitch Gyroscope. Proceedings (mdpi), 2017, 1, 393.	0.2	5
9	A 70.7-dB SNDR 100-kS/s 14-b SAR ADC with attenuation capacitance calibration in 0.35- μm CMOS. Analog Integrated Circuits and Signal Processing, 2016, 89, 357-371.	0.9	7
10	A 64-Channel 965- μs & 10×10^5 /hr, Neural Recording SoC With UWB Wireless Transmission in 130-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 528-532.	2.2	18
11	Fundamental Power Limits of SAR and $1/f$ Analog-to-Digital Converters. , 2015, , .		1
12	A Compact and Autoclavable System for Acute Extracellular Neural Recording and Brain Pressure Monitoring for Humans. IEEE Transactions on Biomedical Circuits and Systems, 2015, 9, 50-59.	2.7	2
13	A programmable closed-loop recording and stimulating wireless system for behaving small laboratory animals. Scientific Reports, 2015, 4, 5963.	1.6	30
14	A Sub-400-nT & 10×10^5 /hr, Multi-Loop MEMS Magnetometer With Integrated Readout Electronics. Journal of Microelectromechanical Systems, 2015, 24, 1938-1950.	1.7	24
15	A Modeling Environment for the Simulation and Design of Charge Redistribution DACs Used in SAR ADCs. , 2014, , .		3
16	A 6-f/conversion-step 200-kSps asynchronous SAR ADC with attenuation capacitor in 130-nm CMOS. Analog Integrated Circuits and Signal Processing, 2014, 81, 181-194.	0.9	8
17	Impact of non-quasi-static effects on $1/f^3$ phase noise in a 1.9-to-2.6 GHz oscillator. , 2014, , .		1
18	Suppression of Flicker Noise Up-Conversion in a 65-nm CMOS VCO in the 3.0-to-3.6 GHz Band. IEEE Journal of Solid-State Circuits, 2013, 48, 2375-2389.	3.5	75

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19	A Unified Method for the Analysis of Phase and Amplitude Noise in Electrical Oscillators. IEEE Transactions on Microwave Theory and Techniques, 2013, 61, 3277-3284.	2.9	14
20	Simulating phase noise induced from cyclostationary noise sources. , 2013, , .		4
21	Analysis and Minimization of Flicker Noise Up-Conversion in Voltage-Biased Oscillators. IEEE Transactions on Microwave Theory and Techniques, 2013, 61, 2382-2394.	2.9	57
22	Reducing flicker noise up-conversion in a 65nm CMOS VCO in the 1.6 to 2.6 GHz band. Proceedings of SPIE, 2013, , .	0.8	0
23	A simulation technique to compute phase noise induced from cyclostationary noise sources in RF oscillators. Proceedings of SPIE, 2013, , .	0.8	0
24	Efficient Calculation of the Impulse Sensitivity Function in Oscillators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 628-632.	2.2	27
25	An efficient linear-time variant simulation technique of oscillator phase sensitivity function. , 2012, , .		19
26	Flicker Noise Up-Conversion due to Harmonic Distortion in Van der Pol CMOS Oscillators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1418-1430.	3.5	40
27	A Multi-Channel Low-Power System-on-Chip for in Vivo Recording and Wireless Transmission of Neural Spikes. Journal of Low Power Electronics and Applications, 2012, 2, 211-241.	1.3	0
28	Origins of $1/f^2$ scaling in the power spectrum of intracortical local field potential. Journal of Neurophysiology, 2012, 107, 984-994.	0.9	46
29	A wireless microsystem with digital data compression for neural spike recording. Microelectronic Engineering, 2011, 88, 1672-1675.	1.1	4
30	A multi-channel low-power system-on-chip for single-unit recording and narrowband wireless transmission of neural signal. , 2010, 2010, 1555-60.		19
31	A 2.5-GHz DDFS-PLL With 1.8-MHz Bandwidth in 0.35- μm CMOS. IEEE Journal of Solid-State Circuits, 2008, 43, 1403-1413.	3.5	21
32	A low-power integrated circuit for analog spike detection and sorting in neural prosthesis systems. , 2008, , .		12
33	A multistandard ΣΔ fractional-N frequency synthesizer for 802.11a/b/g WLAN. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2007, , .	0.0	1
34	A Compact Multichannel System for Acquisition and Processing of Neural Signals. Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 2007, 2007, 441-4.	0.5	15
35	An integrated low-noise multichannel system for neural signals amplification. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2007, , .	0.0	5
36	5-GHz Oscillator Array With Reduced Flicker Up-Conversion in 0.13- μm CMOS. IEEE Journal of Solid-State Circuits, 2006, 41, 2457-2467.	3.5	30

#	ARTICLE	IF	CITATIONS
37	A varactor configuration minimizing the amplitude-to-phase noise conversion in VCOs. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 481-488.	0.1	37
38	A 15-GHz broad-band $\sqrt{\text{divide}/2}$ frequency divider in 0.13- μm CMOS for quadrature generation. IEEE Microwave and Wireless Components Letters, 2005, 15, 724-726.	2.0	28
39	Differentially-Tuned VCO with Reduced Tuning Sensitivity and Flicker Noise Up-Conversion. Analog Integrated Circuits and Signal Processing, 2005, 42, 21-29.	0.9	6
40	A DDS-based PLL for 2.4-GHz frequency synthesis. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2003, 50, 1007-1010.	2.3	29
41	Frequency dependence on bias current in 5 GHz CMOS VCOs: impact on tuning range and flicker noise upconversion. IEEE Journal of Solid-State Circuits, 2002, 37, 1003-1011.	3.5	256
42	Analysis and design of a 1.8-GHz CMOS LC quadrature VCO. IEEE Journal of Solid-State Circuits, 2002, 37, 1737-1747.	3.5	349
43	A voltage-controlled oscillator for IEEE 802.11a and HiperLAN2 application. , 0, , .		0